INSTRUCTION MANUAL

8010B

ELECTRONIC COUNTER

DANA

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8010B
ELECTRONIC COUNTER

DANA LABORATORIES, INC.
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ERRATA SHEET

1. Pages 5-21, 5-23, 5-25, 5-27, 5-29, 5-31, 5-33, 5-35, and 5-37
   a. R69 is 100; should be 10
   b. R75 is 2K; should be 1K
   c. R76 is 3K; should be 1.5K

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SPECIFICATIONS

FREQUENCY MEASUREMENTS to 150 MHz	
Frequency Range:	
dc coupled:	0 to 150 MHz
ac coupled:	10 Hz to 150 MHz
Accuracy:	±1 count ±reference error
Input:	Channel A
Input Characteristics:	
Sensitivity*, sinewave:	50 mV rms to 100 MHz; 100 mV rms to 150 MHz
Sensitivity, pulse:	150 mV peak; 4 nsec minimum width
Impedance:	1 megohm shunted by 25 pF
Maximum input (without damage):	250V rms or 300V peak on all ranges except 150V rms or 200V peak to 1 MHz on 1V range
Voltage ranges:	1, 10, 100 selectable
Trigger level:	Continuously adjustable to ±300% of input voltage range
Trigger slope:	+ or −, selectable
Preset condition:	0 trigger level
Measurement Time:	1 μsec to 100 seconds, selectable in decade steps
Display:	8 digits (optional 9 digits), KHz or MHz
Self Check:	10 MHz

FREQUENCY MEASUREMENTS to 550 MHz (Models 8020B, 8030B)	
Frequency Range:	
ac coupled:	1 MHz to 550 MHz
Accuracy:	±1 count ±reference error
Input:	Channel C
Input Characteristics:	
Sensitivity, sinewave:	50 mV rms (1 mV with optional 030 prescaler)
Impedance:	50 ohms nominal
Maximum Input: (operating)	1V rms
Maximum Input: (without damage)	5V rms
Automatic Gain Control:	26 dB without adjustment (60 dB with option 030)

*Derate 10 dB above 50 MHz if equipped with Option 010

TIME INTERVAL MEASUREMENTS (Models 8010B, 8030B)	
Range:	100 nsec to 10^9 sec (10^{10} sec with option 004)
Resolution:	100 nsec
Accuracy:	±1 count ±reference error ±trigger error*
Input:	
separate mode:	Channel A start and Channel B stop
common mode:	Channel A start and stop
Input Characteristics:	Channel A and B same as described in Frequency Ratio Mode
Display:	μsec, msec, sec

TIME INTERVAL AVERAGE (Models 8010B, 8030B)	
Range:	150 psec to 10 sec (100 sec with option 004)
Accuracy:	$\pm\text{reference error} \pm 2\text{ nsec} \pm \frac{(\text{trigger error}^* \pm 100\text{ nsec})}{\sqrt{\text{No. of Intervals Averaged}}}$
Input:	same as time interval
Intervals Averaged:	1 to 10^8, selectable in decade steps
Display:	nsec, μsec
Min. Time between Stop & Start:	200 nsec

FREQUENCY RATIO MEASUREMENTS (Models 8010B, 8030B)	
Frequency Range:	
Input F_A	0 to 150 MHz
Input F_B	0 to 10 MHz
Ratio Range:	10^{-8} to 10^8 (10^9 sec with option 004)
Multiplier:	F_B scaled by 1 to 10^9 selectable in decade steps
Accuracy:	± 1 count of $F_A \pm \frac{\text{trigger error of } F_B}{\text{multiplier}}$
Display:	Dimensionless

*Trigger error $< \frac{0.0025\ \mu\text{sec}}{\text{Signal Slope V}/\mu\text{sec}}$

SPECIFICATIONS continued

PERIOD MEASUREMENTS	
Range:	100 nsec to 10^9 sec (10^{10} sec with option 004)
Resolution:	100 nsec
Accuracy:	±1 count ±reference error ±trigger error**
Input:	Channel A
Display:	μsec, msec, and sec

PERIOD AVERAGE	
Range:	100 nsec to 10 sec (100 sec with option 004)
Accuracy:	$\pm 1 \text{ count} \pm \text{reference error} \pm \frac{\text{trigger error}^{**}}{\text{No. of periods averaged}}$
Input:	Channel A
Periods Averaged:	1 to 10^8 selectable in decade steps
Display:	nsec, μsec, msec

TOTALIZE MEASUREMENTS	
Frequency Range:	0 to 150 MHz
Input:	Channel A
Count Range:	0 to 10^8 (10^9 sec with option 004)
Accuracy:	±1 count/gate

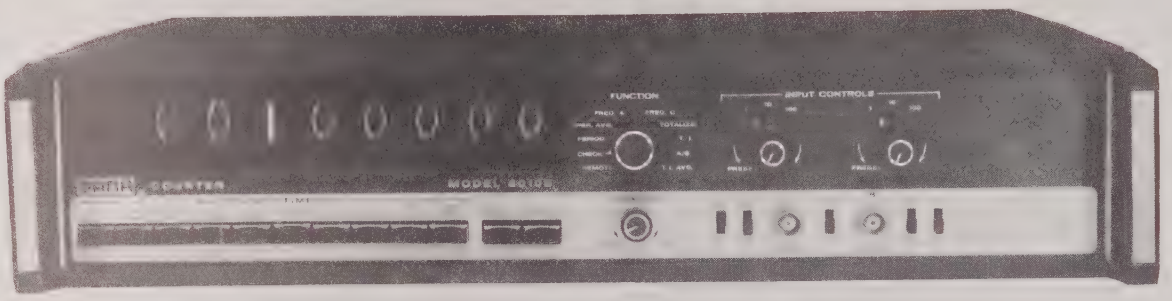
SCALING	
Frequency Range:	0 to 150 MHz
Scaling Range:	10 to 10^{10} selectable in decade steps

GENERAL SPECIFICATIONS	
Internal Reference Oscillator Characteristics:	
Aging Rate:	$<3 \times 10^{-7}$ per month
Temperature Stability:	$\pm 2.5 \times 10^{-6}$, 0°C to + 50°C
Voltage Stability:	$\pm 1 \times 10^{-7}$, with 10% line voltage variation
Time Base:	.01 Hz to 10 MHz selectable in decade steps
Output:	10 MHz square wave, buffered, TTL compatible
External Reference:	1, 5, or 10 MHz 1V rms into 1 kilohm; selectable by internal/external switch
Marker Output:	Negative-going pulse, 15 volt amplitude, rear BNC, duration equal to channel A trigger point to channel B trigger point
Display:	Long-life digital display tubes; 8 standard, 9 optional (option 004)
Input/Output Connectors:	BNC
Operating Temperature:	0° to 50°C
Line Voltage:	50 Hz to 400 Hz; 115V ± 10%
Power Requirement:	60 watts maximum
Weight:	Net, 15 pounds; shipping, 20 pounds
Dimensions: (HxWxD)	3-15/32 x 16-3/4 x 14 inches; 88 x 425 x 356 millimeters

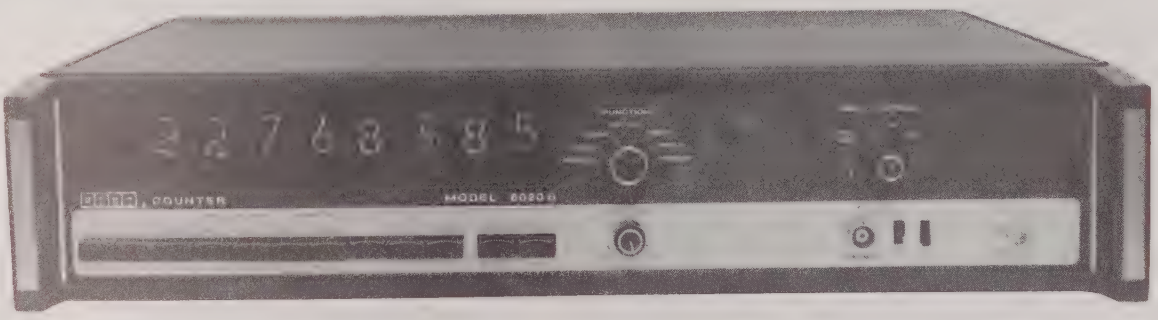
$$^{**}\text{Trigger error} \leq \frac{0.3}{(S/N)Fa}$$

where S/N equals signal to noise ratio and Fa equals frequency.

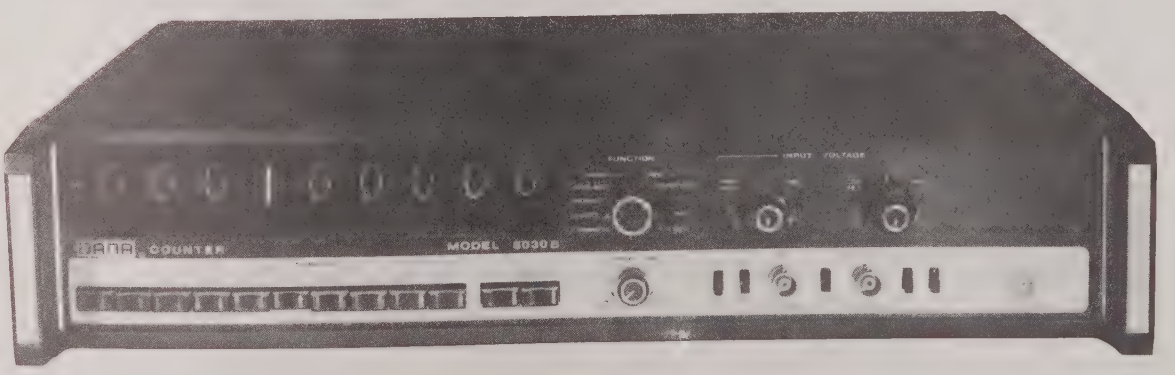
OSCILLATOR OPTIONS		
	Option 050	Option 200
Aging Rate/day:	–	$1x10^{-9}$
Aging Rate/month:	$1x10^{-7}$	$3x10^{-8}$
Temperature Stability, 0° to 50°C:	$\pm 5x10^{-7}$	$\pm 5x10^{-9}$
±10% line voltage stability:	$\pm 5x10^{-8}$	$\pm 5x10^{-9}$
Warmup*:	1 hour	72 hours
*Time to reach aging specification after 24 hours off.		



8010B



8020B



8030B

Figure 1.1 - Models 8010B, 8020B, and 8030B

SECTION 1 GENERAL DESCRIPTION

1.1 SCOPE.

1.2 This manual contains installation, operation, and maintenance instructions for the Dana Models 8010B, 8020B, and 8030B electronic counters (figure 1.1). All models and optional features are covered; therefore, all descriptions may not apply to a particular instrument.

1.3 GENERAL DESCRIPTION.

1.4 Each model in the 8000B Series is self-contained for its intended range of applications. No external or plug-in accessories are required. All models have a minimum of four measurement modes: Frequency, Period, Multiple Period Average, and Totalize. Additional measurement modes of Time Interval, Time Interval Average, and Frequency Ratio are available in certain models. All models operate at frequencies up to 150 MHz. Models 8020B and 8030B operate at RF frequencies. The capability of each model is shown in table 1.1.

1.5 An eight digit display and a high stability reference oscillator provides the standard counter with capability to make meaningful frequency measurements to an accuracy up to 1 part in 10^8. For more demanding applications, a nine digit display and correspondingly higher stability reference oscillators, are available as options.

1.6 The standard temperature compensated crystal oscillator (TCXO) in the counter serves as an ideal reference in a general purpose counter. The average aging rate is 3×10^{-7} per month. Since no temperature controlled oven is used, extended warmup times are not required when moving the counter from one location to another.

1.7 Time Interval Measurements.

1.8 The use of low noise FET input circuitry provides 50 millivolt sensitivity to 100 MHz with a constant 1 megohm input impedance on both the start and stop input channels. The input circuitry includes a three-position attenuator and controls for: trigger level, slope, and coupling, so that triggering can be optimized for non-sinusoidal waveforms.

1.9 Because of high stability input amplifiers, trigger levels will drift less than 5% of full scale over a $10^{o}C$ temperature range and 200 hours of operating time after initial setting. Frequency adjustments to the counter are not necessary during the instrument warmup period or when changes in temperature occur.

1.10 While making a time interval measurement, it is often useful to observe the waveform under test with an oscilloscope. The counter's marker output may be connected to most oscilloscopes to provide a continuous brightening of that portion of the waveform between the start measurement point and the stop point.

1.11 With time interval average capability in the 8010B and 8030B, measurement accuracy and resolution can be improved when measuring repetitive signals. Propagation delays through integrated circuits can be measured to accuracies better than 150 ps when input signal is asynchronous with respect to the counter timebase.

1.12 Two analog outputs are provided on all models with time interval capability for accurately monitoring trigger level settings. The 50% point and 10% - 90% rise time points can be set accurately by measuring the analog voltage outputs with a digital voltmeter.

Table 1.1 - Measurement Capability

Model	Totalize	Period	Period Average	Freq to 150 MHz	Freq to 550 MHz	Ratio	Time Interval	Time Interval Average
8010B	X	X	X	X		X	X	X
8020B	X	X	X	X	X			
8030B	X	X	X	X	X	X	X	X

1.13 RF Measurements.

1.14 Models 8020B and 8030B have RF measurement capability. These counters feature RF amplifiers capable of meaningful measurements as low as 50 mV with the standard prescaler, or as low as 1 mV (–47 dBm) with an optional prescaler (Option 030). Low level, RF signals can therefore be measured without external amplification.

1.15 To measure frequencies between 1 and 550 MHz, the operator simply connects the unknown signal to the input and reads the result. By using a prescaler, both the need for manual tuning and possibility of an incorrect setting have been eliminated. Triggering is automatically optimized for input signal amplitude from 50 millivolts to one volt with the standard prescaler, or from 1 mV to 1 volt with an optional prescaler.

1.16 A wide-band automatic gain control, coupled with excellent sensitivity, enable the carrier frequency of an amplitude modulated signal to be measured. Full accuracy is maintained with greater than 90% amplitude modulation (99% with optional prescaler). Frequency modulated carriers can also be measured as long as the frequency components are within the 1 to 550 MHz bandwidth.

1.17 Models 8020B and 8030B are equipped with a 550 MHz prescaler. The prescaler maintains the stability and accuracy of the basic 150 MHz counter at radio frequencies. Only 40 milliseconds are required to measure 550 MHz to a resolution of 2 parts in 10^{-7}. This fast measurement time is due to the prescaler's capability to divide the input signal and multiply the measurement time by four.

1.18 OPTIONS.

1.19 All options on the 8000B Series counters should be ordered at the time of purchase. However, the Option 030 RF prescaler (1 mV sensitivity, 10 MHz to 500 MHz) and the Rack Mount Adaptor may be added at anytime.

1.20 Rack Mounting Adaptors, Option 003.

1.21 Rack mounting adaptors are used where the instrument is to be installed in a relay-rack or cabinet.

1.22 Ninth-Digit Readout, Option 004.

1.23 The 9th Digit Readout adds one more digit to the eight digit counter. The 9th Digit increases the accuracy to 1 part in 10^9.

1.24 Systems Interface, Options 008/009.

1.25 The systems interface, which includes BCD and remote programming input, is available for all counters. The Option 008 features single line control of function, time base, external gate, +/– slope, hold, and reset and provides analog control of trigger level. The Option 009 features BCD encoded commands for control of function, time base, channel range and trigger level and provides single line control of external gate, +/– slope, hold, reset, separate/common, and ac/dc. Analog control of trigger level is also provided.

1.26 All remote programming and BCD outputs are compatible with TTL logic levels. This allows the Series 8000B counters to be interfaced directly to control and recording devices without requiring level shifting and buffer circuitry. The operation and installation of the options is described in the 008/009 Interface Manual 980469.

1.27 Rear Input, Option 010.

1.28 The Rear Input provides the user a rear-panel connector for Frequency A, Frequency B (not in Model 8020B) and Frequency C (not in Model 8010B) input signals. The Rear Input option reduces the sensitivity of Frequency A 10 dB above 50 MHz.

1.29 Prescaler (1 mV Sensitivity, 10 MHz to 500 MHz), Option 030.

1.30 The Option 030 Prescaler is available on Models 8020B and 8030B. It replaces the standard Prescaler and offers sensitivity as low as 1 mV (–47 dBm). Maximum usable input is 1 volt rms and 5V rms without damage to the prescaler.

1.31 TCXO, Option 050.

1.32 The Option 050 Temperature-Compensated Crystal Oscillator offers a lower aging rate per month, and better voltage and temperature stability than the standard TCXO oscillator.

1.33 Oven Oscillator, Option 200 & 300.

1.34 The Option 200 oven oscillator provides an ultra-stable timebase – extending the time between calibrations and serving as a secondary frequency standard. The oven oscillator is in continuous operation whenever the counter is attached to the power line. The Option 300 is the same as the Option 200 with half the aging rate.

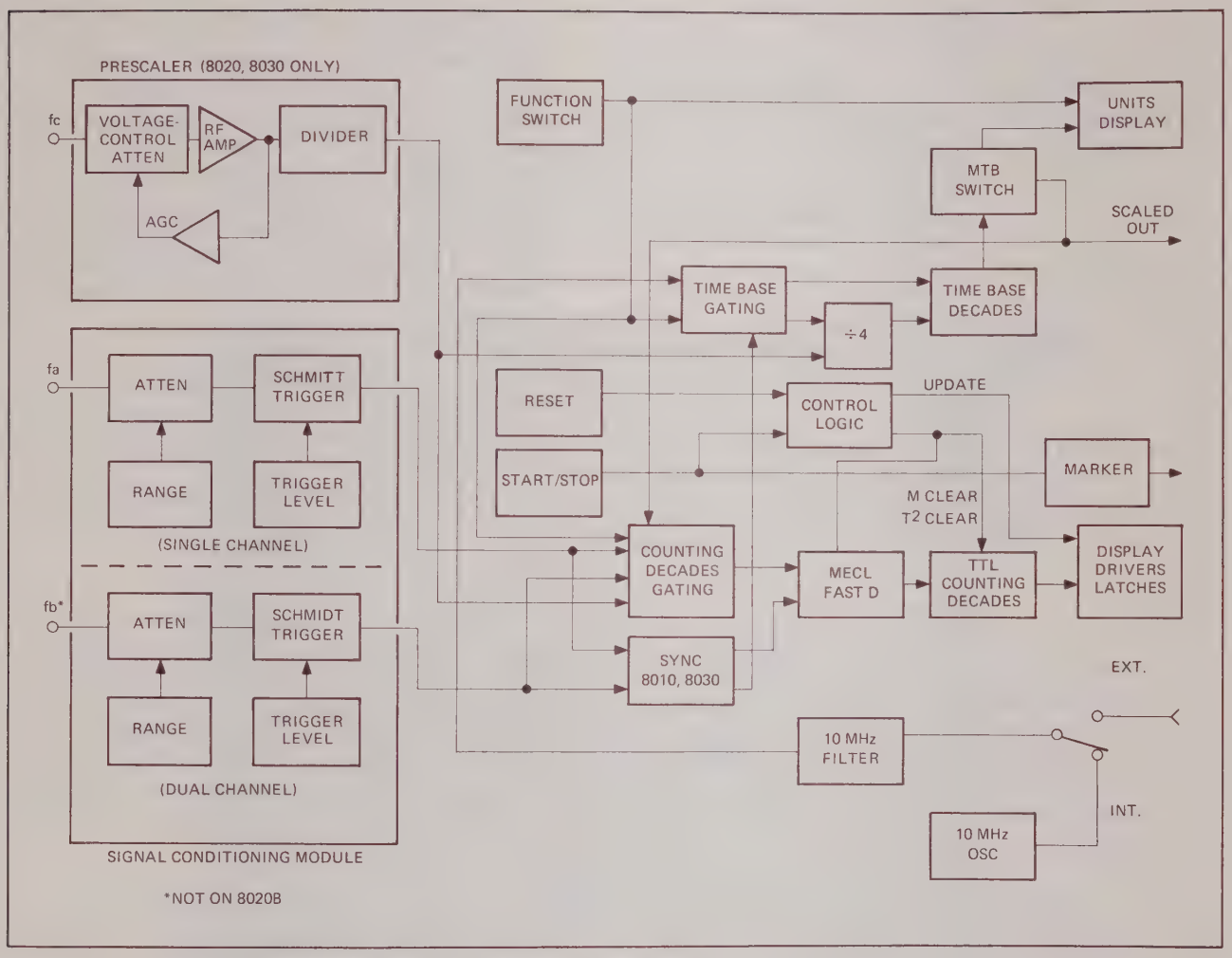


Figure 1.2 - Block Diagram

1.35 ELECTRICAL DESCRIPTION.

1.36 A basic block diagram of the instrument is shown in figure 1.2. Input channels A and B are identical through the attenuator and signal conditioning amplifiers. The input is routed through the BNC input connectors and through the AC/DC coupling switch to the attenuator. The attenuator has three positions: X1 range, X10 range, and X100 range. The attenuator output is applied to the signal conditioning amplifier through an overload circuit that protects the circuitry if an "overload" voltage is applied.

1.37 The signal conditioning amplifier is a low-drift dc-coupled Schmitt trigger circuit. Any point on the input waveform can be selected to trigger the Schmitt circuit by front panel controls: the +/– switch selects either positive or negative slope and the INPUT CONTROLS select the amplitude. Output pulses generated by the Schmitt trigger circuit are applied to the Steering Logic and to the Marker Generator.

1.38 The Marker circuit provides a marker pulse used to intensity-modulate an oscilloscope display. It starts when channel A triggers and terminates when channel B triggers. The pulse represents a precise measurement of the time between channel A and channel B. The oscilloscope trace displays the point where the time measurement starts and terminates. The trigger levels can be adjusted very accurately with the use of the oscilloscope.

1.39 Frequency C (except in Model 8010B) is applied directly to the Prescaler that contains a voltage-controlled attenuator (VCA), RF amplifier, and two high frequency divide-by-two circuits. The dividers scale the input frequency by a factor of four. This is necessary to reduce the frequency to that acceptable by the ECL logic. The voltage-controlled attenuator and RF amplifiers combine to provide automatic ranging over input amplitude variations of 60 dB throughout the operating frequency.

Table 1.2 - Logic Functions of Multiplier Timebase (M/TB) Per Mode

Mode of Operation	Function of MTB switches
Frequency A	Selects gate time
Frequency C	Selects gate time
Period	Selects reference frequency to be counted
Period Average	Selects number of periods to be averaged
Time Interval	Selects the reference frequency to be counted during the time interval A to B
Time Interval Average	Selects number of periods to be averaged
Ratio A/B	Selects number of periods of channel B input to be used as the gate time
Self Test	Selects gate time

1.40 Reference Conditioning receives a reference frequency from either the internal reference oscillator or from the External Reference input. External reference inputs of 1 MHz, 5 MHz, or 10 MHz are buffered, amplified, and applied to a Schmitt trigger circuit to produce harmonics at 10 MHz. A filter rejects frequencies other than 10 MHz. The reference signal is passed on to the digital logic section.

1.41 The counting and multiplier timebase steering logic routes the inputs to the proper set of decades corresponding to the selected operating mode of the instrument. It "steers" the inputs upon commands from the FUNCTION switch.

1.42 Signals to the Control Logic Section are generated by logic in the following blocks in figure 1.2: Multiplier/ Timebase (M/TB) Decades and Start/Stop Logic. The M/TB Decades consist of eight TTL decade counters which, together with Start/Stop Logic, inputs from the Steering Logic, M/TB switches on front panel, and the function switch, control operation of the Control Logic. The circuits combine to perform the functions listed in table 1.3 for each operating mode. The M/TB Decades supply a scaled output to a rear panel connector in the Totalize mode. The output is 1/10N x input frequency, where N is the Multiplier setting on the front panel.

1.43 The M/TB switch and the FUNCTION switch operates in conjunction with the Decimal Point Logic and Units Logic to provide proper annunciators and decimal point locations. They also control other logic contributing to the functions listed in table 1.2.

1.44 Timing of the counter is governed by the Control Logic. After the counter is "armed", it opens the Gate upon command of the Start/Stop Logic. After the Gate goes low, two additional pulses are generated: a Prop-Delay (proper delay) pulse and a Display Time pulse. The Prop-Delay allows for settling time of the accumulated count in the counter decades before Update and Print commands are generated. The Display Time pulse, with width determined by the front panel DISPLAY TIME control, controls the length of time that the accumulated count is displayed before the decades are cleared in preparation for a new count.

1.45 The DISPLAY TIME control on the front panel performs three functions. The CCW position removes power from the display tubes and disables the $\pm$18V and +5V supplies. The CW position HOLD allows the meter to hold a measured count indefinitely. Mid-range of the control provides a continuously variable sample rate from 30 msec to over 5 seconds.

1.46 The STORAGE Switch is a two-position switch (storage-off, storage-on) located on the rear panel. When the switch is in the ON position, the display is continuous and changes only when the measurement is different from that counted during the previous measurement cycle. The OFF position disables the display storage so that the accumulation of the count can be observed by the operator. The RESET switch on the front panel enables the operator to start a new measurement cycle.

1.47 The START/STOP switch on the front panel manually generates the Start/Stop commands to the main gate. This switch is used in Totalize mode.

1.48 The Readout assembly is made up of eight in-line display devices with decimal inputs, five annunciator lamps and a main gate annunciator. The count is displayed by the display devices with correctly positioned decimal points and annunciator indicators (nsec, μsec, sec, KHz, and MHz). The gate annunciator indicates the opening and closing of the main gate.

1.49 The counting decades consist of one high-speed decade made up of ECL (emitter-coupled-logic) and seven TTL decade counters. Each decade applies the accumulated count data in BCD format to the Latches and Drivers. The latches are D-type flip-flops which can store a count for a indefinite period of time. When the STORAGE switch is on, the display is continuous and changes only when the measurement is different from that counted during the previous measurement time. The drivers are BCD-to-ten-line decoders that provide a decoded decimal output to light the corresponding numeral on the readout tube.

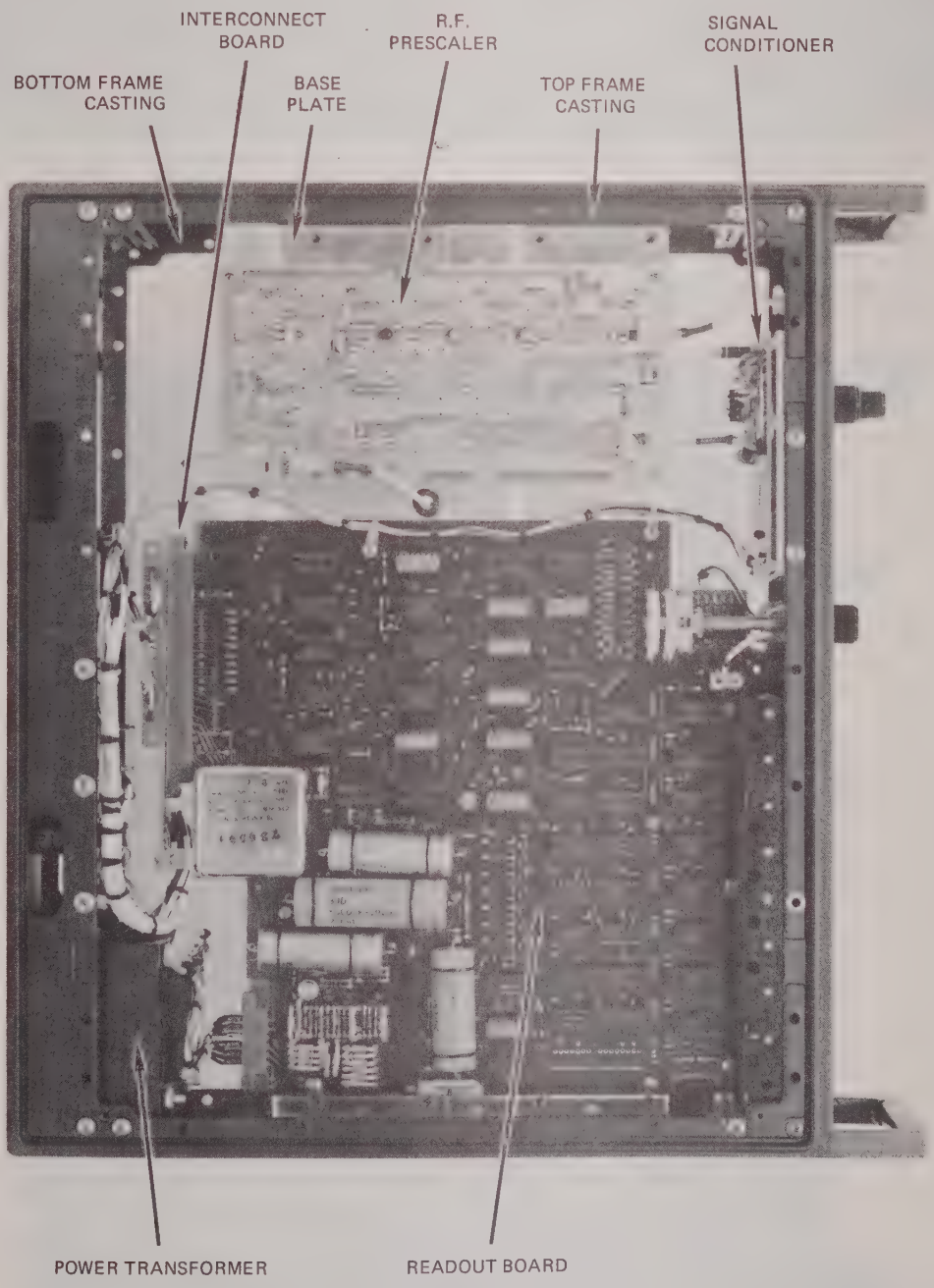


Figure 1.3 - Top View

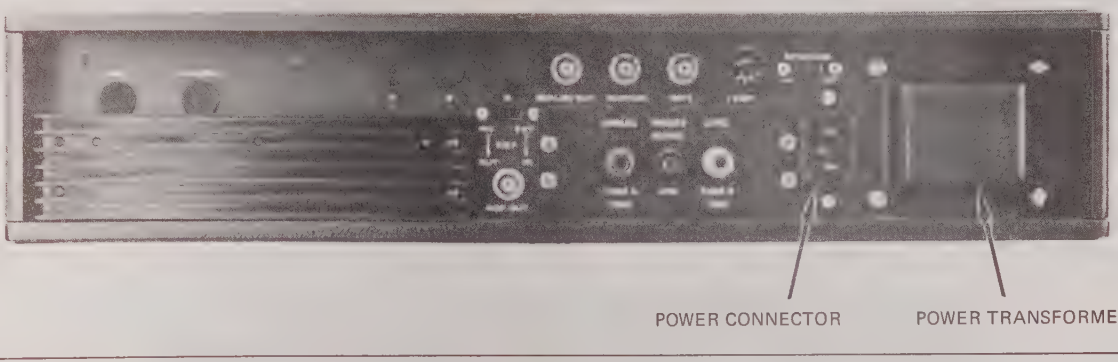


Figure 1.4 - Rear Panel

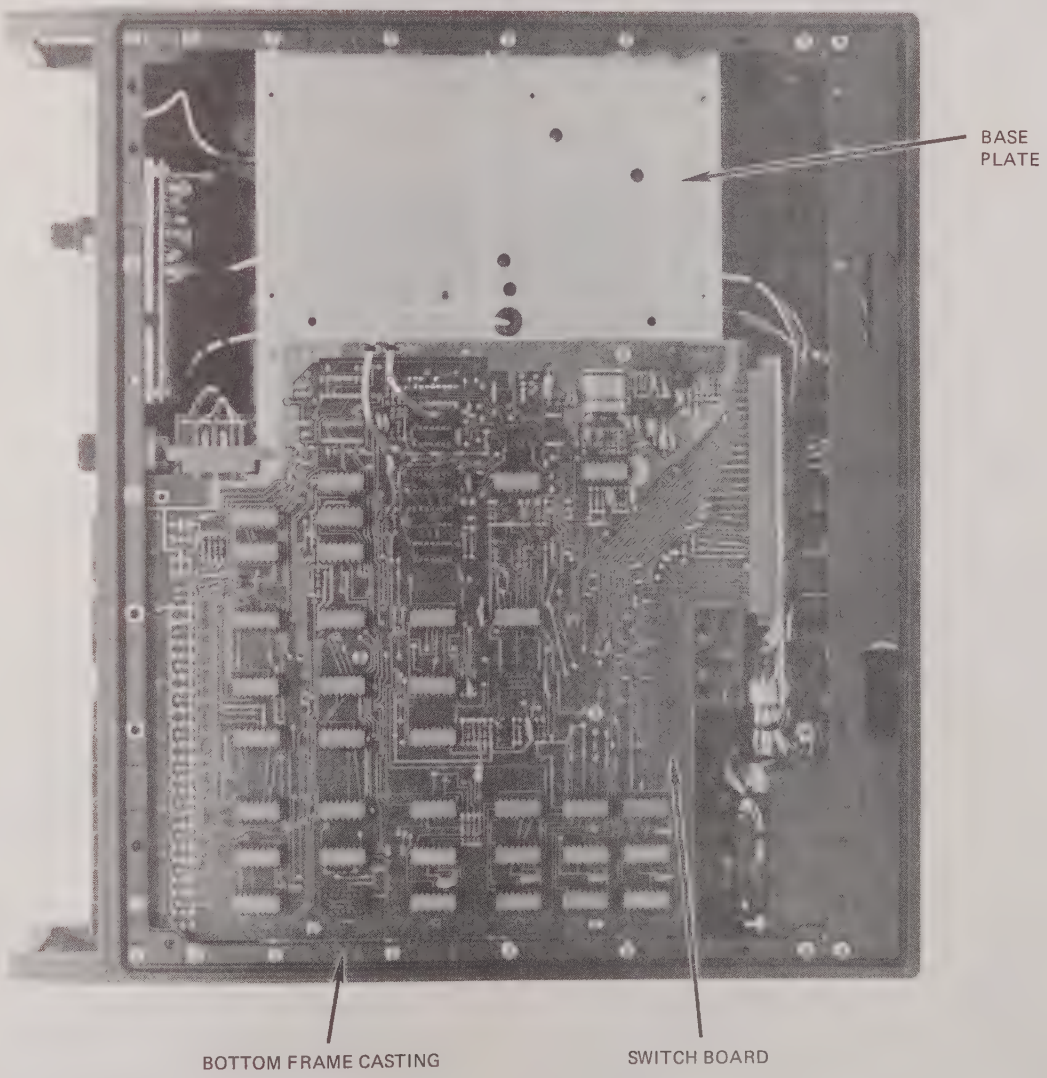


Figure 1.5 - Bottom View

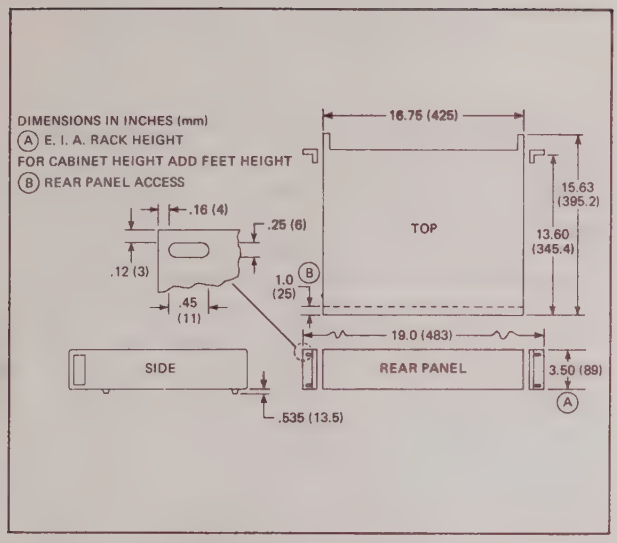


Figure 1.6 - Dimensions

1.50 MECHANICAL DESCRIPTION.

1.51 A top view of the counter is shown in figure 1.3. The counter shown (8020B) is equipped with the RF prescaler mounted on the base plate. The Readout board is mounted on the top of the base plate. The Interconnect board connects the Readout board and the Switch board together electrically at the rear of the Readout and Switch board. The signal conditioner is attached to the front panel. The power transformer and rear panel are one assembly. The rear panel (figure 1.4) assembly is clamped between the top and bottom frame castings.

1.52 The bottom view of the counter is shown in figure 1.5. The Switch board is mounted on the base plate. The base plate is attached to the bottom frame casting.

1.53 A dimensional outline of the 8000B series counter is shown in figure 1.6.

2.1 UNPACKING AND INSPECTION

2.2 The Series 8000B Counter is packed in a molded plastic-foam form within a cardboard carton for shipment. The plastic form holds the Counter securely in the carton and absorbs any reasonable external shock normally encountered in transit. Prior to unpacking, examine the exterior of the shipping carton for any signs of damage. Carefully remove the Counter from the carton and inspect the exterior of the instrument for any signs of damage. If damage is found, notify the carrier immediately.

2.3 Included with the Counter packed in the container are the instruction manual, Dana Part Number 980448, and power cord 403530. Counters which are equipped with remote programming and BCD output (Option 008 systems interface) are shipped with three mating connectors, 600698, and keys included.

2.4 BENCH OPERATION.

2.5 Each Counter is equipped with a tilt bail or "kickstand" to enable the front of the instrument to be elevated for convenient bench use. The tilt bail is attached to the two front supporting "feet" at the bottom of the instrument. For use, the bail is pulled down to its supporting position.

2.6 RACK MOUNTING.

2.7 The instrument can be mounted in a standard 19-inch rack with the optional rack-mounting flanges (403402, includes attaching hardware). To install the flanges, proceed as follows:

a. With instrument on its side, remove four Phillips-head screws holding bottom cover. Remove cover. Remove screws holding feet (and bail) in place. Replace bottom cover.

b. Place one of the supplied screws through each of the two holes in the mounting flange (figure 2.1). Thread a securing nut onto each screw just enough to attach it to the screw (approximately one turn).

c. Place the mounting flange onto the mounting slot in the instrument side panel so that the securing nuts fit entirely into the slot. Be sure the rack-mount slots on the flange are toward the front of the instrument.

d. Tighten screws. The securing nuts will rotate and hold the flange securely in place.

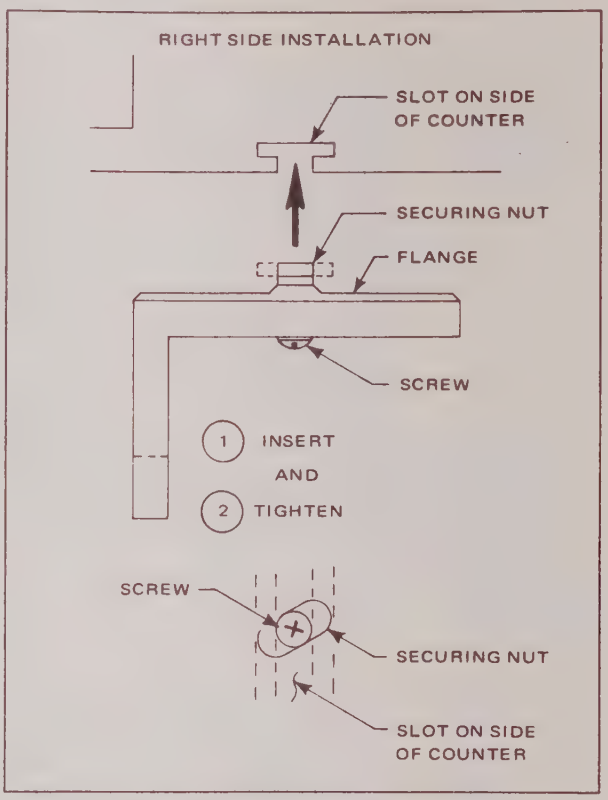


Figure 2.1 - Rack Mount Installation

2.8 POWER CONNECTIONS.

2.9 Power requirements for domestic units are 115V ± 10%, 50 to 400 Hz. Power consumption is 60 watts maximum. All 8000B series counters are adaptable for 230V operation. Figure 2.2 shows input wiring for 230V ± 10% line voltage.

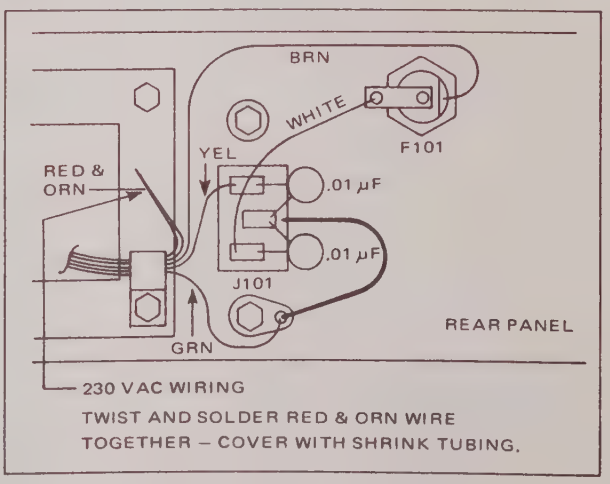


Figure 2.2 - 230V Operation

2.10 Power Cable.

2.11 A standard power cable having a three-pin plug is supplied with the counter. The cord connects to the power connector J101. The ground pin (round) is attached to the main frame of the counter. It is important that this pin be connected to a good quality earth ground.

2.12 Fuse.

2.13 The power fuse holder is located on the rear panel of the counter. A .75 amp 3AG fuse is used.

2.14 REMOTE PROGRAMMING AND BCD OUTPUT.

2.15 Information on the p mming and output options available for the 8000B s Counters is provided in Manual No. 980469, Syst nterface for the 8000B series Counter.

2.16 OPERATING PROCEDURES.

2.17 Table 2.1 describes the function of each operating control and each connector on the instrument. Tables 2.2 through 2.9 describe procedures for operating the instrument in each of the measurement modes.

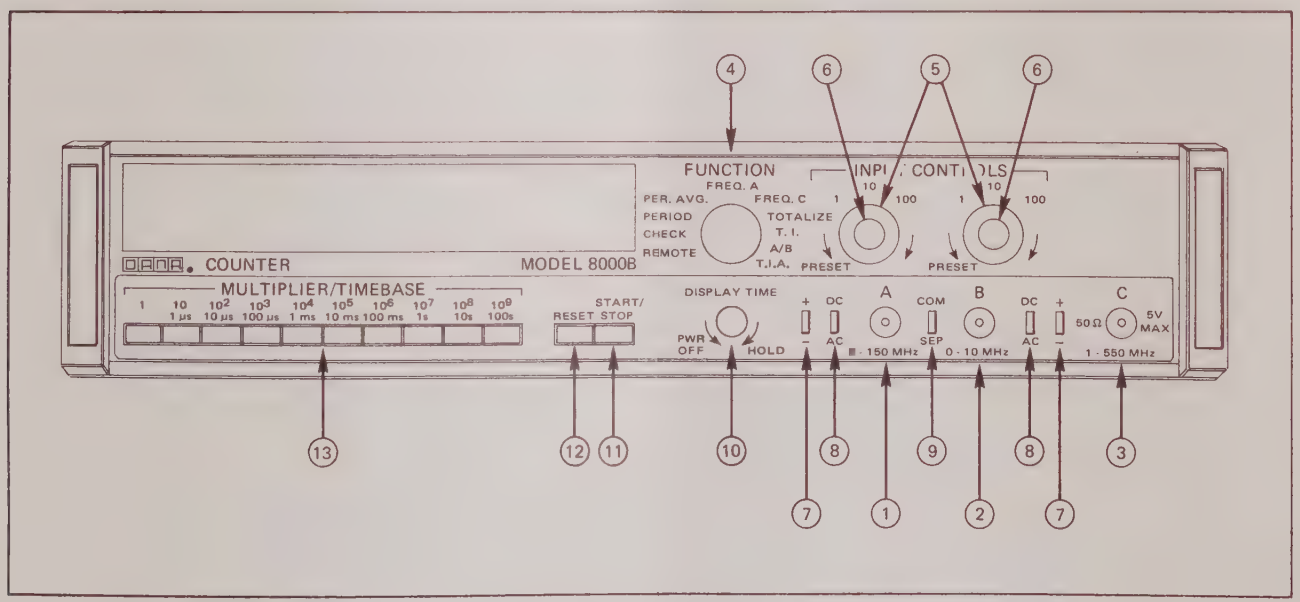


Figure 2.3 - Front Panel

Table 2.1 - Controls and Connectors (see figure 2.3)

input connectors (BNC type)	(1) A INPUT	Used for each function except FREQ C (500 MHz). It accepts up to 250V RMS or 300V peak on all ranges except 150V RMS or 200V peak to 1 MH on 1V range without damage.
	(2) B INPUT*	Always used in conjunction with Channel "A" for making ratio and tim interval measurements. It accepts up to 250V RMS or 300V peak on a ranges except 150V RMS or 200V peak to 1 MHz on 1V range withou damage.
	(3) C INPUT**	Used in the FREQ C mode only. It accepts frequencies from 1 MHz t 550 MHz and amplitudes from 50 mV to 1V. It accepts a maximum of 5V without damage. This input has no trigger controls because the slope always set for +; the coupling is always AC; the level is set at the 0 crossing and the attenuator is automatic.

Control	Position	Action
(4) FUNCTION (rotary switch)	REMOTE	This puts the FUNCTION switch, MULTIPLIER/TIME BASE control RESET and START/STOP switches, and the +/– slope switches unde remote digital programming control, regardless of what position they ar in at the time. The trigger level may be remotely programmed using a analog voltage. To do this, it is necessary for the trigger level control to b set at zero or for the attenuator to be in PRESET. The AC/DC couplin switch, the SEP/COM switch and the attenuator cannot be programmed
	CHECK	In this mode, the counter measures its internal 10 MHz reference. Th rear panel scaled output provides a TTL squarewave with a frequenc equal to 10 MHz divided by the multiplier setting.
	PERIOD	In this mode, the amount of time for one period of the input waveform measured.
	PER. AVG.	In this mode, a number of input waveform periods are averaged and mea ured. The number of periods is determined by the multiplier contro
	FREQ A	In this mode, the frequency on the A channel input is measured
	FREQ C**	In this mode, the frequency on the C channel input is measured
	TOTALIZE	In this mode, the number of events occurring between the start and sto command is totaled.
	T.I.*	In this mode, the time interval between two electrical events is measured The start point is determined by the A trigger controls and the stop poin by the B trigger controls.
	A/B	In this mode, the ratio of the frequency applied at the A input to the fre quency applied at the B input is measured.
	T.I. AVG.*	In this mode, the time interval between two repetitive electrical events ca be averaged and measured. The number of time intervals measured determined by the multiplier control.
INPUT CONTROLS		The purpose of the controls is to set the point on the incoming waveform that causes a trigger pulse to be sent to the counting logic. In the frequenc mode, it is necessary to send one trigger pulse during each cycle of the in put signal; the number of such trigger pulses received during a gate tim determines the frequency measured.

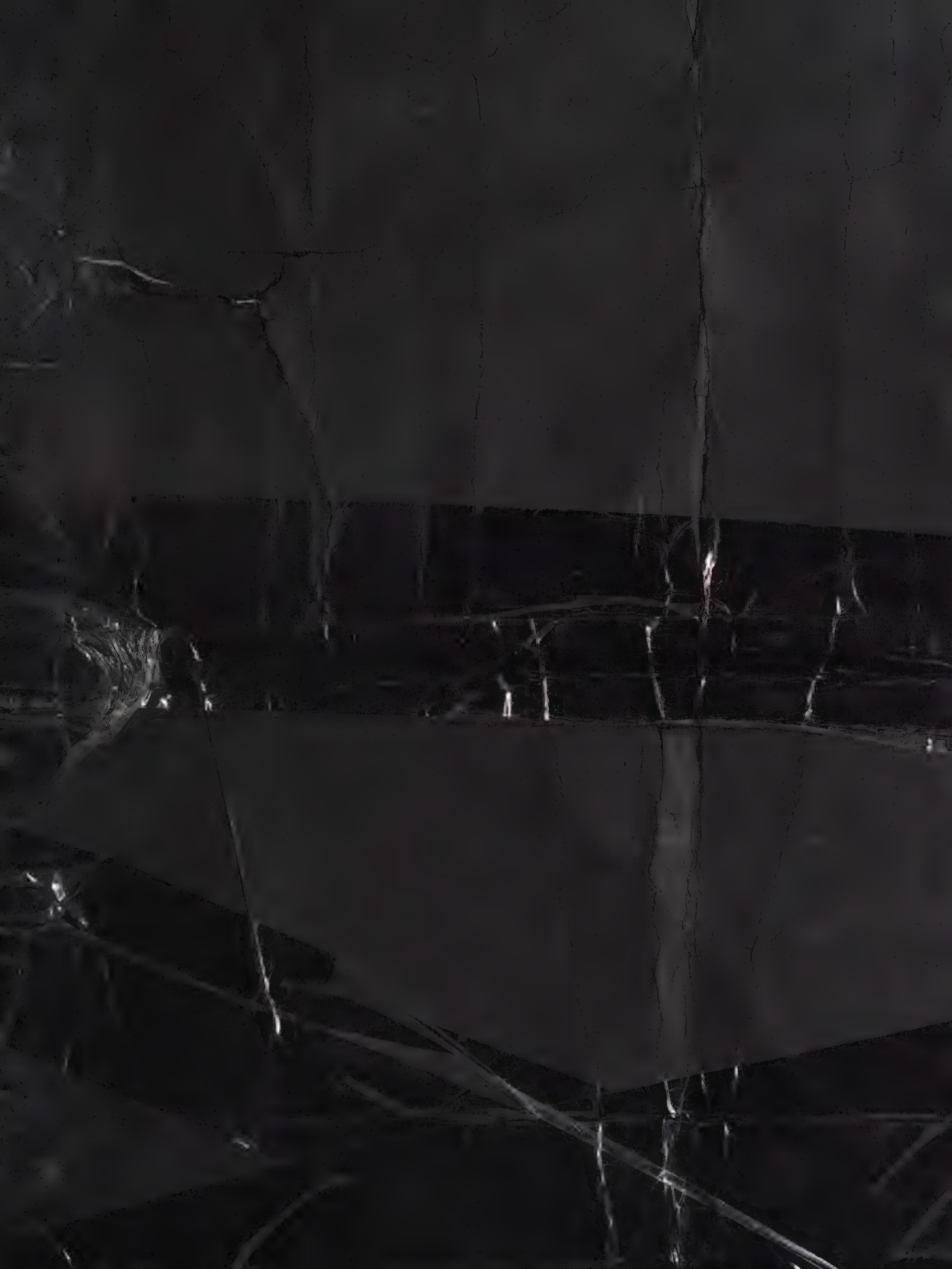
*Not in 8020B
**Not in 8010B

Table 2.1 - Controls and Connectors (Continued)

Control	Position	Action
(5) Trigger Range (outer switch)	1	Couples the input signal conditioner directly. Maximum usable signal is ±3 volts peak.
	10	Attenuates the input voltage by ten or 20 dB. Maximum usable signal is ±30 volts peak.
	100	Attenuates the input signal by one hundred or 40 dB. Maximum usable signal is ±300 volts peak.
		The trigger range also adjusts a special circuit that is designed to prevent false counts due to noise superimposed on the waveform being measured. This special circuit is called the trigger hysteresis. When the trigger range is in the 100V range it prevents all false counts due to superimposed noise of amplitude up to 2.5 volts peak to peak. In the 10V range, the protection is 250 mV; in the 1V range, it is 25 mV. It is therefore most desirable to have the range control set to the highest range possible for any given measurement – the higher the range, the greater the hysteresis protection.
(6) Trigger Level (inner control)		The level control provides continuous adjustment of the trigger amplitude from –300% of the trigger range setting to +300%. (If the trigger range control is set on the 10V range, for example, the trigger level control can be adjusted to cause triggering between –30V and +30V.)
	PRESET	When making frequency measurements, the waveform being measured is usually a low amplitude sinewave. Because this waveform is so widely encountered, a PRESET position has been included at which the counter triggers at a point ≤ ±5% of range.
(7) +/– Slope (slide switch)		Selects which slope of the incoming waveform is to trigger the counter (positive or negative).
	"+"	Causes triggering on the positive-going slope.
	"–"	Causes triggering on the negative-going slope.
(8) AC/DC Coupling (slide switch)	DC	Couples the input signal directly to the signal conditioner. Signal conditioner responds to dc signal changes. Used for time interval measurements.
	AC	Couples the input signal via a capacitor. Signal conditioner responds to periodic AC waveforms. Used for Frequency, Period, and Period AC measurements.
(9) COM/SEP (Not in 8020B)	COM	(Common.) Directs the input signal from input A to channel A and channel B. Used for time interval and multiple time interval average measurements.
	SEP	(Separate.) Connects channel A to channel A input and connects channel B to channel B input.

Table 2.1 - Controls and Connectors (Continued)

Control	Position	Action
(10) DISPLAY TIME (rotary control with switch)	PWR OFF	(Power off.) Turns off the output of the +5 volt, and ±18 volt regulators. Turns off the +150 volts to the display tubes.
	DISPLAY TIME	Applies power to all circuits. Provides a 30 ms (CCW) to 5 second (CW) display time interval between measurements.
	HOLD	Programs the counter to take one measurement. Displays and stores that measurement until RESET is depressed or the position of the DISPLAY TIME control is changed.
(11) START/STOP (momentary pushbutton switch)	Depressed momentarily	This switch is used in the totalize mode. When pushed the first time, the counter starts counting; pushed the second time, the counter stops counting and holds the reading.
(12) RESET	Depressed momentarily	Resets the digital counter to all zeros, arms the counter for a new reading. Commands a new reading anytime.
(13) MULTIPLIER/TIME-BASE Switches (pushbutton switches)	Top row of numbers: 1 10 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9	In Period Average and Time Interval Average modes, the numbers represent the multiplier. This indicates the number of periods or time intervals over which the measurement will be averaged. The higher the multiple, the greater the resolution and the slower the measurement time. In Frequency Ratio mode (A/B), the numbers indicate the number of cycles of the channel B (denominator) signals used to make the ratio measurement. The greater the number of cycles, the greater the resolution and the slower the measurement time.
	Lower row of numbers: 1 μs 10 μs 100 μs 1 ms 10 ms 100 ms 1s 10s 100s	In Frequency mode, the numbers select the time base control. This controls the time the internal gate is open. The longer the gate is open, the greater the resolution, and the slower the measurement time. In Period and Time Interval modes, the numbers indicate the reference frequency to be counted during the gate time. The shorter the time base selected, the greater the resolution; therefore, the left most button is usually selected for these operating modes.



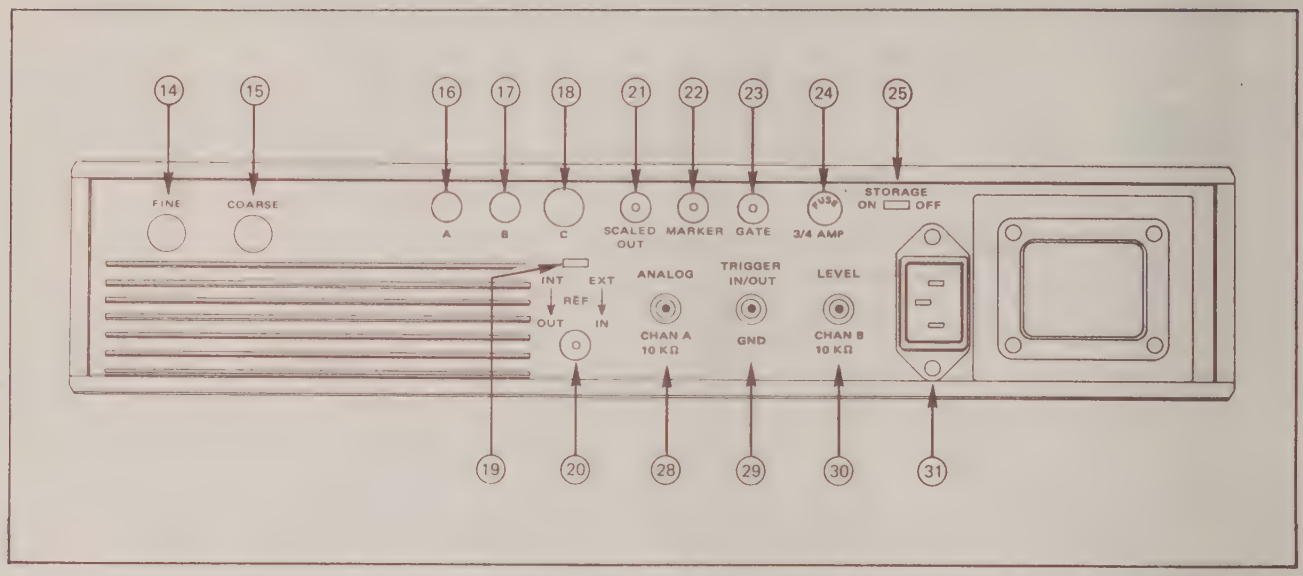


Figure 2.4 - Rear Panel

Table 2.1 - Controls and Connectors (Continued)

REAR PANEL (see figure 2.4)

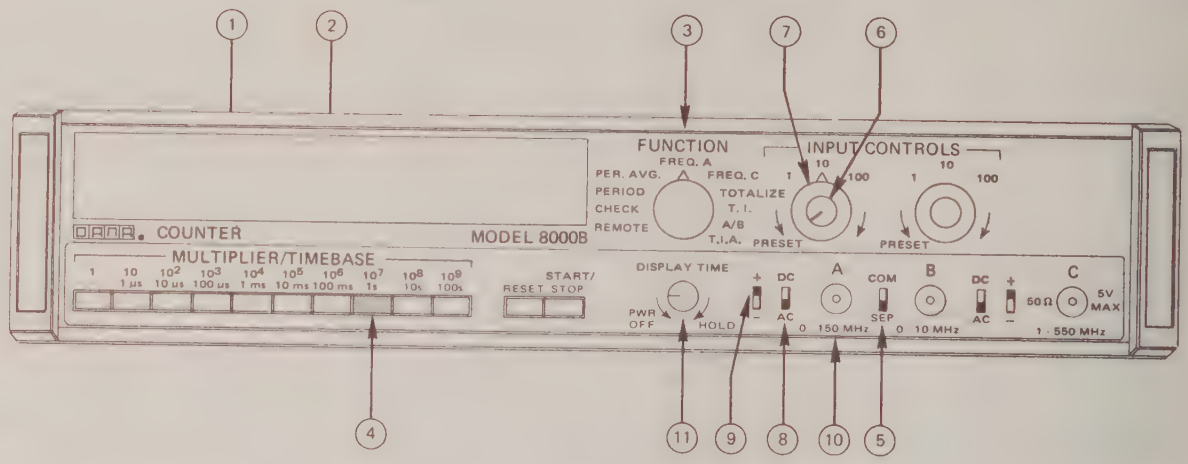
(14) FINE		Access hole used in the FINE adjustment of the ovenized oscillator Option 200. See Calibration.
(15) COARSE		Access hole used in the COARSE adjustment of the ovenized oscillator Option 200. See Calibration.
(16) "A" (BNC connector)		Provides rear input for channel A. Used in Option 010 rear input. Degrades sensitivity by 10 dB above 50 MHz.
(17) "B"*** (BNC connector)		Provides rear input for channel B. Used in Option 010 rear input.
(18) "C"** (BNC connector)		Provides rear input for channel C. Used with Option 010 rear input.
(19) INT/EXT REF. (slide switch)	INT (Internal)	Routes the internal reference oscillator to the reference filter and to the reference BNC connector.
	EXT (External)	Routes the external reference oscillator from the reference BNC connector to the reference filter circuit.
(20) REF (BNC connector)		Used as internal reference oscillator output when the REF switch is in INT position. Used as external input to reference filter when switch is in EXT position. The counter will accept 1, 5, and 10 MHz external reference.
(21) SCALED OUT (BNC connector)		Provides a SCALED OUTput of the input in Totalize mode.
(22) MARKER OUT (BNC connector)		Provides a negative 18 volt output starting with trigger A and ending with trigger B. Used to modulate the Z axis of an oscilloscope.
(23) GATE (BNC connector)		Provides a positive true GATE output capable of driving five TTL loads.
(24) FUSE		Provided for the protection of internal circuits in the counter. Located on the rear panel. 3 AG, 3/4 AMP.
(25) STORAGE (slide switch)	OFF	Allows the counter to continuously update the display. Automatically off in the Totalize mode.
	ON	Allows the counter to store information and periodically updates the display.
(28) ANALOG, CHAN A		Used to measure or program a trigger level to channel A.
(29) TRIGGER IN/OUT GND		Used as a ground return for channel A and B trigger level input and output.
(30) ANALOG, CHAN B*		Used to measure or program a trigger level to channel B.
(31) Power Connector		A three pin connector used for power input. Third pin is power ground.

*Not used in 8020B

**Not in 8010B

***Not in 8020B

Table 2.2 - Frequency Measurement 0 - 150 MHz

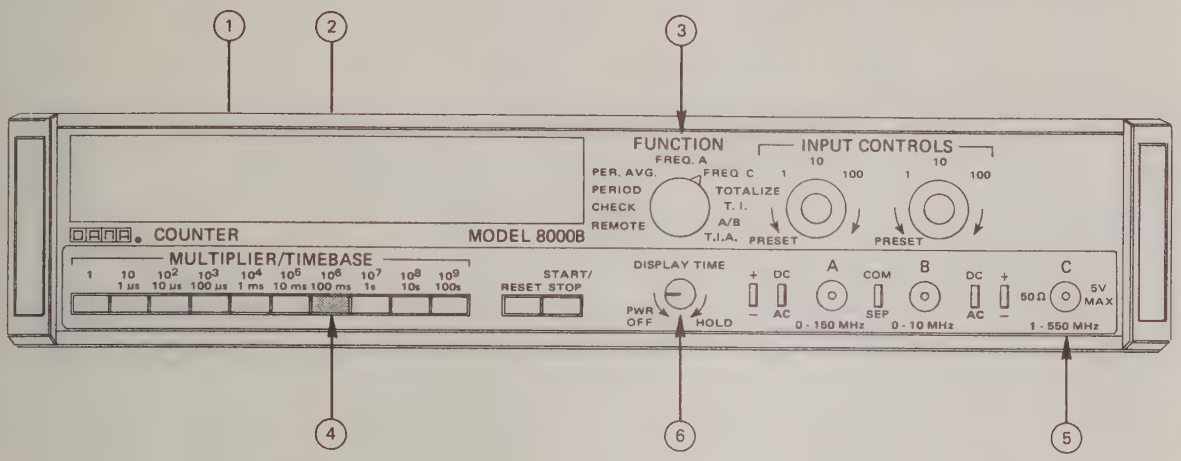


1. Connect AC power.
2. Set STORAGE switch to the ON position.
3. Set the FUNCTION switch to FREQUENCY A.
4. Set the TIMEBASE switch to desired gate time.
5. Set the SEP/COM to SEP.
6. Set channel A level control to desired trigger level or to PRESET to trigger at ≅(0) zero volts.
7. Set INPUT CONTROL range switch to be compatible with the input signal amplitude (1, 10 or 100 volt range).
8. Set AC/DC coupling to AC or DC.
9. Set the A slope to (+) plus.
10. Connect input signal (0 to 150 MHz) to channel A input jack. Note: Max. input 250V RMS or 300V peak.
11. Set DISPLAY TIME to a convenient display interval.

Example: Input frequency to be measured is 600 hertz at 8 volts peak to peak. The TIMEBASE is set to 1 second. Input voltage range is set to 10 volts, trigger level to PRESET, slope to plus and AC/DC to AC. Display will be .000600 MHz with 1 hertz resolution. Change the TIMEBASE to 10 second, the display will be .6000 kHz with 0.1 hertz resolution. Change the TIMEBASE to 100 sec and the display will be .60000 kHz with 0.01 hertz resoltuion.

NOTE: A much faster reading would be to use the PERIOD mode and measure the period of the frequency.

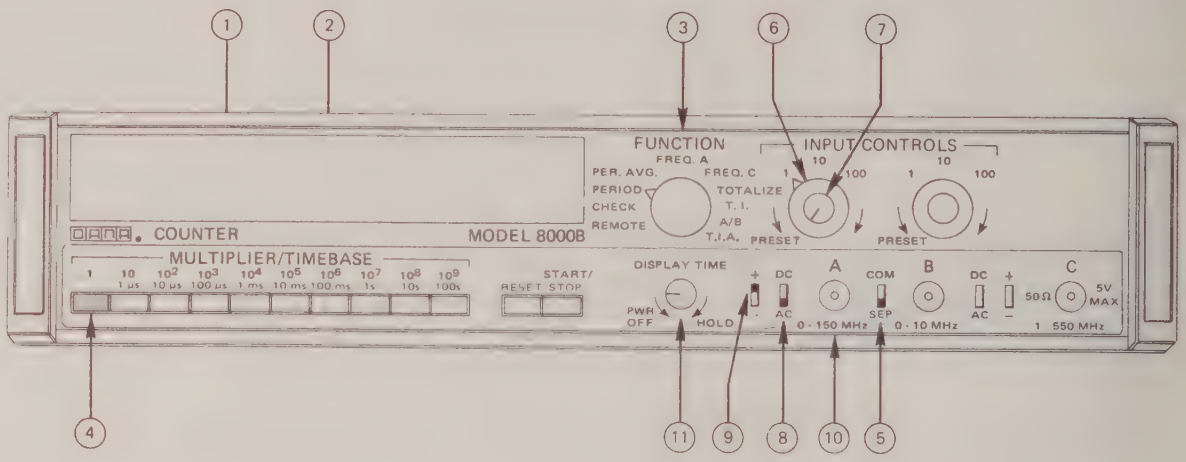
Table 2.3 - Frequency Measurement 1 - 550 MHz (Not in 8010B)



1. Connect AC power.
2. Set STORAGE switch to the ON position.
3. Set the FUNCTION switch to FREQUENCY C.
4. Set the TIMEBASE switch to the desired gate time.
5. Connect the input signal from 1 to 550 MHz (10 to 500 MHz with Option 030) in frequency to channel C input. Note: Max. input operating input is 1V RMS. Max. input without damage is 5V RMS.
6. Set DISPLAY TIME to a convenient display interval.

Example: Input frequency to be measured is 200 MHz at .5V rms. The TIMEBASE is set to 100 milliseconds. The trigger level setting is automatic in the FREQUENCY C function. The display will be 200.00000 MHz with 10 hertz resolution. Gate time is expanded by 4 in this mode of operation (i.e., a 100 ms gate selected on front panel will actually be 400 milliseconds).

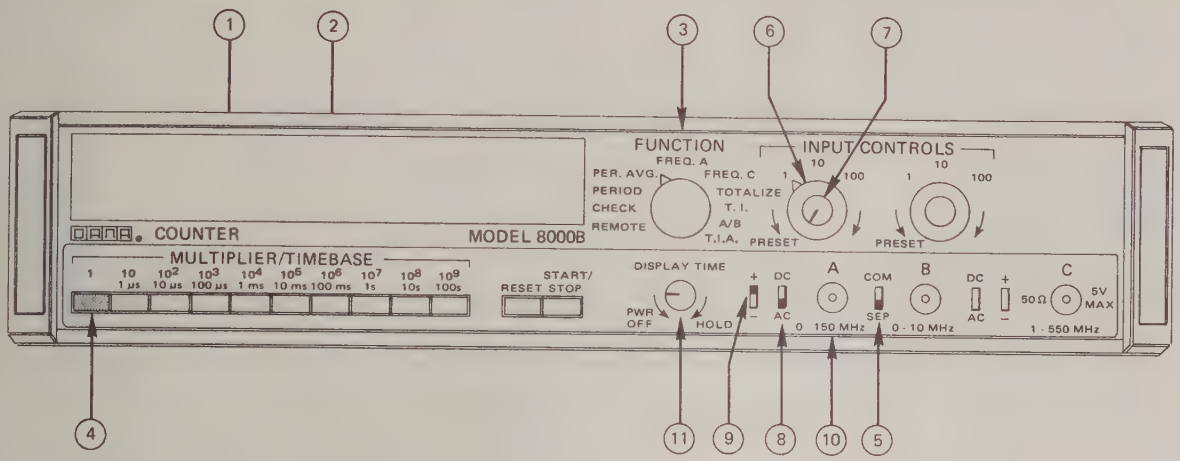
Table 2.4 - Period Measurements



1. Connect AC power.
2. Set STORAGE switch to the ON position.
3. Set the FUNCTION switch to PERIOD.
4. Set the TIMEBASE switch to the desired time units to be counted.
5. Set the SEP/COM to SEP.
6. Set the channel A INPUT CONTROL range switch to be compatible with the input signal amplitude.
7. Set the channel A trigger level control to the desired trigger level or to PRESET to trigger at ≅(0) zero volts.
8. Set the AC/DC coupling to AC or DC on channel A.
9. Set the A slope to (+) plus or (–) minus.
10. Connect the input signal (0 to 10 MHz) to channel A input jack.
11. Set DISPLAY TIME to a convenient display interval.

Example: Input PERIOD to be measured is 1 millisecond at 1V peak. The TIMEBASE is set to 1. The channel A INPUT CONTROL switch is set to the 1-volt range, trigger level is set to the PRESET position and AC/DC is set to AC. The display will be 0001000.0 microseconds with 100 nanoseconds resolution.

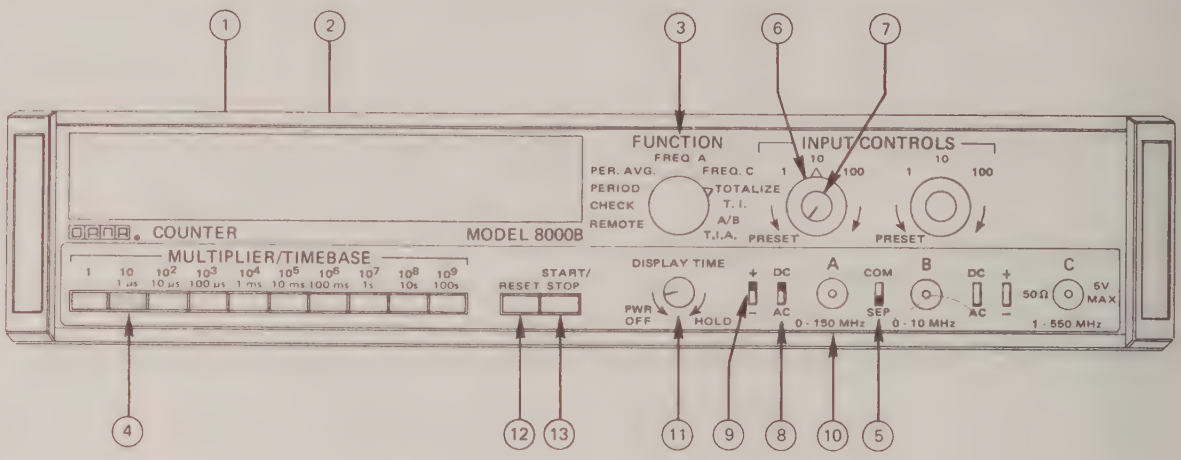
Table 2.5 - Period Average Measurements



1. Connect the AC power.
2. Set the STORAGE switch to the ON position.
3. Set the FUNCTION switch to PERIOD AVERAGE.
4. Set the MULTIPLIER switch to the desired time multiplier position.
5. Set the SEP/COM switch to SEP.
6. Set the channel A INPUT CONTROL range switch to match the input signal amplitude.
7. Set the channel A level control to the desired trigger level or to PRESET to trigger at ≡(0) zero volts.
8. Set the AC/DC coupling to AC or DC on channel A.
9. Set the channel A slope to (+) or (–) minus.
10. Connect the input signal (0 to 10 MHz) to channel A input jack.
11. Set DISPLAY TIME to a convenient display interval.

Example: Input period to be measured is 1 millisecond at 1V peak. The TIME BASE is set to 1. The channel A input voltage range switch is set to the 1 volt range, the trigger level is set to the PRESET position and AC/DC is set to AC. The display is 0001.0000 milliseconds with 100 nanoseconds resolution. Depress the 10 multiplier switch. The display will be 001.00000 ms with 10 nanosecond resolution.

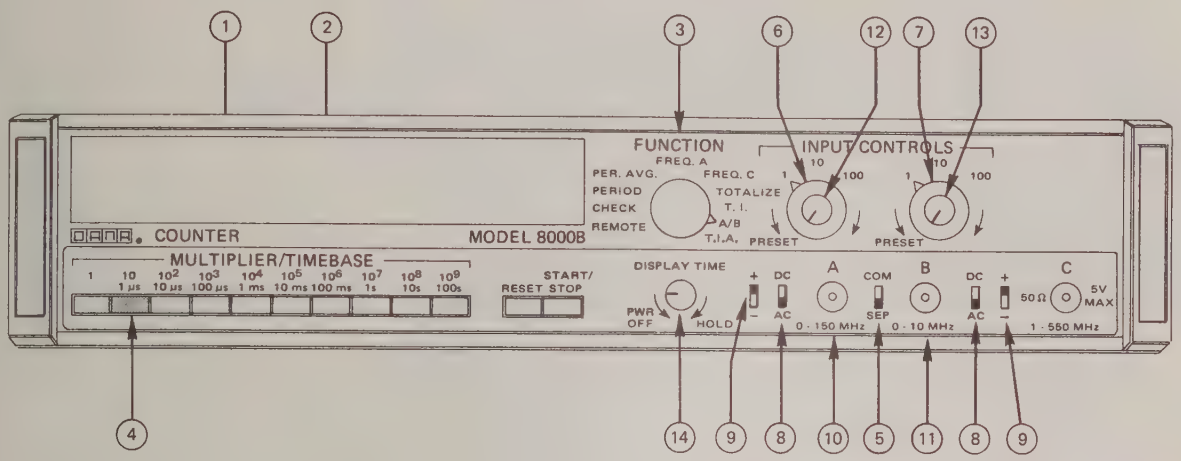
Table 2.6 - Totalize



1. Connect the AC power.
2. Set the STORAGE switch to the ON position. Note: storage automatically disabled.
3. Set the FUNCTION switch to the TOTALIZE position.
4. Set the MULTIPLIER switch for the scaled output desired.
5. Set the SEP/COM switch to the SEP position.
6. Set the channel A INPUT CONTROL range switch to match the input signal amplitude.
7. Set the channel A level control to the desired trigger level or to PRESET to trigger at ≅ (0) zero volts.
8. Set the AC/DC coupling to AC or DC on channel A.
9. Set the channel A slope to (+) plus or (–) minus.
10. Connect the input signal (0 to 150 MHz) to channel A input jack.
11. Turn DISPLAY TIME clockwise to any position. It is not operative in this mode.
12. Depress the RESET switch.
13. To start the count, depress the START/STOP momentary switch. To stop the count, depress the START/STOP switch again.

Example: A series of electrical events is to be counted. They are 10V peak in amplitude and have a rate of 10 kHz. A scaled output is needed at 10 Hz. Set the channel A input voltage range switch to the 10V range, the trigger level to PRESET position, and the AC/DC to AC. The MULTIPLIER switch is set to 10. The count is initiated by depressing the START button. The SCALED OUT will be 10 Hz.

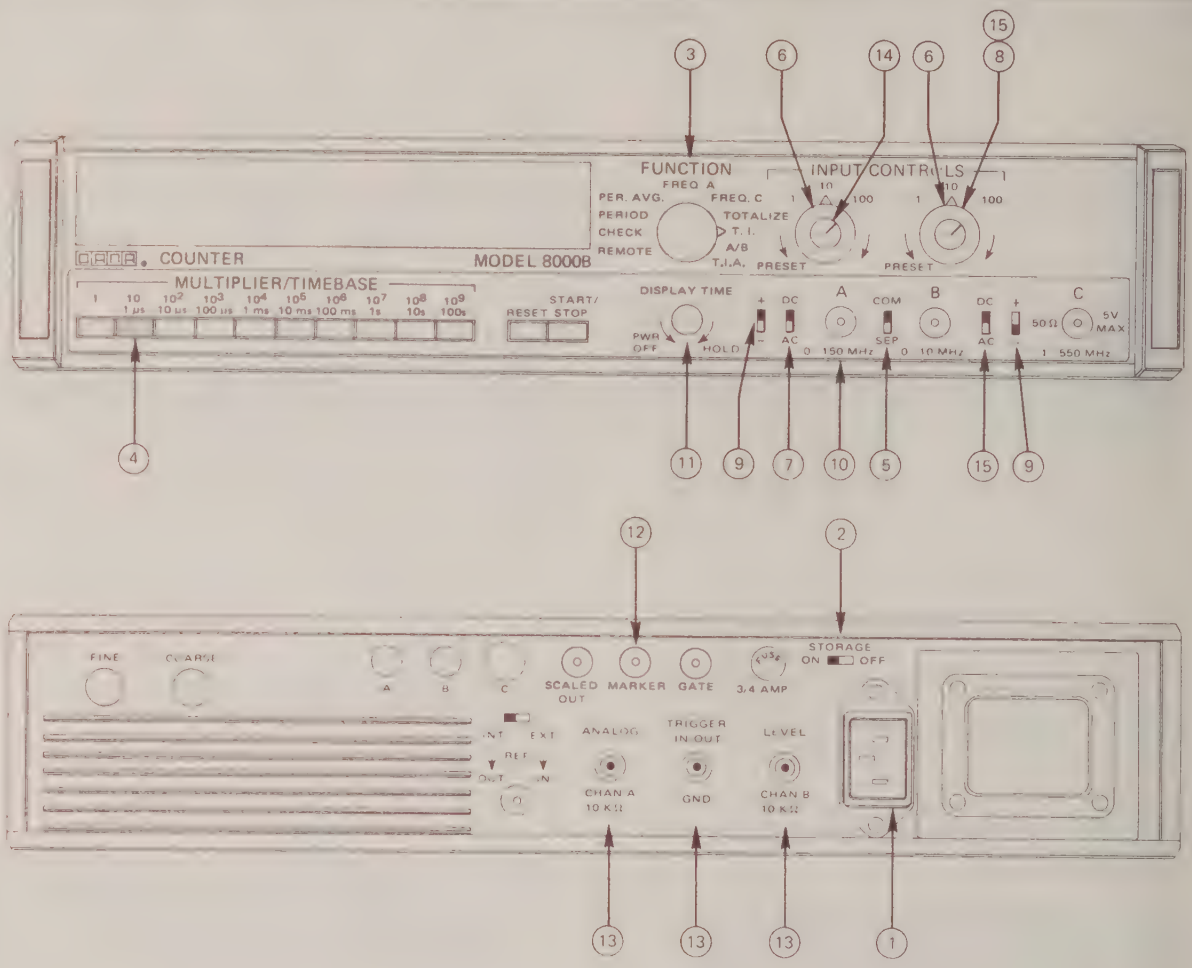
Table 2.7 - A/B Ratio



1. Connect the AC power at the rear panel.
2. Set the STORAGE switch to the ON position.
3. Set the FUNCTION switch to the A/B position.
4. Set the MULTIPLIER switch for the multiplier desired.
5. Set the SEP/COM switch to the SEP position.
6. Set the channel A INPUT CONTROL range switch to match the input signal amplitude.
7. Set the channel B INPUT CONTROL range switch to match the input signal amplitude.
8. Set channel A and B coupling to AC or DC.
9. Set channel A and B slope to (+) plus or (–) minus.
10. Connect the higher frequency input (0 - 150 MHz) to channel A.
11. Connect the lower frequency input (0 - 10 MHz) to channel B.
12. Set the channel A trigger level control to the desired trigger level or to the PRESET to trigger at ≅(0) zero volts.
13. Set the channel B trigger level control to the desired trigger level or to PRESET to trigger at ≃(0) zero volts.
14. Set DISPLAY TIME to a convenient display interval.

Example: The ratio of two frequencies, 100 kHz and 1 kHz, are to be measured. The 100 kHz signal is applied to channel A. The 1 kHz signal is applied to channel B. The 1 MULTIPLIER is depressed. The SEP/COM is set to the SEP position. Both A and B trigger levels are set to PRESET position. The display indicates ratio directly. Ratio equals frequency A divided by frequency B times the multiplier. The display is 00000100. Depress the 10 multiplier. The display is 00001000. Depress the 10^2 multiplier. The display is 00010000.

Table 2.8 - Time Interval (Not in 8020B)



1. Connect the AC power.
2. Set the STORAGE switch to the ON position.
3. Set the FUNCTION switch to the TIME INTERVAL position.
4. Set the TIMEBASE switch to the desired TIME BASE position.
5. Set the SEP/COM switch to the COM position.
6. Set the channel A and B INPUT CONTROL range switch to be compatible with the input signal amplitude.
7. Set channel A AC/DC coupling switch to desired setting.
8. Set channel B AC/DC coupling switch to AC and trigger level to PRESET.
9. Set +/-- slope switches to desired setting.
10. Connect input signal (0 to 10 MHz) to channel A input.
11. Set DISPLAY TIME to a convenient display interval.
12. To use the MARKER of the counter, tee-off the input signal of channel A input and connect to vertical input of oscilloscope. Connect MARKER output of counter to Z axis of oscilloscope.

continued

Table 2.8 - Time Interval (continued)

(*13) Connect two DC voltmeters capable of reading ±30 VDC to the ANALOG TRIGGER LEVEL outputs. Use the following formula to determine the trigger level voltage.

$$TL = \frac{VR}{10}$$

Where: TL = trigger level
V = voltmeter reading
R = Input control range

Example: The meter reading is 5 volts on the Input Control range 1.

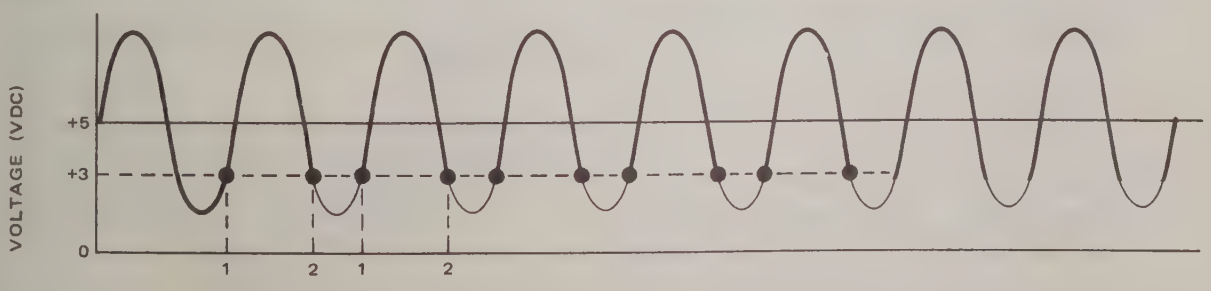
$$TL = \frac{5\,(1)}{10} = .5 \text{ volts}$$

(14) Adjust channel A trigger level control to desired "start" trigger voltage.

(15) Set channel B AC/DC to desired setting and adjust trigger level to desired "stop" trigger voltage.

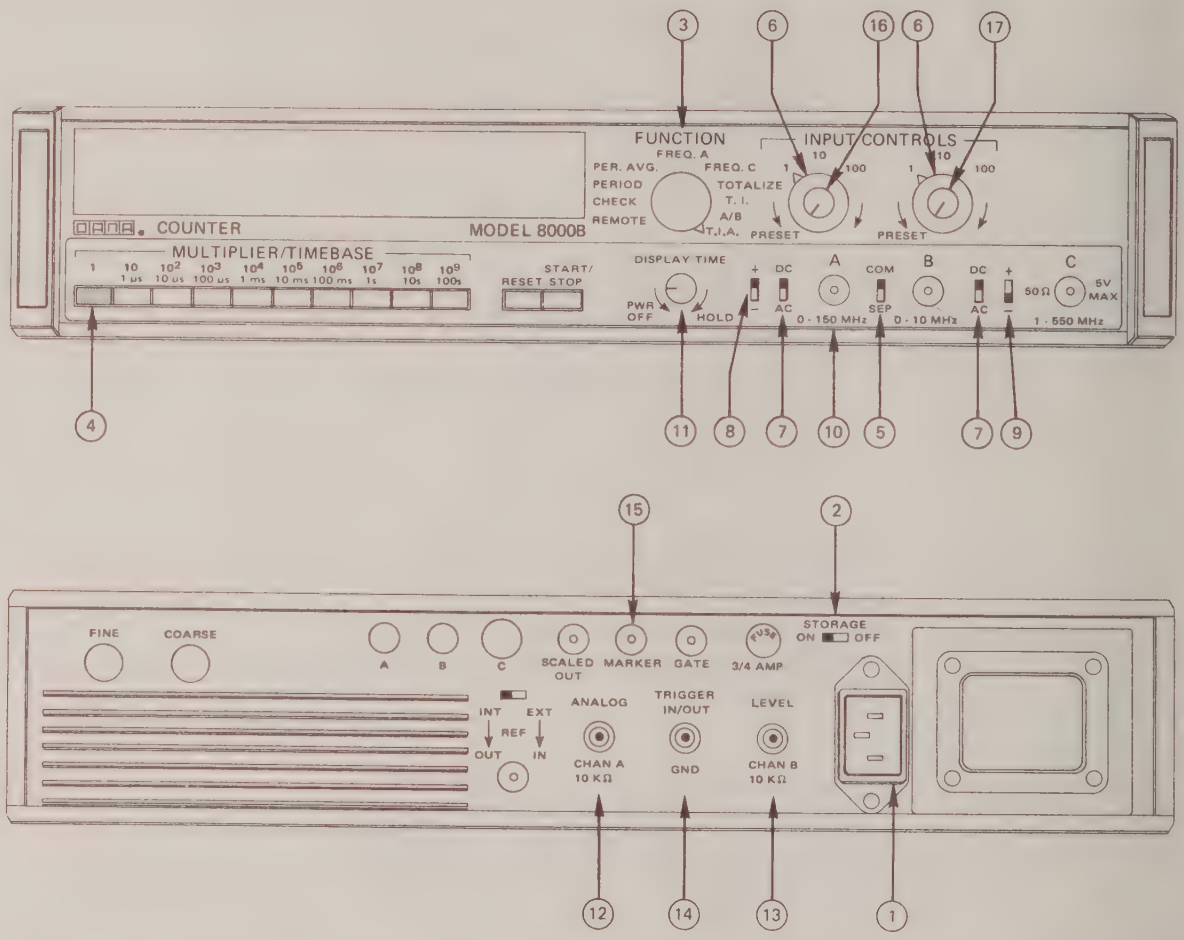
*Two features are provided in the 8000B counters to aid in setting the front panel controls. These features are the MARKER and the trigger level voltage connectors located on the rear panel. The use of these features is optional.

Example: The input waveform is a 1 kHz 5V peak to peak waveform riding on a 5 volt DC voltage. It is desired to measure the portion of the PERIOD which exist above 3 volts. See figure. Set the TIMEBASE to 1 μsec. Set the SEP/COM to COM. Set the channel A and B input voltage range to 10 volts. Set the A and B coupling to DC. Set the channel A slope to plus and channel B slope to (−) minus. Connect the voltmeters and oscilloscope to the counter as before. Adjust the A trigger level to trigger at 3 VDC on the plus slope. Adjust the B trigger level to trigger at 3 VDC on the minus slope. The period that is measured is intensified on the oscilloscope. The display is 0000746.0 μsec.



1. A TRIGGER LEVEL + SLOPE
2. B TRIGGER LEVEL − SLOPE

Table 2.9 - Time Interval Average (Not in 8020B)



1. Connect the AC power.
2. Set the STORAGE switch to the ON position.
3. Set the FUNCTION switch to the TIME INTERVAL AVERAGE position.
4. Set the MULTIPLIER switch to the desired multiplier position.
5. Set the SEP/COM switch to the COM position.
6. Set the channel A and B INPUT CONTROL range switch to be compatible with the input signal amplitude.
7. Set channel A AC/DC coupling switch to desired setting.
8. Set channel B AC/DC coupling switch to AC and trigger level to PRESET.
9. Set +/– slope switches to desired setting.
10. Connect the input signal (0 to 2.5 MHz) to channel A input.
11. Set DISPLAY TIME to a convenient display interval.
- *12. To use the MARKER of the counter, tee-off the input signal of channel A input and connect to vertical input of oscilloscope. Connect MARKER output of counter to Z axis of oscilloscope.

continued

Table 2.9 - Time Interval Average (continued)

(*13) Connect two DC voltmeters capable of reading ±30 VDC to the ANALOG TRIGGER LEVEL outputs. Use the following formula to determine the trigger level voltage.

$$TL = \frac{VR}{10}$$

Where: TL = trigger level
V = voltmeter reading
R = Input control range

Example: The meter reading is 5 volts on the Input Control range 1.

$$TL = \frac{5\,(1)}{10} = .5 \text{ volts}$$

(14) Adjust channel A trigger level control to desired "start" trigger voltage.

(15) Set channel B AC/DC to desired setting and adjust trigger level to desired "stop" trigger voltage.

*Two features are provided in the 8000B counters to aid in setting the front panel controls. These features are the MARKER and the trigger level voltage connectors located on the rear panel. The use of these features is optional.

Example: It is desired to measure the positive pulse width of a 5 kHz square wave. Set the MULTIPLIER to 1. Set the SEP/COM to COM. Set the A and B coupling to DC. Set the A slope to (+) plus and the B slope to (–) minus. Set the A and B trigger levels to PRESET. The display is 0000100.0 μsec. The resolution is 100 ns. Depress the MULTIPLIER 10 and the display is 000100.00 μsec. The resolution is 10 ns.

NOTE: In time interval average mode, the input signals must be repetitive and asynchronous with the counter's reference oscillator (10 MHz). If the input signal approaches a sub-harmonic of the reference frequency, a greater number of time intervals will have to be averaged to achieve good accuracy. The accuracy is found by the following formula.

$$\pm\text{reference error} \pm 2 \text{ nsec} \pm \frac{(\text{trigger error} \pm 100 \text{ nsec})}{\sqrt{\text{Number of Intervals Averaged}}}$$

where: $\text{trigger error} = \dfrac{.0025\ \mu\text{sec}}{\text{signal slope (V/}\mu\text{sec)}}$

SECTION 3 PERFORMANCE CHECK

3.1 INTRODUCTION.

3.2 This procedure is designed to insure that the instrument is operating properly and within its specifications. If any of the readings are not within tolerance, refer to the calibration procedure. If the instrument fails to operate properly, refer to the troubleshooting procedure.

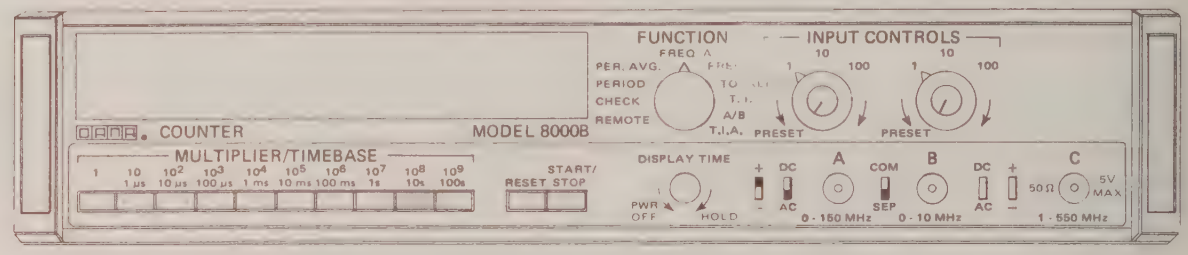
3.3 RECOMMENDED TEST EQUIPMENT.

3.4 Test equipment recommended for the Performance check is listed in table 3.1. Procedures are described in tables 3.2 through 3.11.

Table 3.1 - Required Equipment

Instrument Type	Required Specification	Recommended Instruments
Frequency Standard	1 MHz, 5 MHz, or 10 MHz	
Oscilloscope	150 MHz Bandwidth	TEK 454
Voltmeter	10 mVDC to 200 VDC	Dana 4300
Sine Wave Generator	2 Hz – 10 MHz	Dana 7010
VHF Signal Generator	10 – 150 MHz	HP8654A
VHF Signal Generator	1 – 550 MHz (Not required for 8010B)	HP8654A
Alignment Tool	.075" Hex (nonmetallic)	General Cement 9300
Alignment Tool	Blade (nonmetallic)	
Sampling Voltmeter	0 – 600 MHz	HP3406
50Ω Feedthru		TEK 011-049
BNC "T" Connectors		
50Ω Tee Connector		HP1022A
2 – BNC to GR Adapters		

Table 3.2 - Reference Oscillator Stability



DISPLAY TIME: Power on/CCW position
FUNCTION Switch: FREQ A
TIME BASE: 10 sec
SLOPE A: (+) Plus
A COUPLING: AC
INPUT VOLTAGE RANGE: 1 Volt
TRIGGER LEVEL A: PRESET
SEP/COM Switch: SEP
STORAGE Switch: ON
REFERENCE Switch: INT

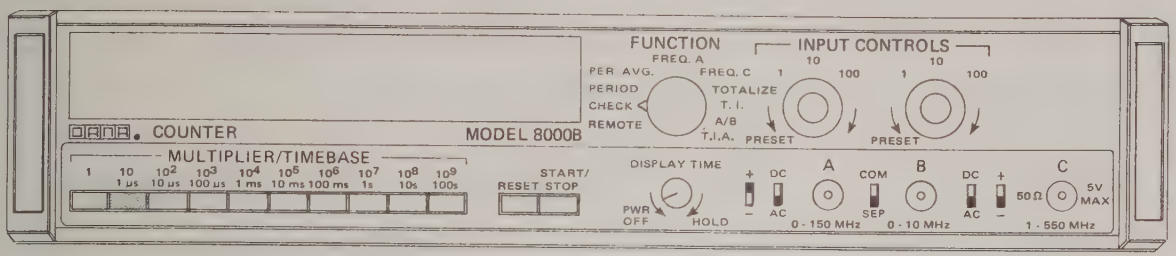
1. Set the controls as shown above.
2. Allow the counter to warmup for 1 hour, except with Option 200, which is 72 hours. Do not remove covers.
3. Connect a 1 MHz at 1V RMS Frequency Standard to Frequency Input A.
4. The difference between the Internal Counter Reference oscillator and the 1 MHz Frequency Standard can be determined by the following formula (20 000 000, – Reading in counts) = the Internal oscillator frequency in hertz.

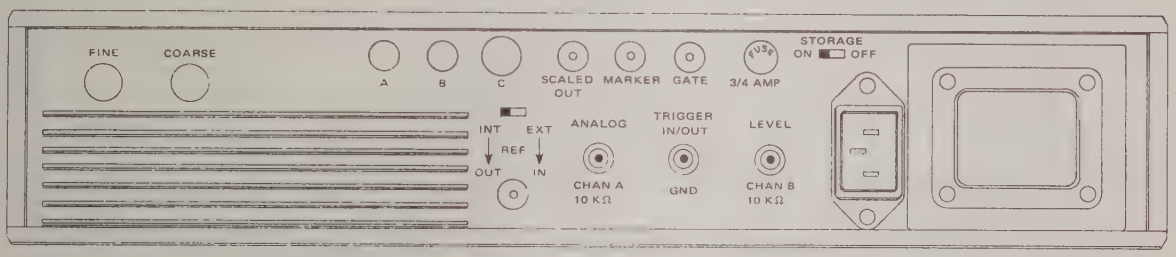
Typical Counter Reference Oscillator Difference for Standard Oscillator

Display	Internal Reference Oscillator
999.9950 kHz	10000.050 kHz
999.9975	10000. 025
1000.0000	10000.000
1000.0025	9999.975
1000.0050	9999.950

5. To calibrate the counter to a Frequency Standard, refer to the Calibration section.
6. To determine long term stability, operate the counter continuously for at least 1 month. The stability is as follows: Standard Oscillator, $< 3 \times 10^{-7}$ per month, Option 050 1×10^{-7} per month, Option 200 1×10^{-9} per day.
7. To measure line voltage stability, use a Variac to vary the line voltage $\pm 10\%$ and measure the frequency difference. The line stability is as follows: Standard Oscillator $\pm 1 \times 10^{-7}$, Option 050 $\pm 5 \times 10^{-8}$, Option 200 $\pm 2 \times 10^{-9}$.
8. To measure temperature stability, vary the temperature from 25°C to 0°. Allow the reading to stabilize and note the reading. Increase the temperature to 50°C and allow the reading to stabilize. The temperature stability 0° to 50°C is as follows: Standard Oscillator $\pm 2.5 \times 10^{-6}$, Option 050 $\pm 5 \times 10^{-7}$, and Option 200 $\pm 5 \times 10^{-9}$.
9. Check the Reference Oscillator output by connecting an oscilloscope to the REF. OUT jack on the rear of the counter. An output of >2.0V peak to peak at 10 MHz is normal.

Table 3.3 - Counting Decades and Multiplier/Timebase Decades





DISPLAY TIME: Power on/CCW position

FUNCTION Switch: CHECK

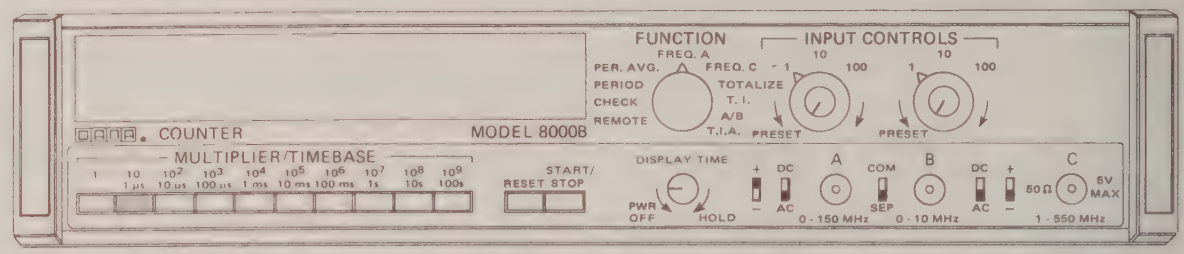
TIME BASE: See chart

STORAGE Switch: ON

REFERENCE Switch: INT

Timebase	Display	Tolerance
1 µs	000000010	± 1 count
10	000000100	± 1 count
100	000001000	± 1 count
1 ms	000010000	± 1 count
10	000100000	± 1 count
100	001000000	± 1 count
1 sec	010000000	± 1 count
10	100000000	± 1 count
100	000000000	± 1 count
9th digit option ——↵		

Table 3.4 - Decimal Point and Units



DISPLAY TIME: Power on/CCW position

FUNCTION Switch: Set for each check

TIME BASE: See table below

STORAGE Switch: ON

REFERENCE Switch: INT

Timebase	DISPLAY			
	FREQ A	Units	FREQ C (Not in 8010B)	Units
1 μsec	000000000	MHz	000000000	MHz
10	00000000.0	MHz	00000000.0	MHz
100	0000000.00	MHz	0000000.00	MHz
1 ms	000000.000	MHz	000000.000	MHz
10	00000.0000	MHz	00000.0000	MHz
100	0000.00000	MHz	0000.00000	MHz
1s	000.000000	MHz	000.000000	MHz
10	00000.0000	kHz	00.0000000	MHz
100	0000.00000	kHz	0.00000000	MHz
9th digit option				

PERIOD (All Models)
TIME INTERVAL (Not in 8020B)

Multiplier Selected	Display	Units
1	00000000.0	μsec
10	000000000	μsec
10^2	0000000.00	msec
10^3	00000000.0	msec
10^4	000000000	msec
10^5	0000000.00	sec
10^6	00000000.0	sec
10^7	000000000	sec
10^8	000000000	–
10^9	000000000	–
9th digit option		

continued

Table 3.4 - Decimal Point and Units (continued)

PERIOD AVERAGE (All Models)

Multiplier Selected	Display	Units
1	00000.0000	msec
10	0000.00000	msec
10^2	000.000000	msec
10^3	00000.0000	μsec
10^4	0000.00000	μsec
10^5	000.000000	μsec
10^6	00000.0000	nsec
10^7	0000.00000	nsec
10^8	000.000000	nsec
10^9	000000000	—
9th digit option ⟵		

TIME INTERVAL AVERAGE (Models 8010B, 8030B)

Multiplier Selected	Display	Units
1	00000000.0	μsec
10	0000000.00	μsec
10^2	000000000	nsec
10^3	00000000.0	nsec
10^4	0000000.00	nsec
10^5	000000.000	nsec
10^6	00000.0000	nsec
10^7	0000.00000	nsec
10^8	000.000000	nsec
10^9	00.0000000	nsec
9th digit option ⟵		

TOTALIZE
A/B RATIO

Verify that no annunciators except the gate are lit when any multiplier button is depressed.

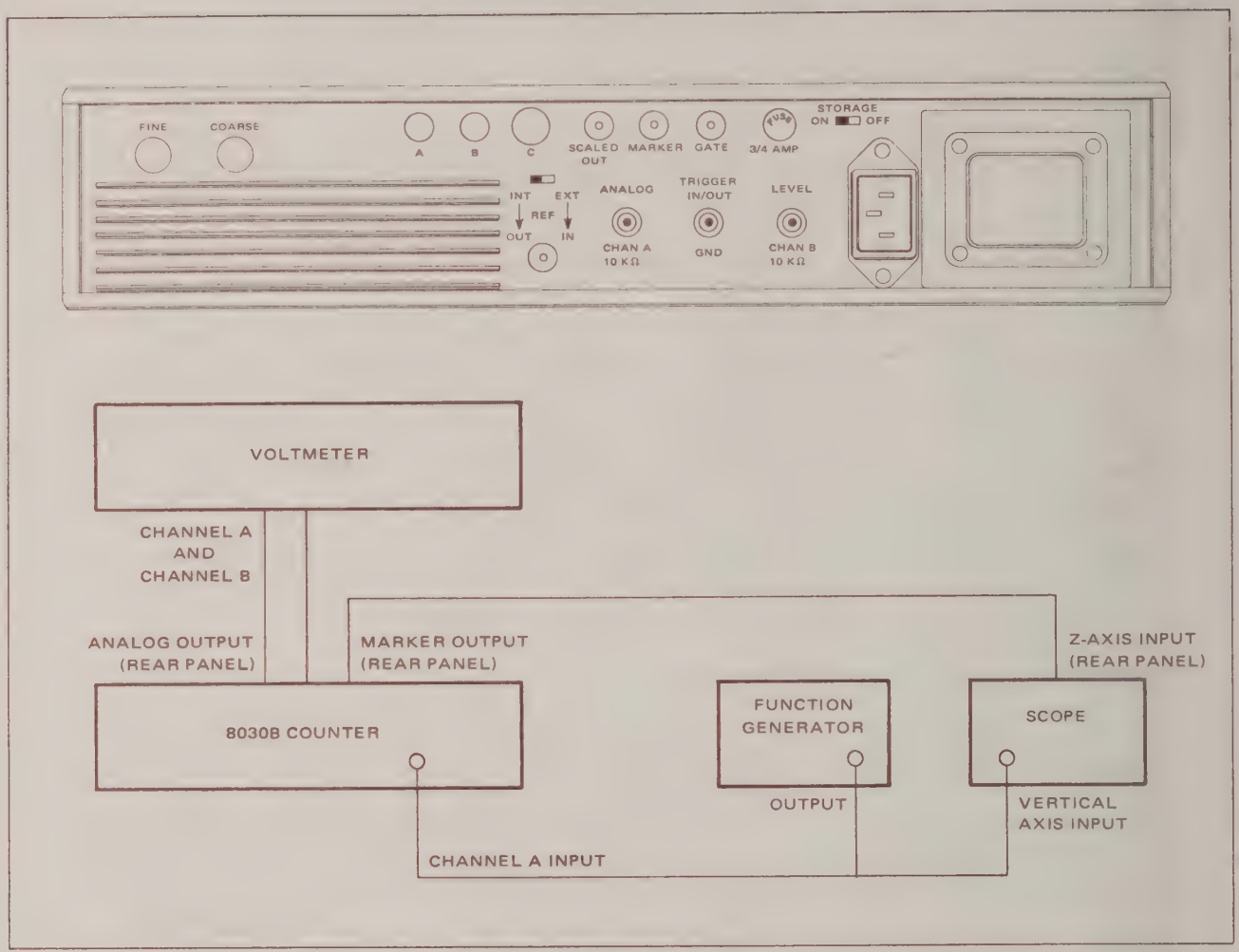
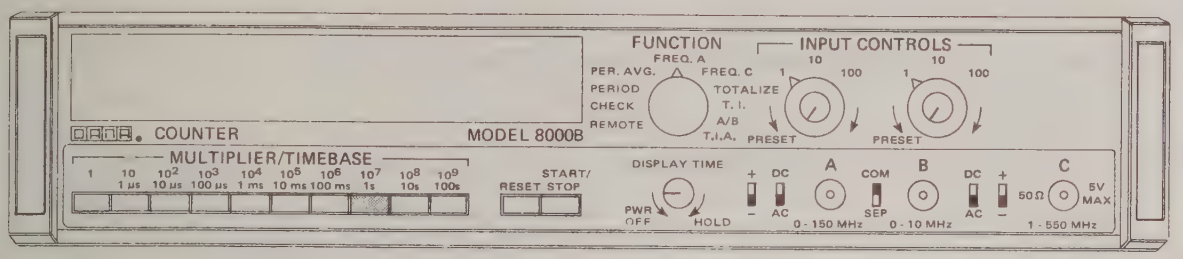


Figure 3.1 - Input Control and Marker Check Connections

Table 3.5 - Input Controls and Marker



DISPLAY TIME: Power on/CCW position
FUNCTION: FREQ A
TIME BASE: 1 second
SLOPE A: Minus (–)
SLOPE B: Minus (–)
COUPLING A: AC
STORAGE: ON (rear panel)

COUPLING B: AC
INPUT RANGE CONTROL A: 1
INPUT RANGE CONTROL B: 1
TRIGGER LEVEL A: PRESET
TRIGGER LEVEL B: PRESET
SEP/COM: COM

1. Set counter controls as shown above.

2. Connect Function Generator output to Input A on the counter. Also connect the Function Generator to the vertical input on an oscilloscope. Refer to figure 3.1 for all connections.

3. Adjust the Function Generator to 100 Hz at 4V peak to peak sine wave. Adjust the oscilloscope for a trace.

4. Connect voltmeter to the channel A Analog Output on the rear panel of the counter. For counters with Option 008, Systems Interface, connect to J110-S and J110-15.

5. Verify that the marker initiation is ±50 mVDC on the negative slope. Vary the channel A trigger level control and verify the marker initiation is variable over +3 volts to –3 volts on the negative slope of the sine wave.

6. Return channel A trigger level to the Preset position. Change channel A slope to (+) plus. Verify that the marker initiation is ±50 mVDC on the positive slope. Vary channel A trigger level control and verify the marker initiation is variable over +3 volts to –3 volts on the positive slope of the sine wave on the oscilloscope.

7. Return the channel A trigger level to Preset and the channel A slope to (–) minus.

8. Connect a voltmeter to the channel B Analog Output on the rear panel of the counter. For counters with Systems Interface, connect to J110-N and J110-15.

9. Verify that the marker termination is ±50 mVDC on the negative slope. Vary the channel B trigger level control and verify that the marker termination is variable over +3 volts to –3 volts on the negative slope of the sine wave.

10. Return channel B trigger level to Preset position. Change channel B slope to (+) plus. Verify that the marker termination is ±50 mVDC on the positive slope. Vary channel B trigger level control and verify the marker initiation is variable over +3 volts to –3 volts on the positive slope of the sine wave on the oscilloscope.

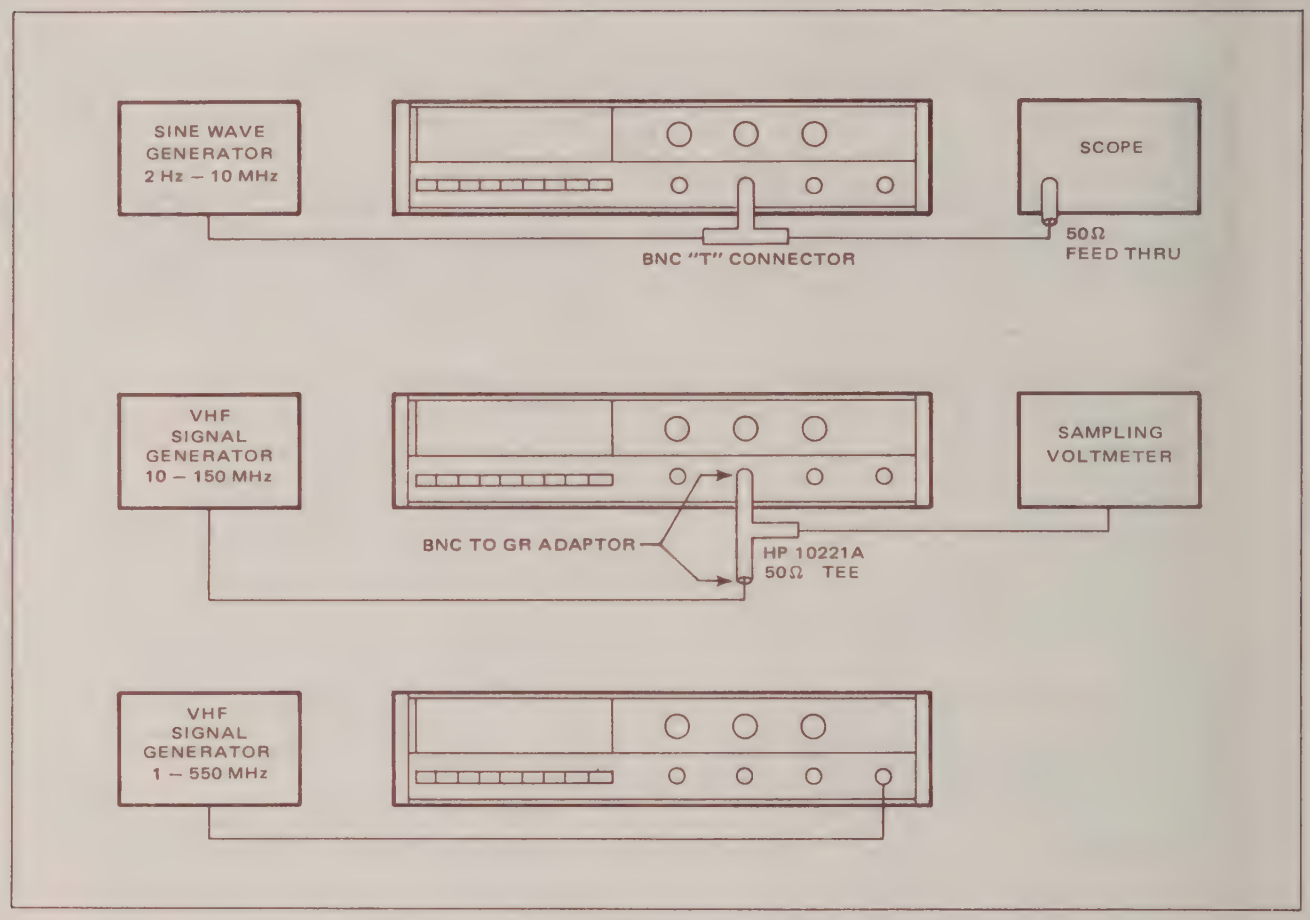
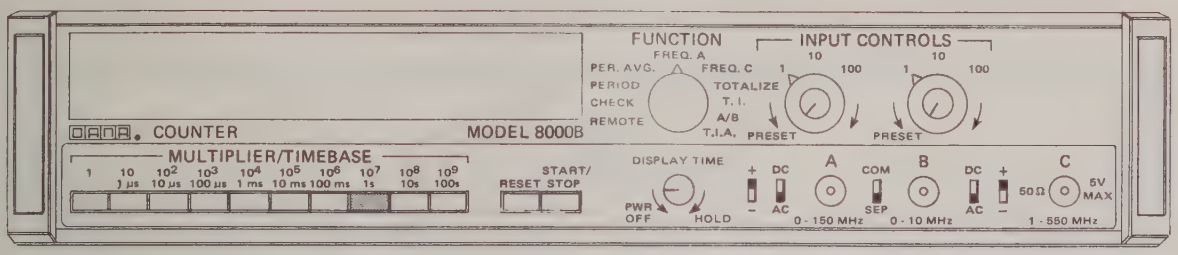


Figure 3.2 - Frequency Response Check Connections

Table 3.6 - Frequency Response and Sensitivity



DISPLAY TIME: Power on/CCW position
FUNCTION: FREQ A
TIME BASE: 1 second
SLOPE A: (+) Plus
SLOPE B: (+) Plus
COUPLING A: AC
STORAGE: ON

COUPLING B: AC
INPUT RANGE CONTROL A: 1
TRIGGER LEVEL CONTROL A: PRESET
INPUT RANGE CONTROL B: 1
TRIGGER LEVEL CONTROL B: PRESET
SEP/COM: SEP

1. Set controls as shown above.

2. Connect a BNC "T" connector to channel A input. Connect a sine wave generator (2 Hz – 10 MHz) and an oscilloscope to the "T" connector. Use a 50 ohm termination at the vertical input to the oscilloscope. Refer to figure 3.2 for hookup.

3. Adjust the sine wave generator between 10 Hz to 10 MHz maintaining 50 mV RMS output. Verify that the counter displays the frequency through this range. Change the A slope to (–) minus. Verify that the counter displays the frequency through this range.

4. Replace the sine wave generator with a VHF signal generator. Connect generator as shown in figure 3.2 and adjust for a 50 mV RMS output.

5. Set the Time Base to 1 second and the A slope to (+) plus.

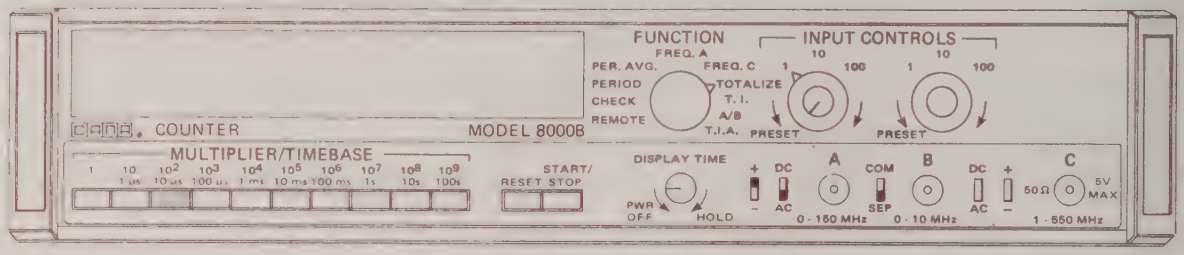
6. Vary the signal generator from 10 MHz to 100 MHz. Verify that the counter displays the frequency.

7. Set the output of the VHF signal generator to 100 mV RMS. Vary the signal generator from 100 MHz to 150 MHz. Verify that the counter displays the frequency.

8. Frequency C Models 8020B, 8030B. Change the function to Frequency C. Connect the VHF signal generator as shown in figure 3.2 and set the output to 50 mV RMS (for Option 030, set the output to 1 mV RMS). Vary the VHF signal generator between 1 MHz and 550 MHz (for Option 030, 10 MHz to 500 MHz).

9. The counter should display all frequencies in this range.

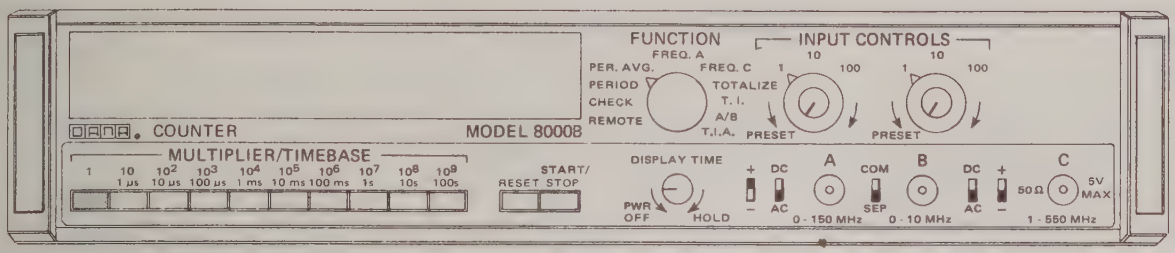
Table 3.7 - Totalize



DISPLAY TIME: Power on/CCW
FUNCTION: TOTALIZE
MULTIPLIER: 10^2
INPUT VOLTAGE RANGE A: 1
TRIGGER LEVEL A: PRESET

1. Set the counter controls as shown above.
2. Connect test oscillator to the counter at Input A. Set the oscillator output to .5V RMS at a frequency of 1 MHz.
3. Connect an oscilloscope to the scaled output jack on the counter rear panel.
4. Push the Reset on the counter. The display should read all zeros. Push the Start/Stop button. The display should totalize.
5. The scaled out should be a series of pulses with an amplitude of greater than 2V P.P. The scaled out repetition rate will be 10 kHz.
6. Depress the Start/Stop again. Totalizing should stop and the accumulated count should be displayed.
7. Push the Reset button and the display should be all zeros.

Table 3.8 - Period and Period Average



DISPLAY TIME: Power on/CCW
FUNCTION: PERIOD
MULTIPLIER: 1

INPUT VOLTAGE RANGE: 1
INPUT TRIGGER LEVEL A: PRESET

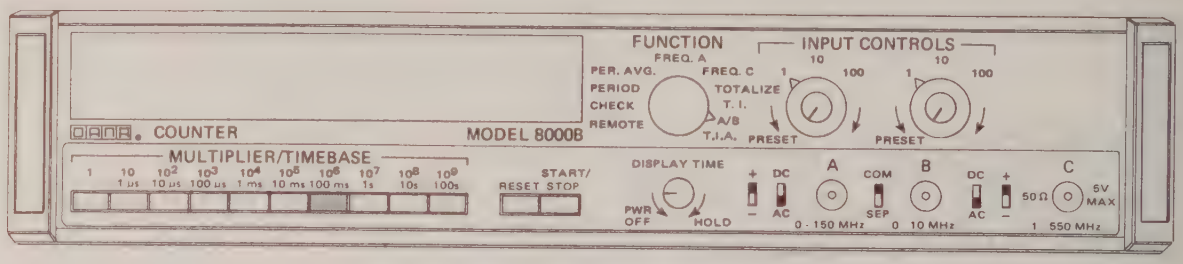
PERIOD

1. Set the counter controls as shown above.
2. Connect a test oscillator to Input A. Adjust the output of the oscillator to .5V RMS.
3. Vary the test oscillator frequency between 10 Hz and 10 MHz. The counter will display the period of the frequency.

PERIOD AVERAGE.

1. Set the Function switch to Period Average. Set the multiplier to 10.
2. Vary the test oscillator frequency between 10 Hz and 10 MHz.
3. The counter will display the period by taking the average period of the periods averaged.

Table 3.9 - A/B Ratio

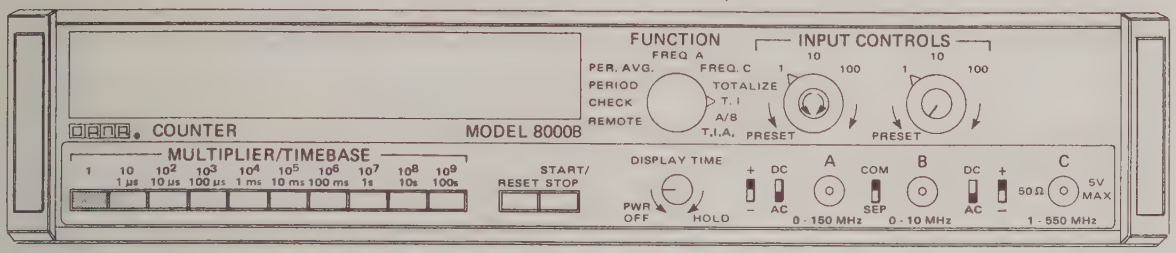


DISPLAY TIME: Power on/CCW
FUNCTION: A/B
MULTIPLIER: 10^6
SLOPE (A and B): (+) Plus
COUPLING (A and B): AC
INPUT VOLTAGE RANGE (A and B): 1
SEP/COM: COM
STORAGE: ON
TRIGGER LEVEL (A and B): PRESET

A/B RATIO (Not in 8020B)

1. Set controls as shown above.
2. Adjust test oscillator output to 10 MHz at 100 mV RMS.
3. Connect test oscillator to Input A.
4. Counter should display 1000000 counts.

Table 3.10 - Time Interval and Time Interval Average



DISPLAY TIME: Power on/CCW
FUNCTION: T. I.
MULTIPLIER: 1
SLOPE A: (+) Plus
SLOPE B: (+) Plus
COUPLING A: AC
COUPLING B: AC

INPUT VOLTAGE RANGE A: 1
INPUT VOLTAGE RANGE B: 1
SEP/COM: COM
STORAGE: ON
TRIGGER LEVEL A: Adjust
TRIGGER LEVEL B: PRESET

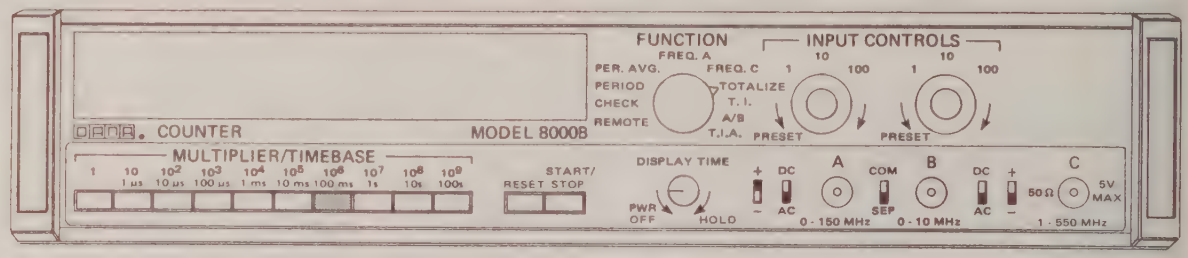
TIME INTERVAL (Not in 8020B)

1. Set controls as shown above.
2. Connect pulse generator output and oscilloscope to a "T" connector. Connect the "T" connector to the input "A" on the counter. Use a 50 ohm feed through on the input to the oscilloscope.
3. Adjust the pulse generator output to 900 kHz repetition rate, with a 200 nanosecond pulse width at 1V peak to peak.
4. The counter will display the period of the waveform.
5. Set slope B to (–) minus. The counter will display pulse width.

TIME INTERVAL AVERAGE (Not in 8020B)

6. Set the function to T.I. AVG., and the multiplier to 10^3.
7. The counter will display the pulse width of the input waveform.
8. Set the slope B to (+) plus. The counter will display the period of the input waveform.

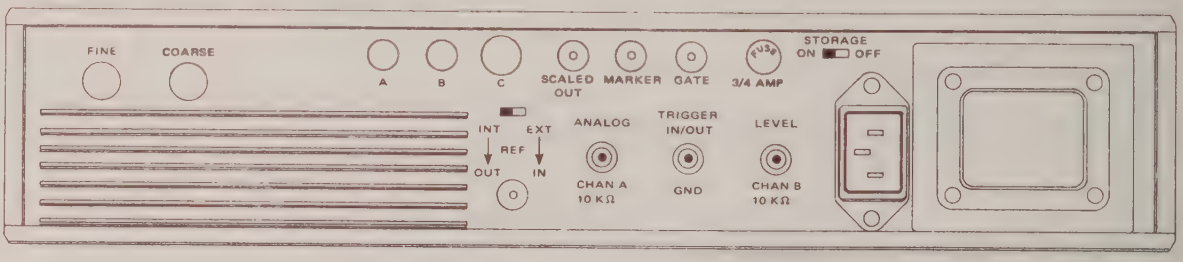
Table 3.11 - Display Time and Gate Output



DISPLAY: Power on/CCW

FUNCTION: TOTALIZE

1. Set controls as shown above.
2. Connect the vertical input of an oscilloscope to the gate output on the counter rear panel.
3. Press Reset and check that the gate output is low.
4. Press Start/Stop and check that the gate output is greater than 2V.
5. Press Start/Stop again and check that the gate output is low.
6. Set the Function switch to Frequency A and the Time Base to 100 msec.
7. Vary the Display Time and check that the repetition rate changes from approximately 30 milliseconds to 5 seconds.



4.1 GENERAL.

4.2 This section covers the theory of operation of the Series 8000B Counter. Operation of the unit is dependent on the measurement mode selected. For this reason, general operating principles of each mode of operation are described first followed by individual circuit descriptions. Where circuitry differences occur between models, the models covered are identified.

4.3 Drawings in this section are included for explanation only. For specific reference designators, wiring details, etc., refer to the complete schematics in Section 6.

4.4 MEASUREMENT MODES.

4.5 Figures 4.2 through 4.11 summarize the basic principles of each operating mode in simplified form. Any point (positive or negative) on the input waveform can be selected to trigger the generation of pulses to the main gate.

4.6 The block labeled "counter" refers to both a high-speed decade on the Switch board and the display counter. The high-speed decade divides its input by 10 and advances the display counter. It also updates the least-significant readout position (figure 4.1).

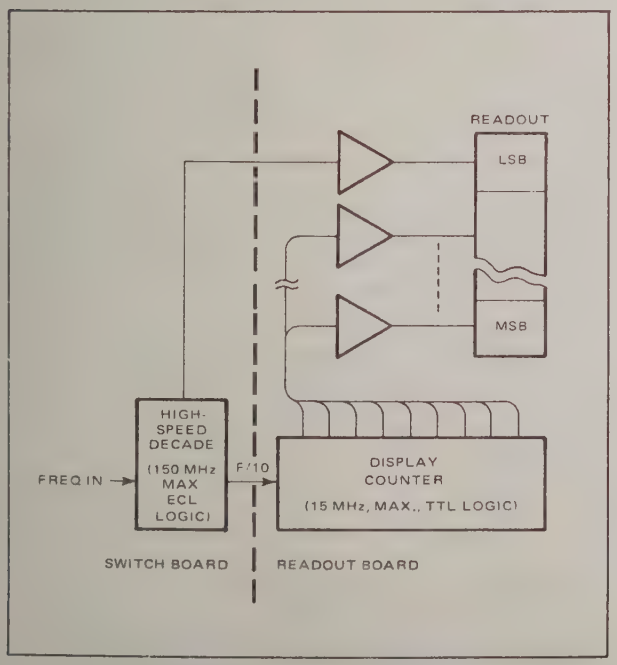


Figure 4.1 - Counter Definition

4.7 The "Display" block includes quad-latches and drivers for each of the readout positions (bits), and the readout tubes.

4.8 The "Reference Frequency" block can be either an external reference frequency or the internally generated reference frequency. The internal reference includes the reference oscillator (on Readout board), and the reference conditioning circuits (on the Switch board).

4.9 "Main Gate" refers to the logic that generates the signal $\overline{\Delta t}$. This signal controls the times at which the counter begins or stops counting. Counter operation is dependent on the mode of operation and other selections made by the operation (timebase, input trigger level, etc).

4.10 Self-Check Mode.

4.11 The Self-Check mode of operation (figure 4.2) enables the operator to check for proper operation of the counter. The reference frequency is used for two purposes. It is counted by the counter during the measurement time and it generates the time base frequency that produces the gating signal. Proper operation of the counter is determined by varying the time base and observing the readout (see Section 3, table 3.3).

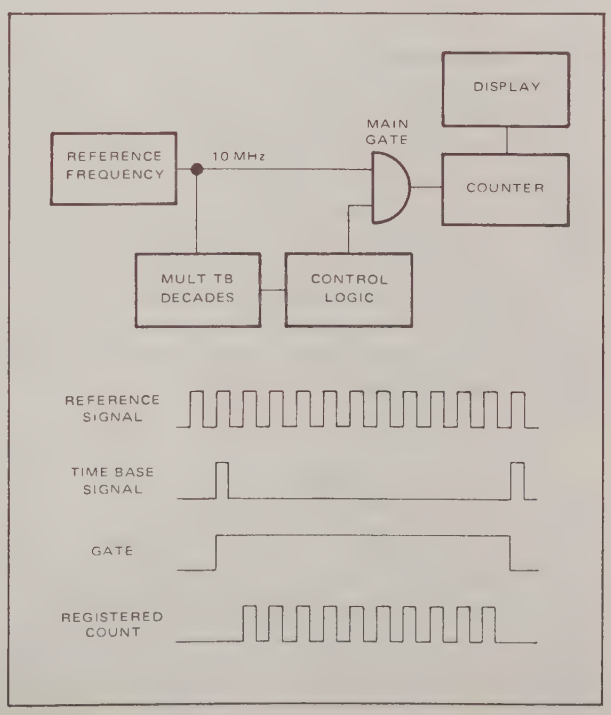


Figure 4.2 - Self-Check Mode

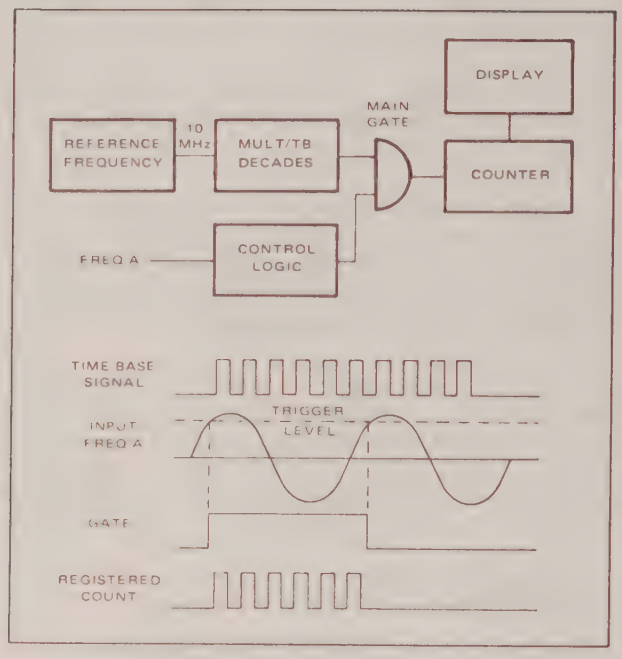


Figure 4.3 - Period Mode

4.12 Period Mode.

4.13 Period is the inverse of frequency. Therefore, frequency A is applied to the control logic and the reference frequency is connected to the multiplier/timebase decades (figure 4.3).

4.14 Clock pulses are derived by dividing down the 10 MHz reference oscillator output. The specific decade division is determined by the setting of the MULTIPLIER/TIMEBASE switches. The output of the M/TB decades is presented to the input of the counter. Trigger pulses resulting from two consecutive signals from input A are applied to the control logic. The first trigger pulse opens the main gate; the next pulse closes it. During "gate open" time, the counter counts the applied clock pulses. The count is displayed on the readout directly in microseconds, milliseconds, or seconds, according to the MULTIPLIER/TIMEBASE switch setting.

NOTE

Low Frequencies may be determined more accurately by measuring period rather than frequency directly. This is because the longer period of a low frequency allows more counts to accumulate in a period measurement. Therefore, resolution and accuracy are both improved.

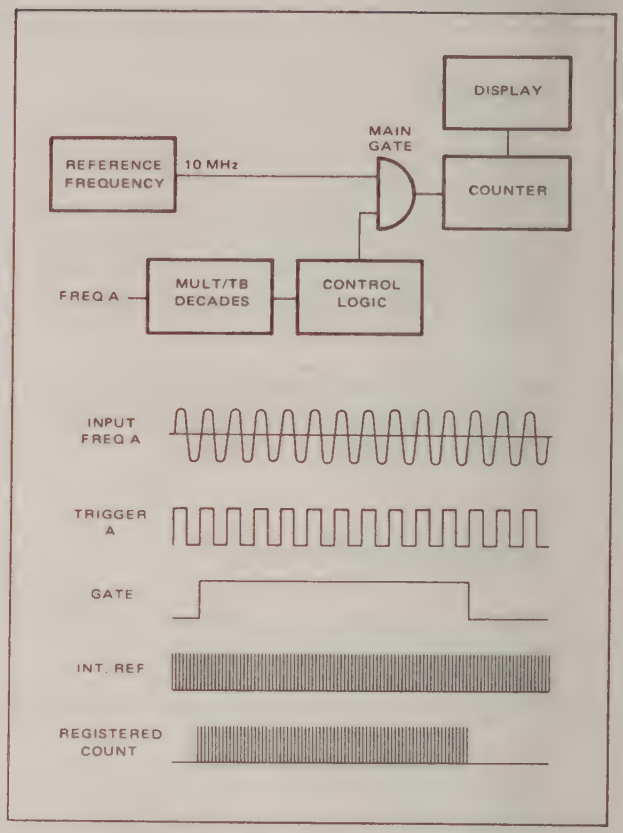


Figure 4.4 - Period Average Mode

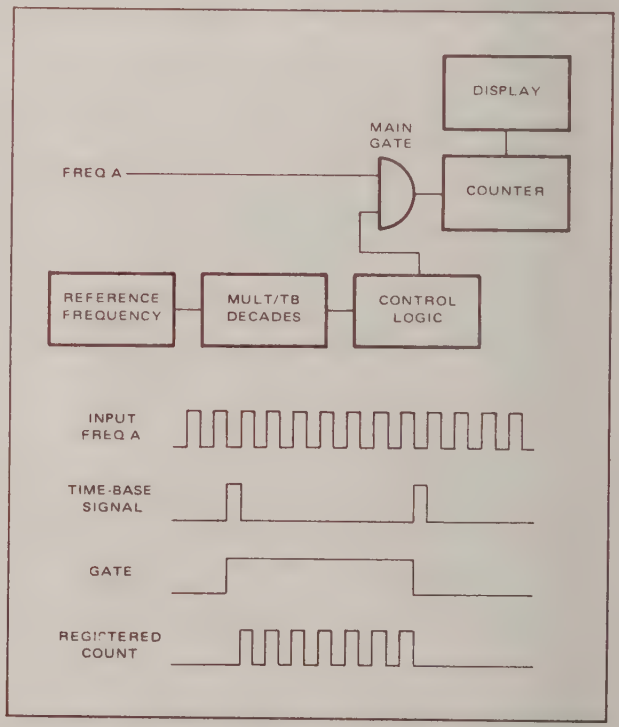


Figure 4.5 - Frequency "A" Mode

4.15 Period Average Mode.

4.16 Period Average mode is used to obtain increased resolution and accuracy over period measurements. The more periods over which a signal is averaged, the greater the accuracy of the measurement.

4.17 In this mode of operation (figure 4.4), the reference oscillator is routed directly to the main gate and the unknown frequency is routed through the multiplier/time base decades to the control logic which, in turn, controls the main gate. The pulses occurring during main "gate open" are counted, stored, and an accurate readout measurement is displayed. The "gate open" period is determined by the setting of the MULTIPLIER/TIMEBASE switches.

4.18 Frequency A Mode.

4.19 During direct frequency measurements, the counter compares the unknown frequency against the known reference frequency (figure 4.5).

4.20 Input signal F_a is routed to the main gate of the counter. The internal reference supplies a 10 MHz signal through the multiplier/time base decades and through the control logic to control the main gate.

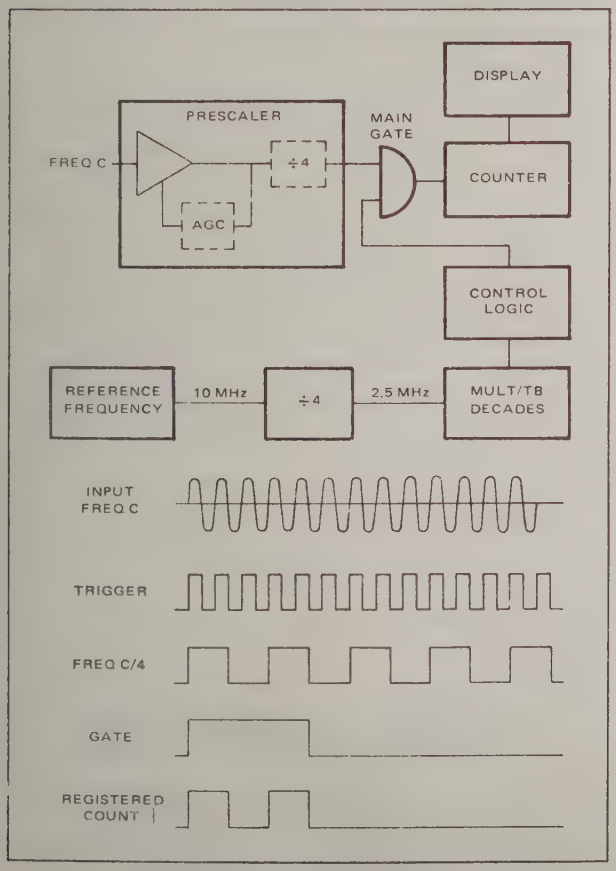


Figure 4.6 - Frequency C Mode

4.21 The number of input pulses accumulated during the main "gate open" interval is a measurement of the input frequency. The count obtained is displayed on the readout. This display may be retained until such a time as a new sample is ready to be displayed.

4.22 Frequency C Mode. (Not available in Model 8010B.)

4.23 In the Frequency C mode, the unknown frequency is applied to the main gate through the prescaler. The prescaler includes an amplifier, automatic gain control circuit, and a divide-by-four circuit (figure 4.6).

4.24 The AGC circuit maintains the required amplifier gain which alleviates the need for manual trigger and range control. The divide-by-four circuit is necessary to reduce the unknown frequency to a frequency which the main counter circuitry can count. The reference frequency is also divided by four to enable direct readout. The actual gate time is four times the selected time base.

4.25 Totalize Mode.

4.26 In Totalize mode, the main gate is controlled by the manual START/STOP switch on the front panel of the instrument or external START/STOP commands (figure 4.7).

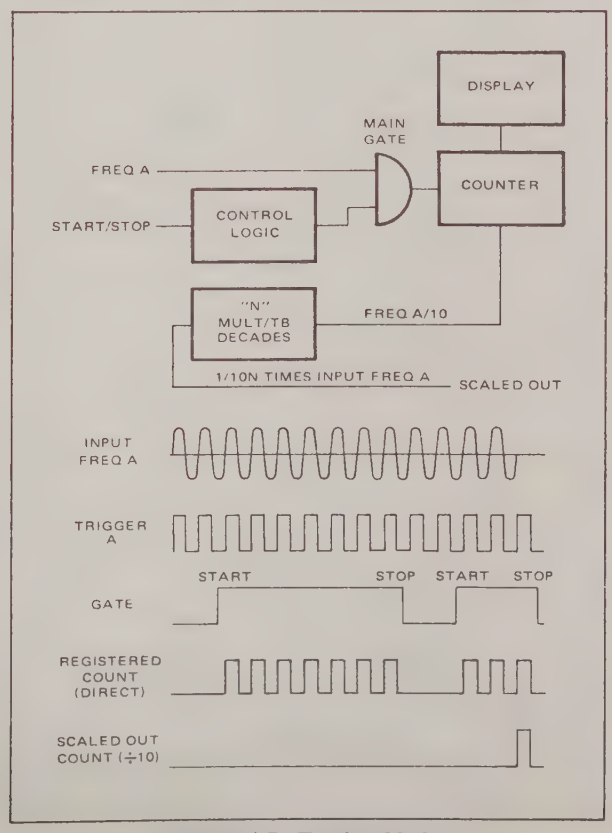


Figure 4.7 - Totalize Mode

4.27 With the first Start/Stop command, the control logic opens the main gate allowing the input pulses to be totalized by the counter. Simultaneously, a continuous update is supplied to the flip-flops which make up the display latches. The counter readout then represents the input pulses received during the interval between "start" and "stop". External start/stop commands may be applied via the REMOTE connector if equipped with the systems interface option.

4.28 In this mode, the instrument delivers a scaled output frequency to a connector on the rear panel, SCALED OUT. The output is the input signal frequency scaled by 1/10N where N is the multiplier setting.

4.29 Time Interval Mode. (Not available in Model 8020B.)

4.30 The Time Interval mode of operation allows measurement of the time between two electrical events to a maximum resolution of 100 nanoseconds (figure 4.8). The first event (start) is connected to channel A and opens the gate. The second event (stop) is connected to channel B and closes the gate. These signals control the main gate through the control logic. Slope and trigger level controls on the front panel allow variable trigger levels on the + or – slope of the input waveforms. Pulses from the 10 MHz reference oscillator are routed to the multiplier/timebase decades and to the main gate.

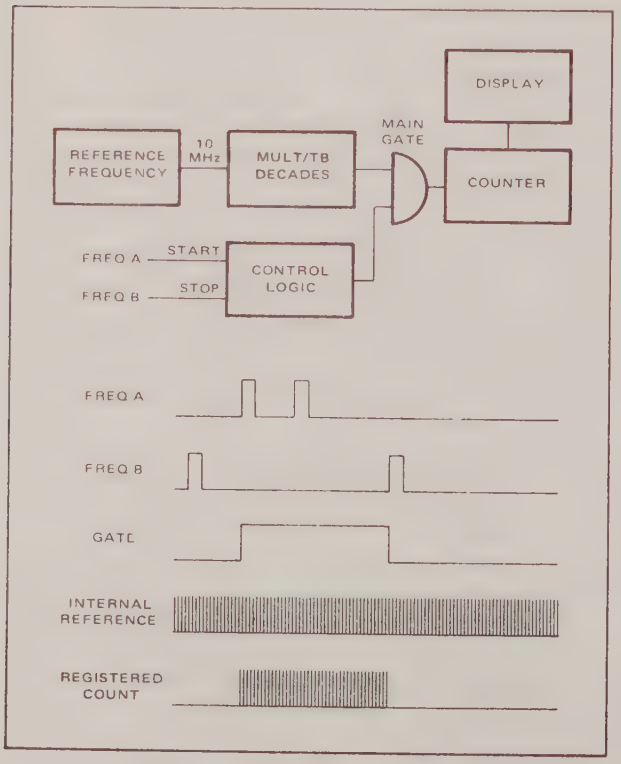


Figure 4.8 - Time Interval Mode

4.31 The pulses occurring during the main gate are counted and displayed. Channel A can be triggered after the channel B trigger in 30 ms on a single time interval measurement.

4.32 Time Interval Average. (Not available in Model 8020B.)

4.33 Similar to the Time Interval mode of operation, the Time Interval Average mode measures the count accumulated during a multiple of intervals (figure 4.9). It then averages the count by shifting the decimal point and displaying the result. This mode of operation makes it possible to achieve greater resolution and accuracy when measuring time intervals. The A trigger point can follow the B trigger point as close as 200 nanoseconds.

> **NOTE**
>
> In T.I. Average mode, the input signals must be repetitive and asynchronous with the counter's time base.

4.34 A/B (Ratio) Mode. (Not available in Model 8020B.)

4.35 This mode is identical in function to the frequency measurement modes, but substitutes an external signal for the reference frequency (figure 4.10).

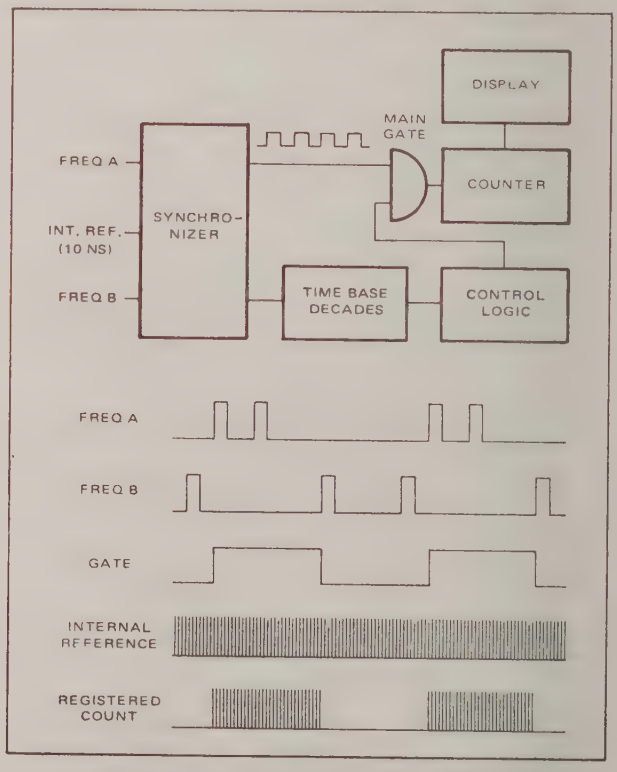


Figure 4.9 - Time Interval Average Mode

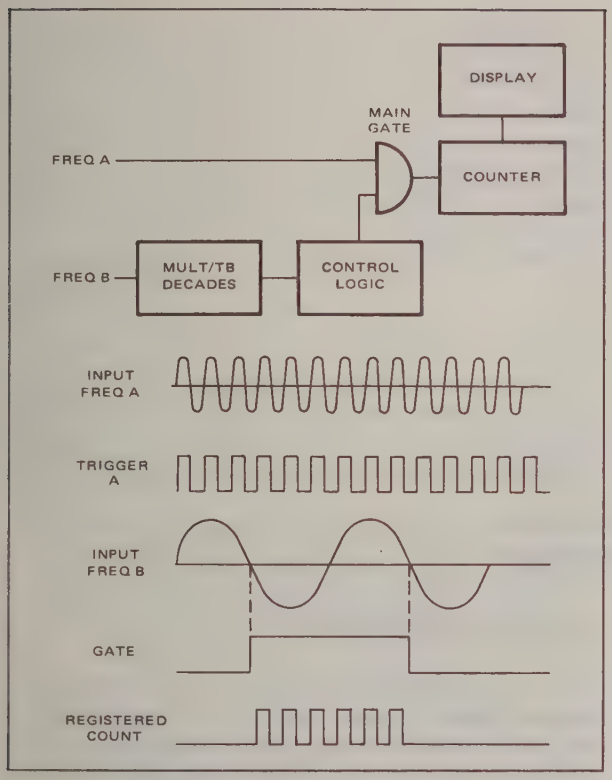


Figure 4.10 - A/B Ratio Mode

4.36 The higher of the two frequencies which are to be measured is connected to input A; the lower frequency to input B. Input B is applied to the multiplier/timebase decades. The higher the multiplier/timebase selected, the greater the resolution and the longer the measurement time. Two successive trigger pulses derived from the multiplier/timebase decades applied to input B open and close the main gate. During the "gate open" interval, the counter counts the trigger pulses derived from input A and the ratio Fa/Fb is then displayed on the readout.

4.37 CIRCUIT DESCRIPTIONS.

4.38 A block diagram of the counter is shown in figure 4.11. The circuit descriptions to follow make reference to the schematics in Section 6 as well as to partial schematics within this section.

4.39 Prescaler (Schematic: figures 6.13 and 6.15). Not available in Model 8010B.

4.40 The Prescaler provides the signal conditioning function for channel C. It accepts frequencies from 1 MHz to 550 MHz (10 MHz to 500 MHz with 030 option), automatically controls the amplitude of the signal, and divides the frequency of the signal by a factor of four. The scaling reduces the incoming signal to a rate compatible with the

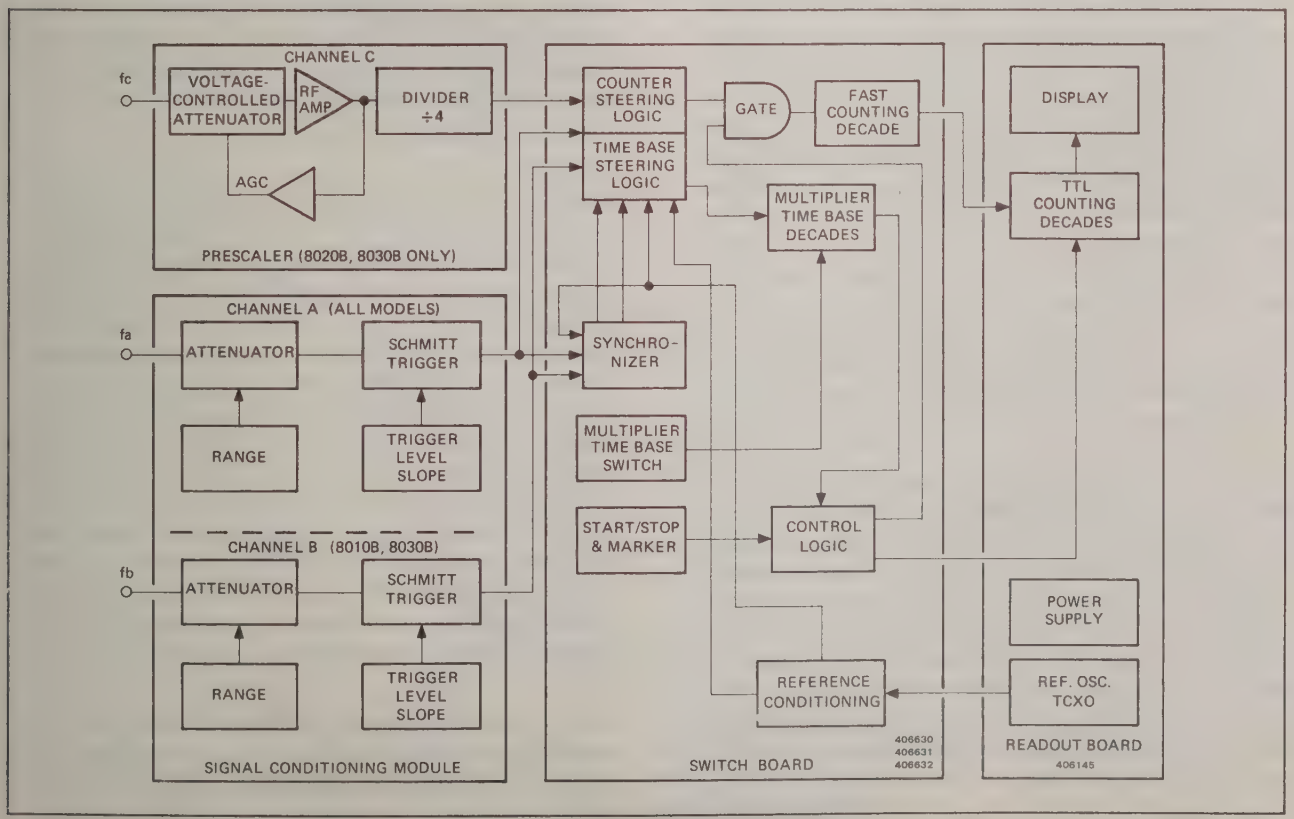


Figure 4.11 - Functional Block Diagram (All Models)

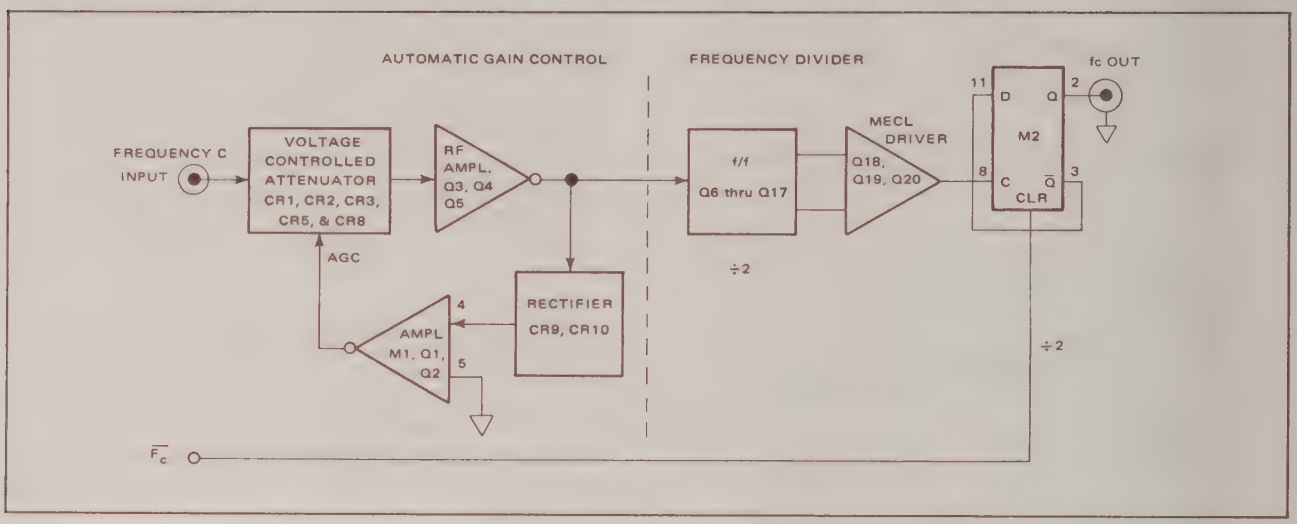


Figure 4.12 - 550 MHz Prescaler

high-speed decades. The circuitry, shown simplified in figure 4.12, is divided into two sections: the automatic gain control section (including the attenuator) and the frequency divider section.

4.41 AUTOMATIC GAIN CONTROL.

4.42 The "C" input signal from the input connector passes through the voltage-controlled attenuator to the RF amplifier. The attenuator consists of two diodes in series with the signal path and three diodes shunting the signal path. With no signal from the AGC amplifier (M1), series diodes CR2 and CR5 are forward-biased providing a low impedance signal path while shunting diodes CR1, CR3, and CR8 are back-biased and provide little attenuation to the signal. As the AGC signal goes negative, series diodes CR2 and CR5 conduct less, increasing their apparent impedance while the diodes in shunt begin conducting and attenuating the signal. The signal from the attenuator passes through the three-stage amplifier (Q3, Q4, and Q5) which increases the signal level to approximately 200 mV rms. The AGC circuit maintains 200 mV rms at the bases of Q11 and Q14.

4.43 The output of the amplifier is applied to the divider section and to a voltage rectifier circuit consisting of diodes CR9 and CR10. The rectifier produces a positive dc voltage level proportional to the RF level of the amplifier output which, after amplification and inversion by differential amplifier M1, controls the attenuator. The gain control circuit holds the signal level of the amplifier input to approximately 50 mV (1 mV with option 030). With option 030, operation is the same as described for the standard Prescaler, but an additional stage of amplification is included (see schematic, figure 6.15).

4.44 FREQUENCY DIVIDER.

4.45 This portion of the Prescaler consists of a discrete transistor flip-flop, a driver circuit (Q18, Q19, and Q20), and a ECL* type D flip-flop, M2. The discrete transistor flip-flop consists of transistors Q6 through Q17. The function of this circuit is to divide the frequency of the signal by two. At low frequency operation, the information is transferred so fast (on the positive edge of the pulse) that it is possible for the flip-flop to go into oscillation at a natural resonate frequency of 300 MHz. A Skew circuit is employed to guard against self oscillation.

4.46 The driver stage for the discrete flip-flop consists of Q8, Q11, Q14, and Q17. The level at which transistors Q8 and Q11 switch is the same at all frequencies. The level at which transistors Q14 and Q17 switch is controlled by the skew circuit consisting of C35, CR16, R55, R59, and C38. The output of the skew circuit is frequency dependent. At frequencies below 300 MHz, the current path is from −18V through resistors R59, R55, and diode CR16 to ground. This biases Q17 at −.2V. Below 300 MHz, the input signal has to overcome the −.2V bias on Q17 base before the flip-flop toggles. As the frequency goes above 300 MHz, the impedance of capacitor C35 decreases and the signal coupled by C35 increases in amplitude. The signal is rectified by CR16. As the frequency continues to increase, capacitor C38 charges to a higher DC level (approaching zero) removing the −.2 volts bias.

4.47 Diodes CR11 through CR14 are level shifters which increase the rise and fall time of the discrete flip-flop. The output of the discrete flip-flop is amplified by Q18, Q19,

*emitter-coupled logic

and Q20. The signal is applied to ECL flip-flop M2. The reset line of M2 is controlled by $\overline{Fc}$. When Frequency C is selected $\overline{Fc}$ is false, M2 is released from the reset state and divides the frequency of the signal by two. The signal (now divided by four) is fed to the input gate of the steering logic. When $\overline{Fc}$ is true, Frequency C is not selected and the flip-flop M2 output is held in the reset state.

4.48 Signal Conditioning Module (Schematic: figure 6.2).

4.49 In Model 8020B, the Signal Conditioning Module conditions the signal to be compatible with ECL logic and establishes the trigger level of the channel A input. In Models 8010B and 8030B, an additional (and basically identical) module is used for conditioning the channel B input.

4.50 In dual-channel models, the input to the channel B Signal Conditioning Module comes from either of two sources depending on the position of the SEP/COM switch. In the COM (common) position, the B input signal is from the channel A input connector (and common with A). In SEP (separate), the signal is from the B input connector (figure 4.13).

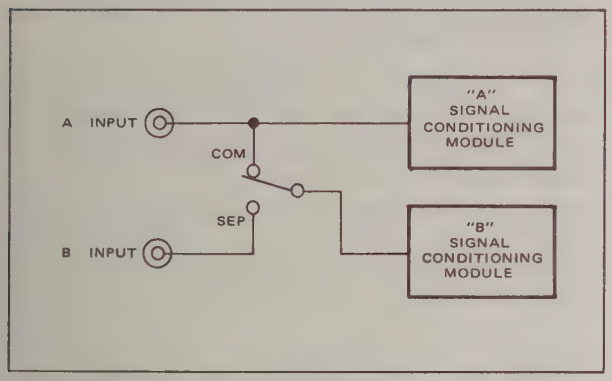


Figure 4.13 - SEP/COM Switch

4.51 Since the modules are identical for channels A and B, only channel A Signal Conditioning is described.

4.52 CHANNEL A ATTENUATOR (figure 4.14).

4.53 With the AC/DC coupling switch set to AC, the signal applied to input A flows through capacitor C1; with DC selected, the capacitor is bypassed through the coupling switch, S207. The signal flows through the attenuator according to the range selected. In the 1-volt range, the signal passes directly through the INPUT VOLTAGE range switch; in the 10-volt range, the signal is attenuated by a factor of 10 (20 dB); and in the 100 volt range, the signal is attenuated by a factor of 100 (40 dB). From the range switch, the signal passes through 100-kilohm resistor R4 in parallel with 47 pfd capacitor C2 to the signal conditioning network.

4.54 SCHMITT TRIGGER.

4.55 As shown in figure 4.14, the signal from the channel A attenuator (f_a in) flows through emitter follower circuits Q1 and Q2. Transistors Q4 and Q8 form a gain stage to drive the input side of a Schmitt trigger consisting of transistors Q3, Q5, Q6, and Q7. The signal from the attenuator is prevented from exceeding ±4 volts by clamp zener diodes CR1, CR2 and diodes CR3 and CR4. The trigger level of the trigger circuit is determined by the potential applied to the input of the follower circuits consisting of Q9 and Q10. With PRESET selected (the extreme counter-clockwise position of the front panel trigger level

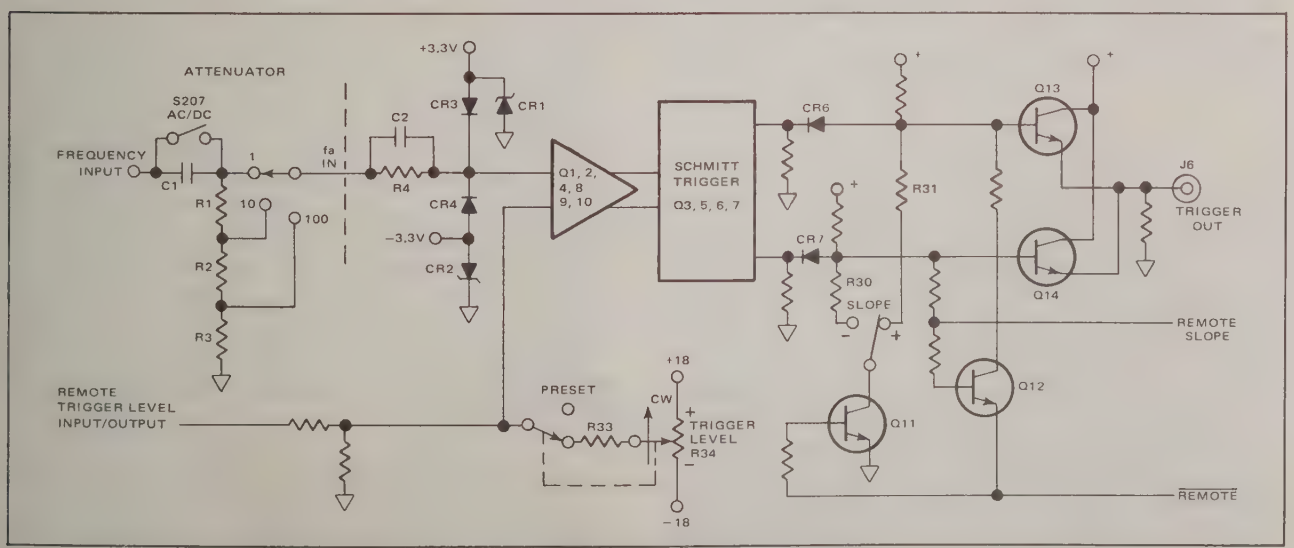


Figure 4.14 - Signal Conditioning Block Diagram

control) and assuming no remote level input, the trigger level is approximately zero volts (0 VDC ± 5% of the input voltage range selected). With PRESET out, the trigger level is adjustable by the trigger level control across ±300% of the range selected. The trigger level may be monitored by connecting a voltmeter across the analog output on the rear panel.

4.56 SLOPE.

4.57 The trigger circuit generates two outputs (180° out of phase) which are gated through diode CR6 or diode CR7, depending on the position of the +/– slope switch. With + slope selected, the anode of diode CR6 is held low through R31 and Q11. A positive pulse is generated during the positive-going edge of the input signal and passes through CR7, through Q14 to connector J6. With – slope selected, the anode of diode CR7 is held low through R30 and Q11. A positive pulse, generated during the negative-going edge of the input signal, passes through CR6 through Q13 to connector J6. When Remote is not selected, transistor Q11 is conducting and the signal that appears at J6 is determined by the position of the +/– (slope) switch on the front panel. In Remote, Q11 is off and Q12 determines the signal at J6.

4.58 Switch Board Assembly (Schematic: figure 6.4).

4.59 The Switch board assembly is one of two large printed circuit boards mounted to the base plate. The Switch board is accessible from the bottom of the counter. The switch board contains the following circuits: time base decades and switches, counter and time base steering logic, fast counting decade, control logic, reference conditioning, and a synchronizer circuit. Each circuit is described in the following paragraphs.

4.60 REFERENCE CONDITIONING CIRCUIT.

4.61 The Reference Conditioning circuitry converts the reference signal to a 10 MHz square wave and routes it to the steering circuits. This circuit processes a reference signal supplied either from the internal frequency source or from an external frequency standard through rear panel connector J106. The source is selected by the rear panel REF switch S102. The internal frequency source is a self-contained, temperature-compensated oscillator located on the Readout board. The external reference (1, 5, or 10 MHz) must be capable of delivering 1 volt RMS at connector J106 (input impedance is 1K ohm). With the REF switch set to the EXT position, an external signal is fed to the input of the conditioning circuitry and the signal path from the internal frequency source is open; with the INT position selected, the internal frequency source is supplied to the input of the conditioning circuitry and the output of the conditioning circuitry is routed to connector J106 for use as a secondary standard source.

4.62 The circuit is shown in simplified form in figure 4.15. The signal from the REF switch is shaped by the limiting action of inverter MA2 and applied to the Schmitt trigger circuit consisting of two inverters (MA2). The output is a square wave. The trigger output is differentiated through a capacitor-resistor combination (C37, R98) and the negative spikes from the differentiated signal are applied to the crystal filter circuitry (Q19, Y1). This circuit produces a 10 MHz damped oscillation that is sustained by input spikes at 10 MHz or by subharmonics at 1 and 5 MHz. The

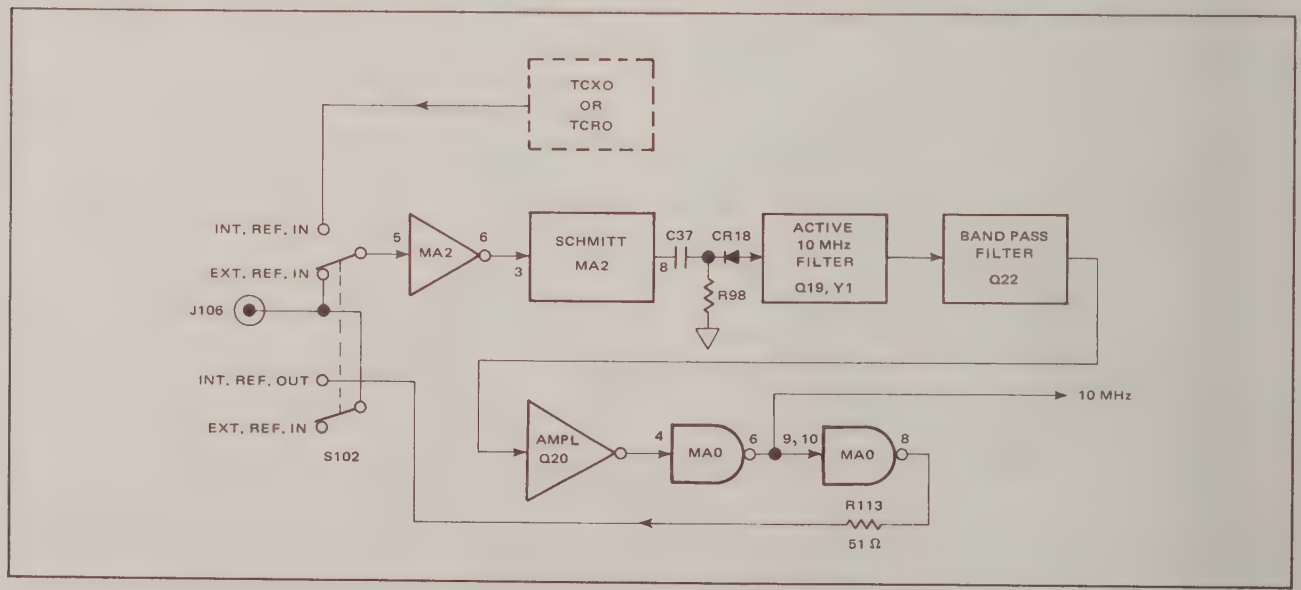


Figure 4.15 - Reference Conditioning Circuit

active filter output is applied to the bandpass filter, increasing the amplitude of the signal and removing the harmonics. The signal then flows through amplifiers Q20, Q21 and four NAND gates (MA0), two of which are used as inverters. The output of the first gate (MA0-6) is routed to the steering circuits in the instrument, the output of the second gate (MA0-8) passes through resistor R113 and the INT position of the reference switch to connector J106.

4.63 FAST COUNTING DECADE (Figure 6.4).

4.64 The Fast Counting Decade consists of four high-speed counters (MD2, MD3, and MD4) interconnected to form a divide-by-ten circuit. The BCD outputs of the counter are buffered and inverted through transistors Q3, Q4, Q5, and Q6 and routed to the quad latch ME9, driver MF9, and the least-significant digit readout of the Readout board. The buffered 4 and 8 bits from the decade are combined in NAND gate MC5 to form a quasi-square output (fa/10) with a frequency equal to 1/10 of the decade input signal. The counter is controlled by a gate signal applied to clock input C1 in the first flip-flop MD2. When C1 is false, the pulses at the clock input C2 are counted; when C1 is true, the flip-flop is inhibited. The gate control line connected to C1 is designated $\overline{\Delta t}$.

4.65 COUNTER STEERING LOGIC.

4.66 This circuitry routes signals to the input of the fast-counting decade according to the measurement mode selected. Signal flow through the circuit is shown in figure 4.16a through c.

4.67 Ratio, Totalize and Frequency A Modes (figure 4.16a).

4.68 Lines from the Ratio, Totalize and Frequency A positions of the FUNCTION switch are applied to a three-input NAND gate, MF5. The line for the selected mode is pulled low by the FUNCTION switch selection. The output of MF5 is high biasing CR1 and CR2 such that the f_a signal flows through CR1 and CR2 to MD1. MD1 is a ECL* four-input OR gate. The signal on pin 3 of MD1 causes the output of MD1 to change state (all other inputs to MD1 are low). The signal is routed to the clock input of MD2, a type D ECL flip-flop. Flip-flops MD2, MD3A, MD3B, and MD4 form a divide-by-ten fast-counting decade divider. The output of the fast counting decade drives the display counter on the Readout board and updates the least-significant digit of the readout.

4.69 Period and Time Interval Modes (figure 4.16b).

4.70 Signal flow in Period or Time Interval mode is as follows. Period or Time Interval is selected by the

*emitter-coupled logic

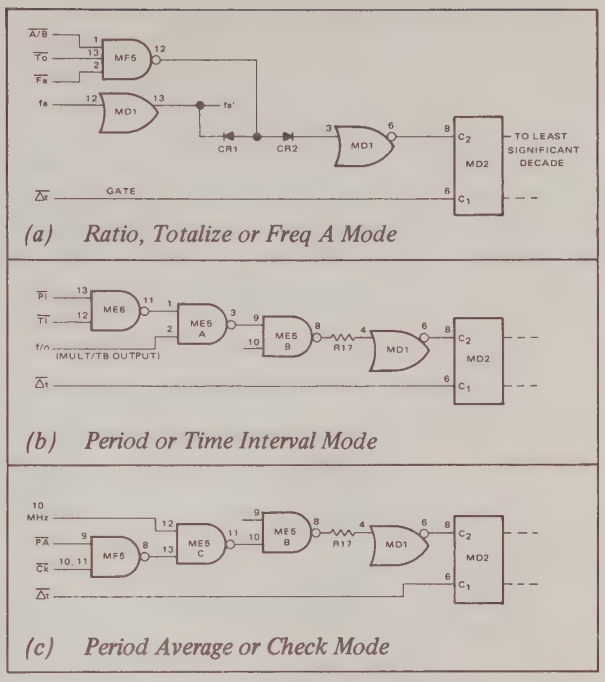


Figure 4.16 -Counter Steering Logic

FUNCTION switch, and one of the two lines, $\overline{PI}$ or $\overline{TI}$, is pulled to ground. These lines are connected to a two-input Nand gate, ME6. The output of ME6 goes high and is connected to the input to ME5A, a two-input Nand gate. The second input to ME5A is f/n. When the input line, pin 1, to ME5A is high, f/n is gated through ME5A and inverted. The signal is applied to the input (pin 9) of ME5B. The second input, pin 10, is high and the signal f/n is inverted through ME5B. The output of ME5B, f/n, goes to pin 4 of MD1, an ECL four-input NOR gate. The other three inputs to MD1 are low. The output of MD1 is routed to the clock input of the fast counting decade (MD2-8). The time that the counts are allowed to accumulate in the fast counting decade is controlled by $\overline{\Delta t}$ (main gate).

4.71 Period Average and Check (figure 4.16c).

4.72 Signal flow in Period Average or Check mode is as follows. Period Average or Check is selected by the FUNCTION switch, and one of the two lines, $\overline{PA}$ or $\overline{Ck}$, is pulled to ground. $\overline{PA}$ and $\overline{Ck}$ are connected to the inputs of a three-input Nand gate, MF5. The output of MF5 is high. The signal from MF5 is connected to two-input Nand gate, ME5C. The other input is connected to the 10 MHz Reference. The output of ME5C, (10 MHz) is connected to the input of a two-input Nand gate, ME5B. The other input to ME5B is high. The output of ME5B (10 MHz) is connected to the input of a four input ECL Nor gate, MD1. The other three inputs are low. The output of MD1 is routed to the clock input of the fast-counting decades (MD2-8).

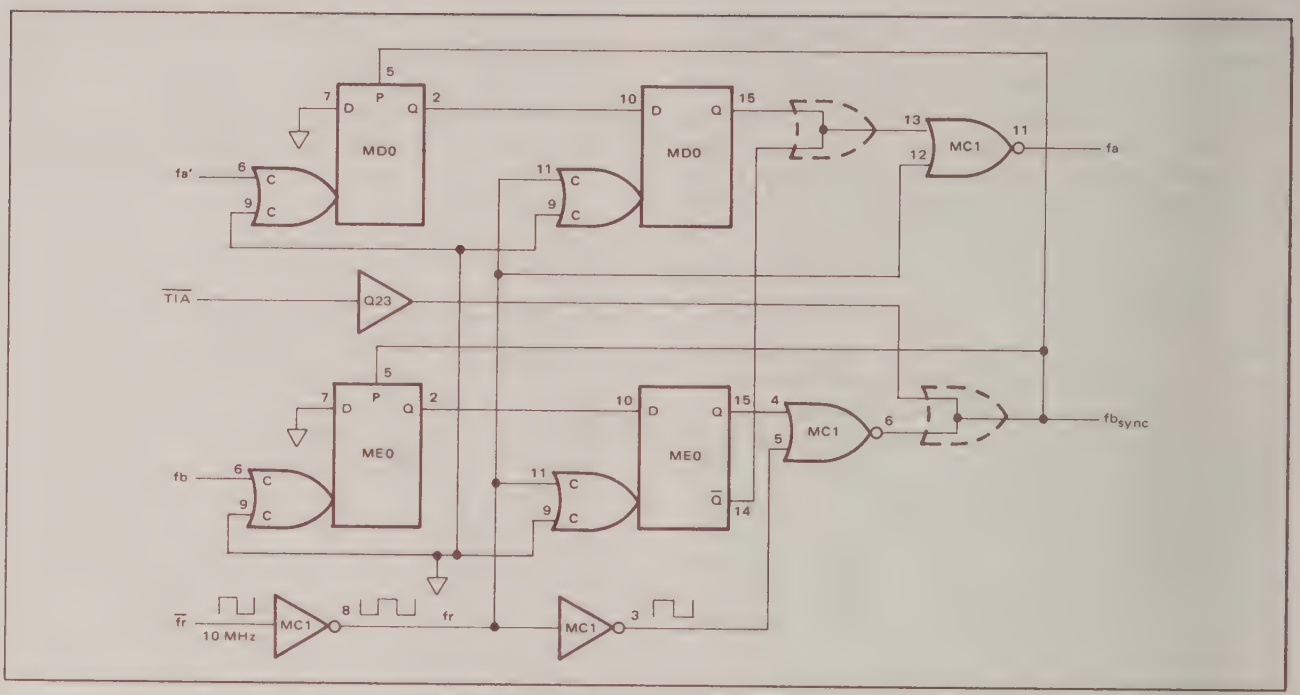


Figure 4.17 - Synchronizer Block Diagram

4.73 SYNCHRONIZER (Not in Model 8020B).

4.74 The synchronizer circuit is utilized when the Time Interval Average mode is selected. The TIA mode averages a predetermined number of intervals. Two different types of gates are required: a synchronized gate to eliminate the ±1 count error for each interval averaged and a main gate to select the predetermined number of intervals to be averaged. Figure 4.17 shows a block diagram of the synchronizer and the timing diagram is shown in figure 4.18.

4.75 In Time Interval Average mode, the synchronizer will not be enabled until signal f_b SYN pulse occurs.

4.76 The first pulse on channel B (f_b) is routed to the synchronizer and is gated (MC1-6) with the reference signal. The signal f_b SYN, synchronous with the reference signal, is routed to the time base decades. This first f_b SYN pulse causes the time base decades to change from nines to zeros and produces the first f/n pulse. Signal f/n is routed to the START flip-flop in the control logic. The START flip-flop is set by the Start pulse which opens the main gate and generates $\overline{\Delta t}$.

4.77 The synchronizer is now ready to initiate a synchronized gate. The next pulse from channel A is routed to the synchronizer and allows the next reference pulse to open the synchronous gate (MC1-11). The output of the synchronous gate (10^7 counts per second) is routed to the counting decades. Since the main gate is already open because of the previous f_b SYN, the counting decades count the pulses. This is the start of the A-to-B interval measurement.

4.78 The next pulse to arrive on channel B produces f_b. Signal f_b is routed to the synchronizer and allows the next reference pulse to terminate the synchronous gate. The number of f_b SYN pulses to the time base decades required for the second f/n to be generated is dependent on the multiplier setting of the MULTIPLIER/TIMEBASE switches. If the "1" multiplier is selected, f/n is produced with the current f_b SYN pulse. If the "10" multiplier is selected, ten f_b SYN pulses must accumulate in the time base decade before the second f/n is generated. If f/n is not generated before f_a arrives, the pulses from the reference signal do not accumulate in the counter. Signal f/n is routed to the STOP flip-flop. The main gate and $\overline{\Delta t}$ are terminated with the second f/n. The display time flip-flop is reset for the display timeout. At the end of the display timeout, the update pulse is generated and the counter decades are reset to zero for a new measurement.

4.79 When the TIA mode is selected, Q23 is turned off releasing the Preset inputs to flip-flops MD0-5 and ME0-5. The output of transistor Q23 and the output of gate MC1-6 form a wired OR gate. The Q outputs of MD0 and ME0 have previously been preset. The Q outputs of MD0-15 and ME0-15 disable gates MC1-13 and MC1-4. Signal f_b

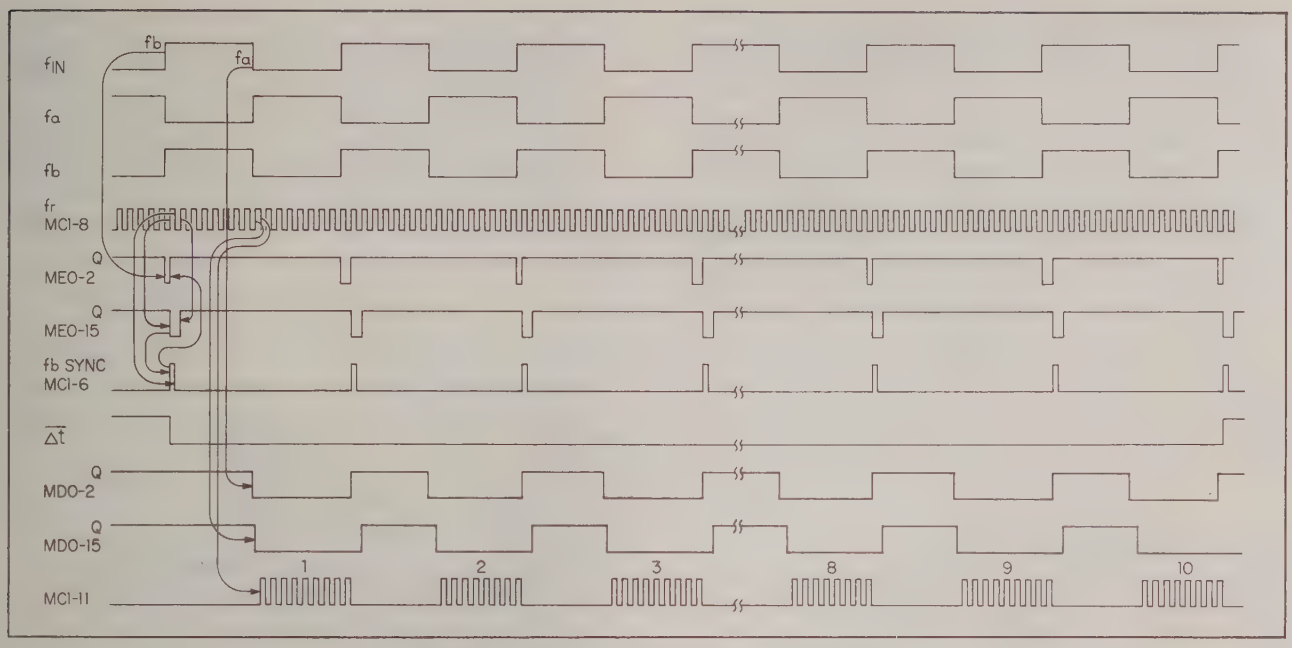


Figure 4.18 - Synchronizer Timing Diagram

clocks the low D input of ME0-7 to the Q output of ME0-2. On the next positive clock (fr) from inverter MC1-8, the low D input on ME0-10 is clocked to the Q output of ME0-15. The low Q output enables gate MC1-4. The reference clock now is inverted and appears at MC1-6. The high output of MC1-6, (f_b SYN) presets the Q outputs of flip-flops MD0-2 and ME0-2 high. Note that the Q output of MD0-2 is high because f_a has not clocked the low D input to the Q output (MD0-2). Signal f_b SYN goes to the multiplier time base decades. The trailing edge of the first f_b SYN causes the outputs of the multiplier time base decades to change state and open the main gate $\overline{\Delta t}$.

4.80 On the next positive clock pulse from inverter MC1-8, the high D input to ME0-10 is clocked to the Q output disabling the gate MC1-6 forming the trailing edge of f_b SYN. The output of gate MC1-6 goes low. The signal f_a arrives at the input to flip-flop MD0 and clocks the low D input to the Q output. The next positive output from inverter MC1-8 clocks the low D input of MD0-10 to the Q output enabling the synchronous gate MC1-11. The reference clock via MC1-8 and MC1-11 flows to the counting decades. Signal f_b arrives at the input to ME0-6 and clocks the low D input to the Q output. The next positive clock pulse from MC1-8 clocks the low D input to the Q output of ME0-15. The Q output of MD0-14 is connected to the Q output of MD0-15 and forms another wired OR gate. $\overline{Q}$ of ME0-14 causes the Q output of MD0-15 to go low disabling MC1-11 and stopping the reference clock to the counting decades. At the same time, gate MC1-6 is enabled for one clock pulse which presets flip-flops MD0-5 and ME0-5, and generates f_b SYN. Signal f_b SYN generates a stop pulse which causes the main gate to close, generation of the update pulse, and a clear to be generated clearing the counting decades. The process begins over again after timeout and the arrival of f_b, then f_a, in that order.

4.81 MULTIPLIER TIME BASE SWITCH LOGIC.

4.82 The interlocking pushbutton switches select one of ten decade divider outputs. The time base decades divide the signal applied to the input by 1, 10, 10^2, 10^3, 10^4, 10^5, 10^6, 10^7, 10^8, or 10^9. The outputs are selectable by the MULTIPLIER/TIME BASE switches. The MULTIPLIER/TIME BASE switch selected pulls the line low. The low level is routed to an inverter through a decoupling diode. The high output is connected to a two-input NAND gate. The other input of the NAND gate is connected to one of the ten outputs of the time base decades. If a multiplier of 10^2 through 10^9 is selected, the output signal of the nand gate is routed through a reclocking circuit. The reclocking circuit is necessary to remove the propogation delays developed in the time base decades. The 1 and 10 multipliers are routed around the reclocking circuit via two nand gates. The output of the gate is the frequency applied to the time base decades divided by the multiplier or f/n.

4.83 Signal f/n is used as a start/stop pulse within the counter and delivered to the rear panel as Scaled Out. Signal f/n is always produced with the first pulse applied to the time base decades and the first pulse is not dependent on the multiplier selected. The time base decades are reset to the nine state at the end of display time when $\overline{T^2 \text{ CLEAR}}$ goes low. When the first pulse is applied to the time base

decades, the output of the decades changes from all nines to all zeros. Thus, a change of state of output f/n is produced from any one of the ten multiplier switch positions.

4.84 The signal f/n is derived from various input signals to the time base decades. The reference oscillator (10 MHz) is applied to the input of the time base decades in the Check, Frequency A, Period and Time Interval modes. Selection of the MULTIPLIER/TIME BASE switches determines the repetition rate of f/n. Frequency A is applied to the input in Period Average mode. Selection of the switches determines the number of periods of f_a to be measured before f/n is generated. Frequency B is applied to the input in Ratio and Time Interval Average modes. Selection of the switches selects the number of periods of f_b input to be counted before f/n is generated. Frequency A divided by

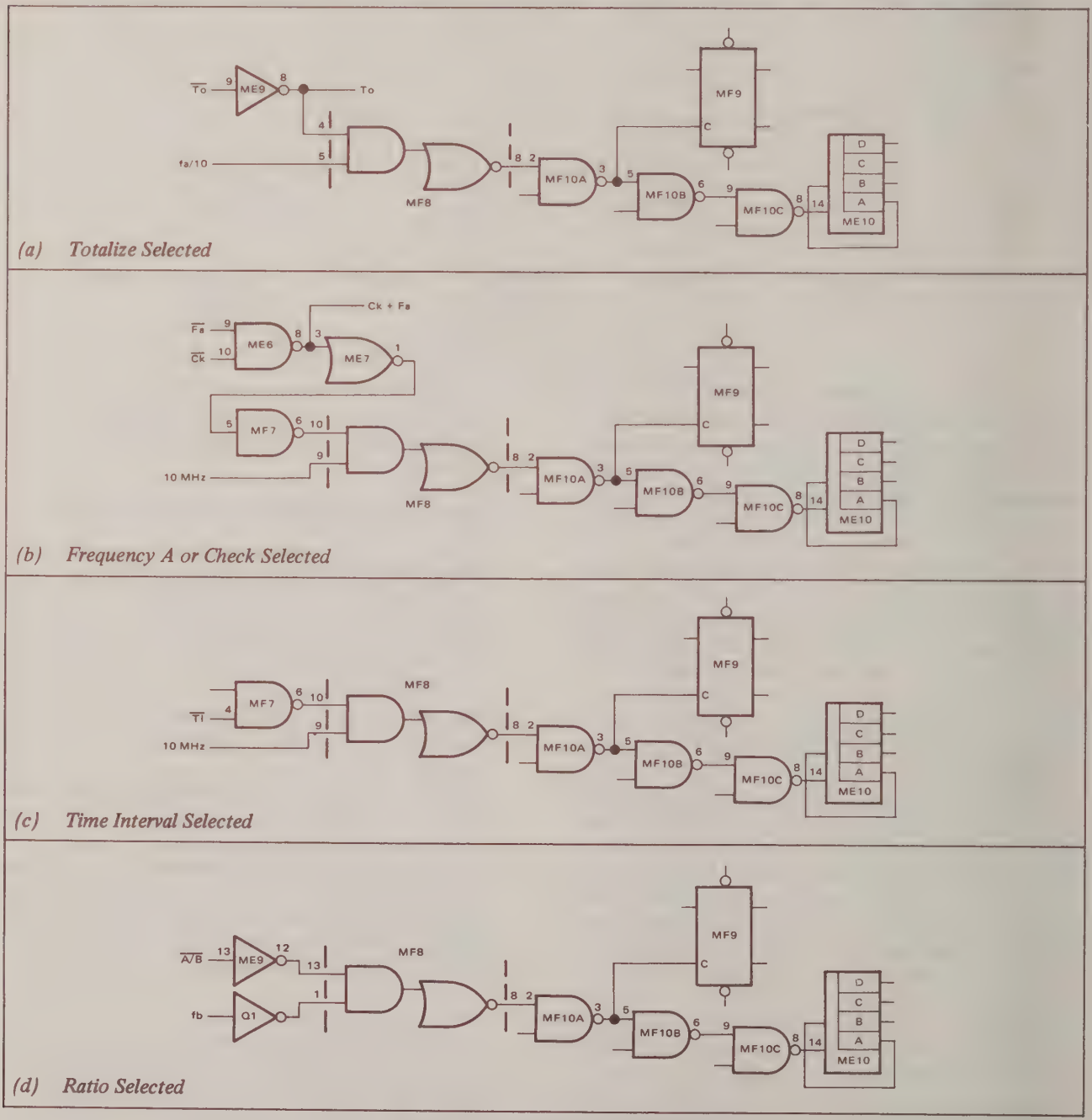


Figure 4.19 - Time Base Steering Logic

continued on page 4-13

ten (f_a/10) is applied to the input in the Totalize mode. Selection of the switches determines the scaling factor of f/n. The reference oscillator divided by four is applied to the time base decades in the Frequency C mode. Selection of the switches determines the repetition rate of f/n. Signal f/n is used for the start/stop pulses which establish the gate time.

4.85 TIME BASE STEERING LOGIC.

4.86 This circuitry routes signals to the time base divider circuit according to the measurement mode selected. Signal flow through the circuit is shown in figure 4.19a through h.

4.87 Totalize Mode.

4.88 Signal flow through the Time Base Steering logic in the Totalize Mode (figure 4.19a) is as follows. The Totalize mode is selected by the FUNCTION switch and $\overline{TO}$ is pulled to ground. $\overline{TO}$ is connected through inverter ME9 to an expandable 4-wide 2-input Nor gate, MF8. The output of MF8 is routed through Nand gates MF10A, and MF10C. The output of MF10C is applied to the clock input to the time base decades (MF9-14).

4.89 Frequency A or Check Mode.

4.90 Signal flow through the Time Base Steering logic in the Frequency A or Check mode is as follows (figure 4.19b). Frequency A or Check mode is selected by the FUNCTION switch which pulls one of the two lines $\overline{FA}$ or $\overline{Ck}$ to ground. These two lines are connected to Nand gate ME6. The output of ME6 (Ck + Fa) is connected to Nor gate ME7. The signal (Ck + Fa) is inverted through ME7. The output of ME7 is applied to Nand gate MF7. The output of MF7 is tied to pin 10 of a expandable 4-wide 2-input Nor gate MF8. The input of MF8 is high, thus enabling gate MF8. The 10 MHz reference, connected to pin 9 of MF8, passes on through MF10A, MF10B, MF10C, to the time base decades.

4.91 Time Interval Mode (Not in Model 8020B).

4.92 Signal flow through the Time Base Steering logic in the Time Interval mode is as follows (figure 4.19c). Time Interval is selected by the FUNCTION switch which pulls the TI line to ground. The $\overline{TI}$ line is connected to the input to Nand gate MF7. The other input, being high, causes the output of MF7 to be high. The output of MF7 is connected to one of two inputs to Nand gate MF8. The other input to MF8 is the 10 MHz reference. Since this gate is enabled, the 10 MHz reference passes through to MF10A, MF10B, MF10C, and to the time base decades.

4.93 Ratio Mode (Not in Model 8020B).

4.94 The signal flow through the Time Base Steering logic in Ratio mode is as follows (figure 4.19d). Ratio (A/B) is selected by the FUNCTION switch. The switch pulls the A/B line down to ground. The $\overline{A/B}$ line is routed to Inverter ME9. The output of ME9 is applied to pin 13 of MF8. The other input (pin 1) is tied to transistor Q1. When Q1 is on, pin 1 of MF8 is high and gate MF8 is enabled. The signal, f_b, passes through MF8 to MF10A, MF10B, and MF10C to the time base decades.

4.95 Time Interval Average Mode.

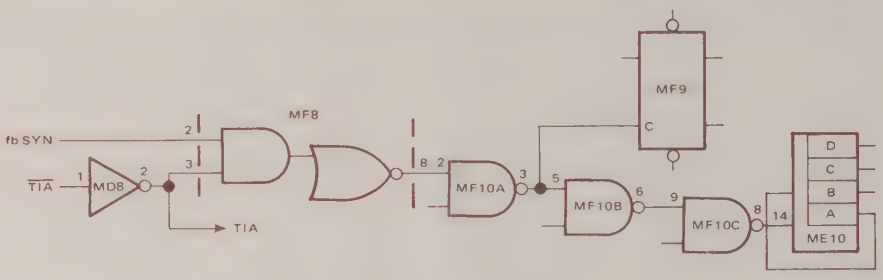
4.96 The signal flow through the Time Base Steering logic in the Time Interval Average mode is as follows (figure 4.19e). The Time Interval Average mode is selected by the FUNCTION switch which pulls the $\overline{TIA}$ line down to ground, the $\overline{TIA}$ line is connected to Inverter MD8. The output of MD8, is connected to pin 3 of MF8. The other input of MF8 pin 2 is connected to f_b SYN. With gate MF8 enabled, f_b SYN signal passes through MF8 to MF10A, MF10B, and MF10C to the time base decades.

4.97 Period Average Mode.

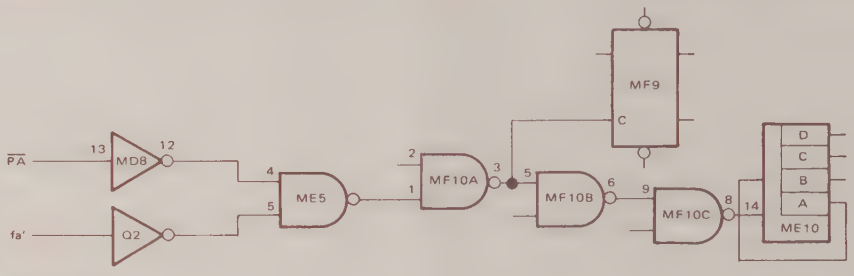
4.98 The signal flow for the Time Base Steering in Period Average mode is as follows (figure 4.19f). The Period Average mode is selected by the FUNCTION switch, which pulls the $\overline{PA}$ line low at the input of inverter MD8. The output of MD8 is connected to one input of Nand gate ME5. The other input of ME5 is connected to fa'. Signal fa' passes through ME5 to MF10A. Nand gate MF10A is enabled and fa' is applied to MF10B and MF10C, to the time base decades.

4.99 Frequency C and Period Modes.

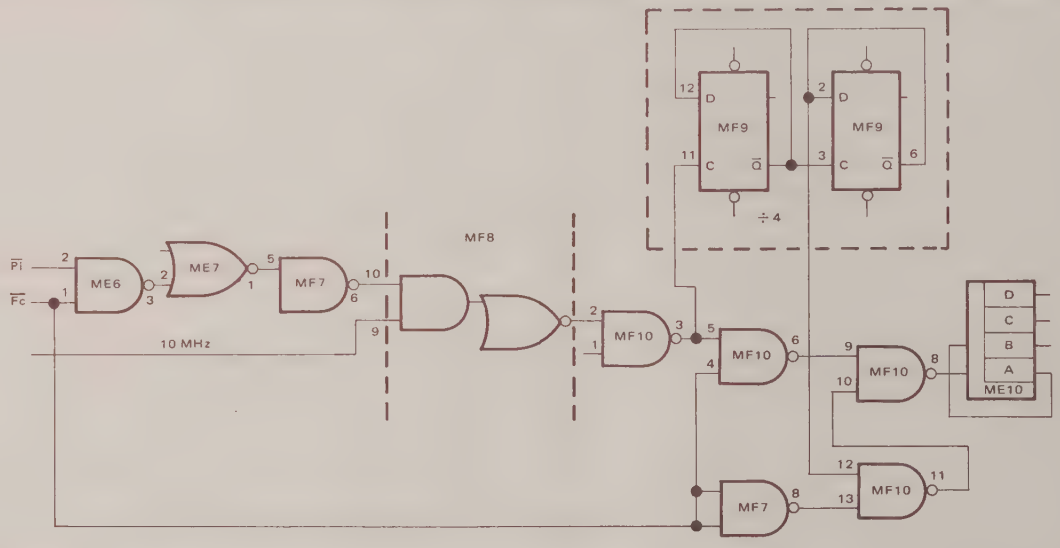
4.100 The signal flow for the Time Base Steering in Frequency C and Period modes is as follows (figure 4.19h). Frequency C or Period is selected by the FUNCTION switch. The FUNCTION switch pulls one of the two control lines, $\overline{Fc}$ or $\overline{Pi}$, low. Both lines are connected to Nand gate ME6. The output of ME6 is high and is connected to Nor gate ME7. The output of ME7 is connected to Nand gate MF7 and is low. The output of MF7 is connected to pin 10 of MF8 and is high. This enables the 10 MHz reference to pass through MF8 to Nand gate MF10A. The signal flow in the Period mode is from MF10A to MF10B, to MF10C, to the time base decades. The signal flow in Frequency C mode is from MF10A to a type D flip-flop, MF9, connected as a divide-by-four counter. The output of MF9 is applied through Nand gate MF10D to MF10C and to the time base decades.



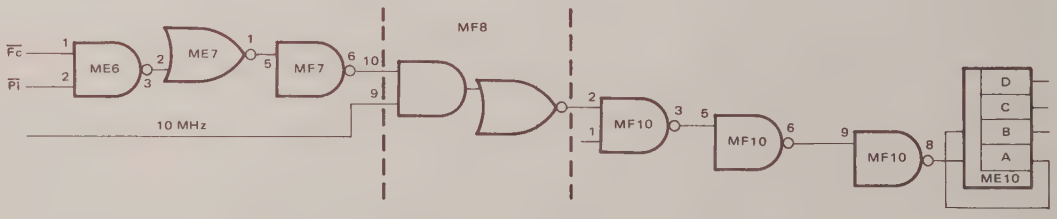
(e) Time Interval Average Selected



(f) Period Average Selected



(g) Frequency C Selected



(h) Period Selected

Figure 4.19 - Time Base Steering Logic

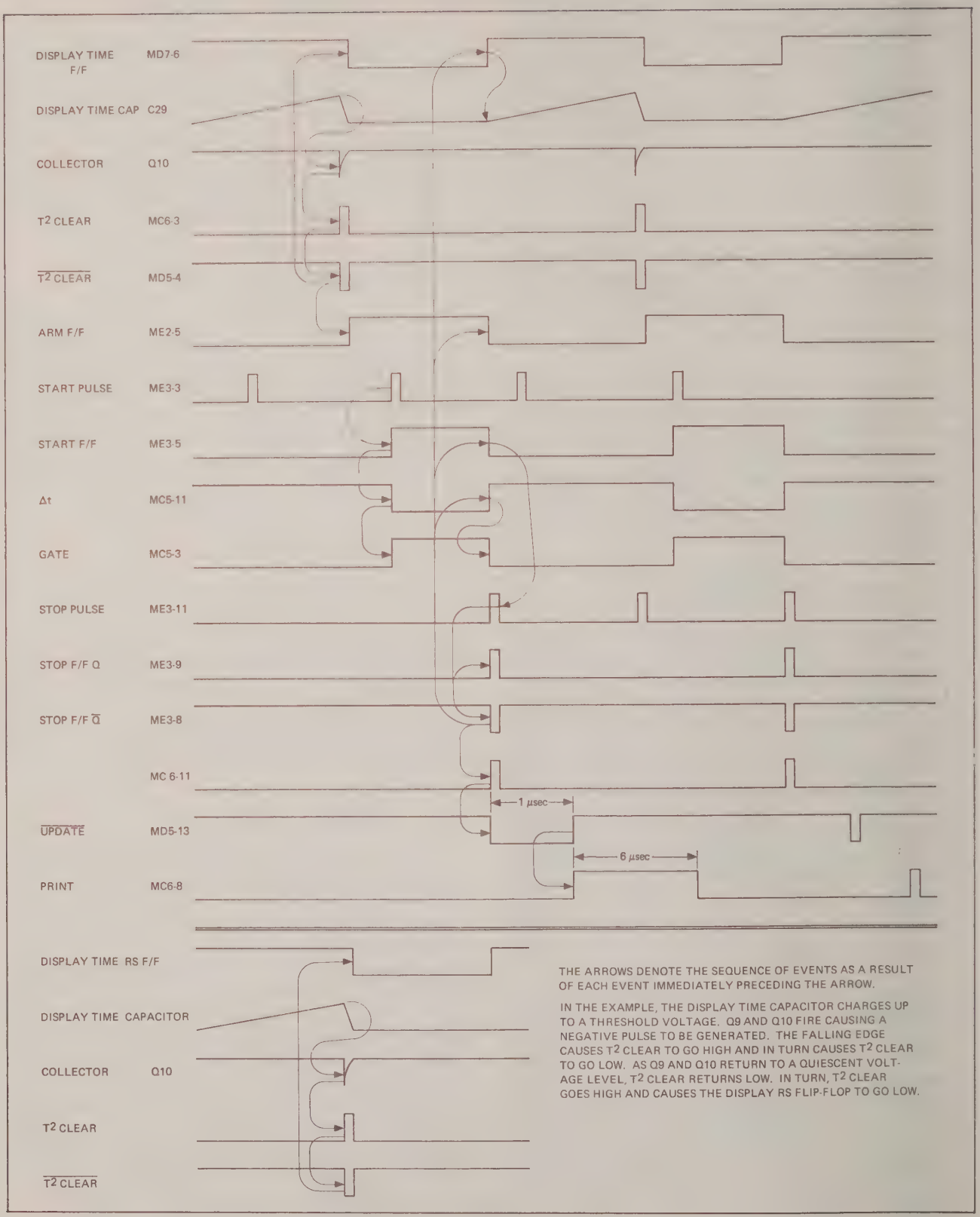

DISPLAY TIME F/F MD7-6
DISPLAY TIME CAP C29
COLLECTOR Q10
T2 CLEAR MC6-3
T2 CLEAR MD5-4
ARM F/F ME2-5
START PULSE ME3-3
START F/F ME3-5
Δt MC5-11
GATE MC5-3
STOP PULSE ME3-11
STOP F/F Q ME3-9
STOP F/F Q̄ ME3-8
MC 6-11
1 μsec
UPDATE MD5-13
6 μsec
PRINT MC6-8
DISPLAY TIME RS F/F
DISPLAY TIME CAPACITOR
COLLECTOR Q10
T2 CLEAR
T2 CLEAR
THE ARROWS DENOTE THE SEQUENCE OF EVENTS AS A RESULT OF EACH EVENT IMMEDIATELY PRECEDING THE ARROW.
IN THE EXAMPLE, THE DISPLAY TIME CAPACITOR CHARGES UP TO A THRESHOLD VOLTAGE. Q9 AND Q10 FIRE CAUSING A NEGATIVE PULSE TO BE GENERATED. THE FALLING EDGE CAUSES T2 CLEAR TO GO HIGH AND IN TURN CAUSES T2 CLEAR TO GO LOW. AS Q9 AND Q10 RETURN TO A QUIESCENT VOLTAGE LEVEL, T2 CLEAR RETURNS LOW. IN TURN, T2 CLEAR GOES HIGH AND CAUSES THE DISPLAY RS FLIP-FLOP TO GO LOW.

Figure 4.20 - Control Logic Timing

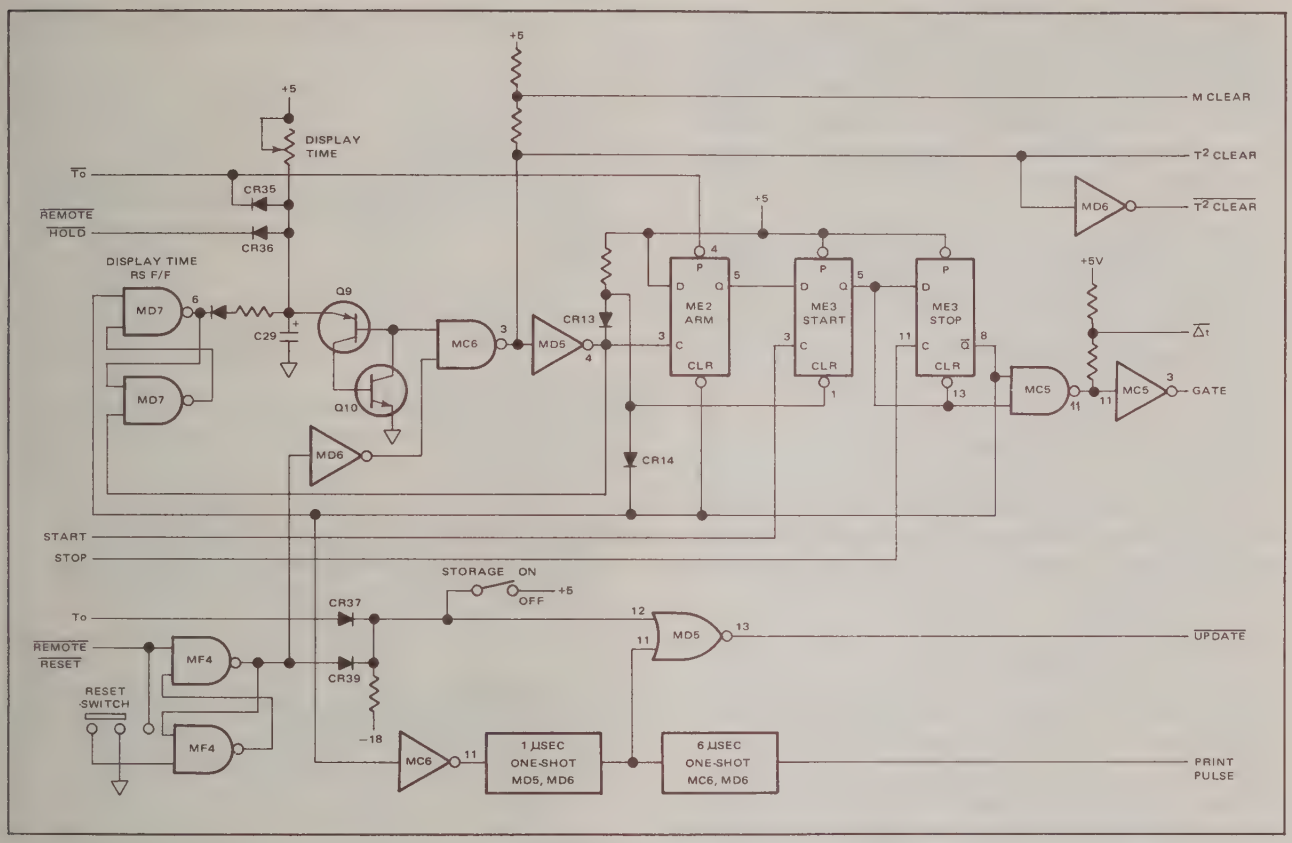


Figure 4.21 - Block Diagram Control Logic

4.101 CONTROL LOGIC.

4.102 This circuitry controls the timing sequence for the balance of the instrument; it generates the main gate control signal ($\overline{\Delta t}$). The timing sequence is illustrated in the timing diagram of figure 4.20, the circuitry is shown simplified in figure 4.21. With the DISPLAY TIME control set to produce periodic readings (not in the HOLD position), the operating sequence for all modes, except Totalize, begins when MD7-6 goes high. The display time integrating capacitor C29 charges at a rate dependent on the setting of the DISPLAY TIME control. When the voltage across C29 reaches approximately +3.7 volts, a latching circuit (Q9 and Q10) fires. Gate output MC6-3 goes high and inverter output MD5-4 goes low, resetting the display time RS flip-flop MD7. The voltage across C29 is discharged, Q9 and Q10 is reset, and MC6-3 goes low. From the previous reading, ME2-5 is low, ME3-5 is low and ME3-8 is high. An inverted T^2 CLEAR pulse (MC6-3), generated by the display time circuit, is fed to the clock input of a type D flip-flop ME2-3 and sets ARM (ME2-5) high on the trailing edge of the pulse. The instrument is now ready to measure. A START pulse to ME3-3 (clock) sets the Q output (ME3-5) high, causing $\overline{\Delta t}$ to go low (MC5-11) and MAIN GATE (MC5-3) to go high and enables STOP flip-flop so it will respond to the next STOP pulse.

4.103 When a STOP pulse is received at ME3-11 (clock), ME3-8 goes low causing $\overline{\Delta t}$ to go high and MAIN GATE to go low. The same ME3-8 signal is inverted and fires the 1-microsecond one-shot (MD5, MD6). The output of the one-shot is inverted through MD5 to produce the $\overline{\text{UPDATE}}$ pulse. At the same time, ME3-5 is reset low (through CR14 to ME3-1) which causes ME3-8 to reset high (through ME3-13). At the completion of the 1-microsecond one-shot, a 6-microsecond one-shot (MC6, MD6) fires. The output is inverted by MC6 to form the PRINT pulse used with Systems Interface, Option 008.

4.104 In the Totalize mode, the operation of the circuitry is the same with the following exceptions: the selection of Totalize sets MD5-12 true through CR37, causing MD5-13 to go false ($\overline{\text{UPDATE}}$). This allows the accumulation of pulses in the counter to be continuously monitored by the operator. Also, pin 4 of ME2 is held to ground, presetting Pin 5 of ME2 (ARM) to high and the display time circuit is disabled through CR35. The Start/Stop pulses are generated manually by the START/STOP switch on the front panel or

electrically through the external gate line (EXT. GATE) and perform the same function as the internally generated pulses in the other measurement modes. However, since the ARM line is held high as long as the instrument is in the Totalize mode, the Totalize measurement may be started and stopped as many times as desired.

4.105 The reset circuit (MF4) is used to reset the Counting Decades. In REMOTE HOLD, for modes other than Totalize, the reset commands a new reading.

4.106 START/STOP LOGIC.

4.107 The Start/Stop logic generates the Start and Stop pulses used by the control logic to control the main gate. The Start pulse is used to set the Start flip-flop (in the control logic) which initiates the gate. The Stop pulse sets the Stop flip-flop. The output of the Stop flip-flop terminates the gate. The routing of the signals is shown in figure 4.22a through e.

4.108 Totalize Mode (figure 4.22a).

4.109 In the Totalize mode the start pulse is initiated by the START/STOP switch or by the external gate line pulled to common. The START/STOP switch and the external gate lines are tied to the input of an RS flip-flop (MF4) made from two cross-coupled nand gates. The output of the flip-flop is low when the START/STOP switch is not depressed. When the switch is depressed, the inhibit is removed and the flip-flop output goes high. The output stays high as long as the switch is depressed or the external gate line is pulled to common. The output of the flip-flop is tied to inverter MF3. The output of the inverter is connected to two four-input nand gates. The gate is initiated on the first Start/Stop command and terminated on the second.

4.110 Period Mode (figure 4.22b).

4.111 In the Period mode, the $\overline{Pi}$ line is low causing the output of inverter MD6 to enable nand gate MF6. The rising edges of f_{aT} (frequency A at TTL level), produces Start and Stop pulses for the control logic.

4.112 Time Interval Mode (figure 4.22c).

4.113 In the Time Interval mode, the $\overline{TI}$ line is low. $\overline{TI}$ is inverted through ME6-6 which enables Nand gates MF6-6 and MF6-8. When Frequency A triggers and f_{aT} rises, it causes the output of MF6-6 to go low. This causes a Start to be generated at the output of ME4. When Frequency B triggers and f_{bT} rises, it causes the output of MF6-8 to go low. This causes a Stop to be generated at the output of ME4-8.

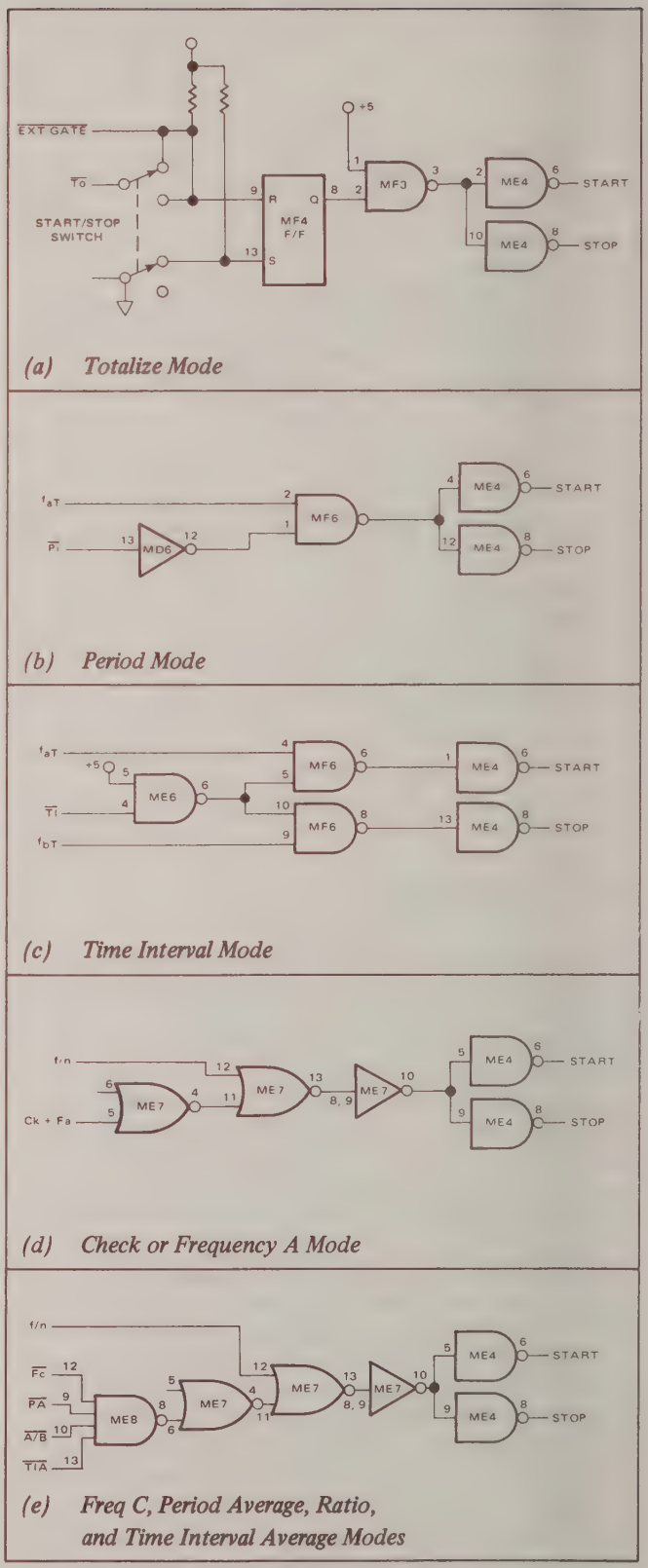


Figure 4.22 - Start/Stop Signal Flow

4.114 Check or Frequency A Mode (figure 4.22d).

4.115 In the Check or Frequency A mode, Ck + Fa is high and is connected to Nor gate ME7-5. The other input to ME7-6 is low. The output of ME7-4 is low and is connected to Nor gate ME7-11. The other input to ME7-12 is connected to the scaled output (f/n). The scaled output is the reference oscillator frequency divided by the time base decade selection.

4.116 Frequency C, Period Average, Ratio, and Time Interval Average Modes (figure 4.22e).

4.117 In the Frequency C, Period Average, Ratio, and Time Interval Average modes, one of the inputs ($\overline{Fc}$, $\overline{PA}$, $\overline{A/B}$, $\overline{TIA}$) to Nand gate ME8 is selected and pulled low. The output of ME8-8 goes high and Nor gate ME7-4 goes low enabling Nor gate ME7-13. The gate is initiated when f/n goes low via the Start pulse at ME4-6. The next time f/n goes low the gate is terminated via the Stop pulse at ME4-8.

4.118 MARKER LOGIC (figure 4.23).

4.119 The MARKER output provides a negative 18-volt pulse starting when channel A triggers and stopping when B triggers. It is used for increasing the intensity of an oscilloscope trace.

4.120 The circuit consists of two D-type flip-flops (ME1) driving a voltage level shift circuit (Q16, Q17). Channel A input (f_aT) sets ME1-6 low causing Q16 to turn off. In turn, Q17 turns off producing a −18 volt output at the collector of Q17. A trigger from the channel B input (f_bT) sets the second half of ME1. Q resets ME1-6 high causing transistors Q16 and Q17 to saturate and producing a collector output of about zero volts for the marker output at J103.

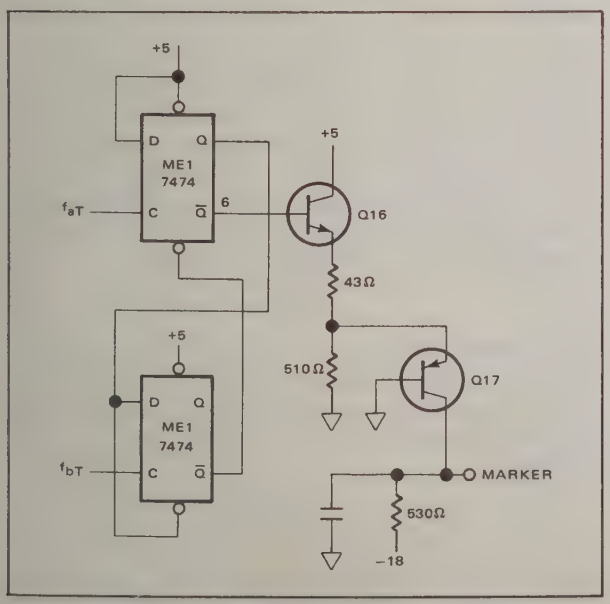


Figure 4.23 - Marker Logic (Not on 8020B)

4.121 Readout Board.

4.122 The readout board assembly is one of two large printed circuit boards mounted to the base plate. The readout board is accessible from the top of the counter. The readout board contains the following circuits; the reference oscillator, the power supply, the function switch, the display tubes, the TTL counting decades, and the storage.

4.123 COUNTER/DISPLAY.

4.124 The counter and display circuit counts, stores and displays the number of pulses received from the high-speed decade on the switch board. The counter consists of seven decade counters (type 7490), eight quadruple bistable latches (type 7475), eight numeric display tube drivers (type 7441), and eight numeric display tubes. An additional tube, driver, latch, and decade are included in instruments having the 9th digit, Option 004. Transistor Q1 controls the update inputs of all the quad latches. A low update signal from the control logic allows each latch to assume the same level as the decade counter to which it is connected. A high update signal allows the latches to store the information. The $\overline{T^2\ CLEAR}$ line (when low) resets the decade counters to zero.

4.125 POWER SUPPLY.

4.126 The power supply (figure 4.24) provides all voltage levels for the operation of the instruments and standby power (with power OFF selected) for the continuous operation of the optional frequency source (with instruments equipped with Option 200). All supplies except the +150 volt supply are regulated.

4.127 The +150V supply is used by the gas tube display and derived from a +250 volt full wave bridge circuit. Current limiting resistor R60 drops the voltage to the tubes to approximately +150 volts when the tubes are conducting. With power OFF, the +150 line is opened.

4.128 The +28 volt supply is used only for the optional frequency reference (Option 200) and is derived from a tapped secondary full wave rectified circuit and discrete 28-volt regulator.

4.129 The −18-volt supply is used throughout the instrument and is derived from a −28 volt full wave rectified supply and a regulator consisting of zener CR20 and transistors Q26 and Q101. Referring to the schematic, Q26 and

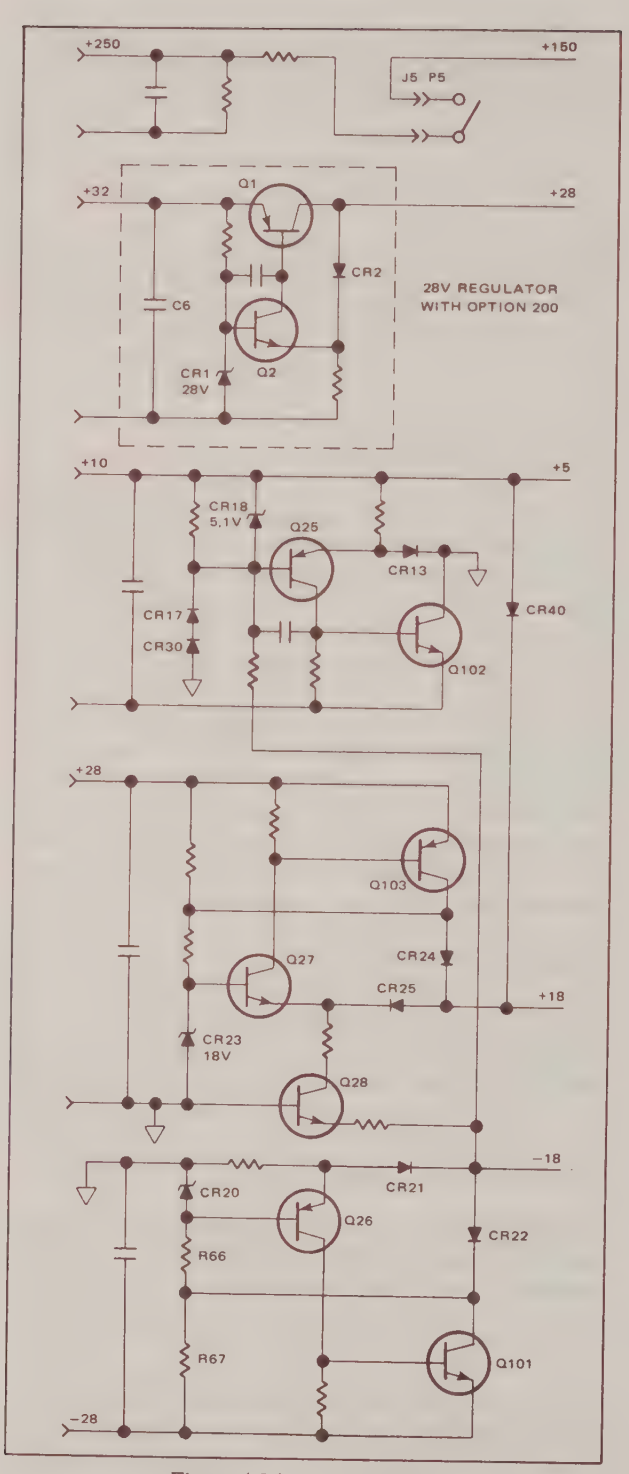


Figure 4.24 - Power Supply

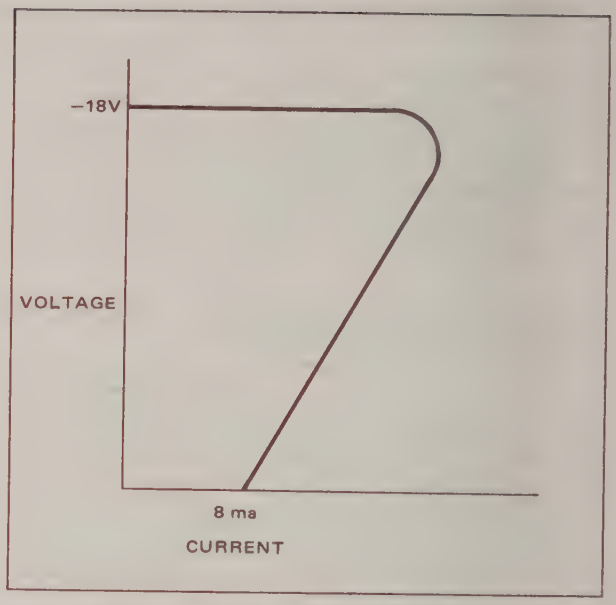


Figure 4.25 - Characteristic of −18V Regulator

CR20 (18 volt zener) form a 12 milliamp current generator with resistors R66 and R67 supplying current to the zener. The base of Q101 is driven by the current generator causing Q101 to conduct heavily pulling the output towards −28 volts through diode CR22. At −18 volts, diode CR21 starts conducting causing the current generator to lessen the output and at this point stability is reached. When the power switch is set to OFF the −18 volt supply is shorted to ground. The voltage at the cathode of CR22 turns off Q26 by depriving CR20 of idling current and the short circuit current folds back to approximately 8 ma as shown in figure 4.25.

4.130 The +18 volt supply is also used throughout the instrument and is derived from a +28 full wave rectified circuit. The regulator circuit, consisting of transistors Q27, Q28, Q103, and 18 volt zener CR23, operates in the same manner as the −18 volt supply. Transistor Q28 functions as a switch and turns off the +18 supply when the −18 volt supply goes to ground (instrument is shut off).

4.131 The +5 volt supply is used by all of the digital circuitry. The regulator operates in the same manner as the ±18 volt supplies but uses a 5-volt zener. The current for the zener is supplied through resistor R63 from the −18 volt supply.

SECTION 5 MAINTENANCE

5.1 INTRODUCTION.

5.2 This section contains maintenance information for the counter. Included are TTL theory, ECL theory, diode gate theory, signal flow in all modes of operation, troubleshooting, and diagrams to localize, isolate and locate defective components. Performance check procedures are not included in this section, but can be found in Section 3.

5.3 RECOMMENDED TEST EQUIPMENT.

5.4 Test equipment recommended for maintaining, troubleshooting, and servicing the counter is listed in table 5.1. Test equipment with equivalent characteristics may be substituted for equipment listed.

5.5 CALIBRATION.

5.6 Internal Reference Oscillator Adjustment.

5.7 The following procedures are given for adjustment of the counter's internal reference oscillator. One of three different reference oscillators may be used in the counter. The reference oscillators are as follows:

a. Standard Temperature-Compensated Crystal Oscillator (TCXO); Dana part number 730551

b. Option 050 Temperature-Compensated Crystal Oscillator (TCXO); Dana part number 730578

c. Option 200 Temperature-Compensated Reference Oscillator (TCRO); Dana part number 730228

5.8 For standard and option 050 reference oscillators, perform the following set-up procedures.

a. Set the counter controls as follows:

Control	Setting
DISPLAY TIME	about 9 o'clock
FUNCTION	FREQ A
TIMEBASE	10 second
A Slope	Plus (+)
A Coupling	DC
A Trigger Level	PRESET
SEP/COM	SEP
STORAGE	ON
REF	INT OUT
A Input Voltage Range	10

Table 5.1 - Required Equipment

Instrument Type	Required Specification	Recommended Instruments
Frequency Standard	1 MHz, 5 MHz, or 10 MHz	
Oscilloscope	150 MHz Bandwidth 500 MHz Bandwidth	TEK 454 TEK 7900
Voltmeter	10 mVDC to 200 VDC	Dana 4300
Sine Wave Generator	2 Hz – 10 MHz	Dana 7010
VHF Signal Generator	10 – 150 MHz	HP8654A
VHF Signal Generator	1 – 550 MHz (Not required for 8010B)	HP8654A
Pulse Generator	4 ns pulsewidth	Datapulse 112
Alignment Tool	.075" Hex (nonmetallic)	General Cement 9300
Alignment Tool	Blade (nonmetallic)	
Sampling Voltmeter	0 – 600 MHz	HP3406
BNC "T" connector		
50Ω Tee connector		HP 10221A
2 – BNC to GR Adaptors		

b. Connect a 1 MHz frequency standard to A input.

c. Allow 1 hour time for the counter temperature to stabilize.

d. The difference between the internal reference oscillator and the 1 MHz frequency standard can be determined by the following formula:

Internal Oscillator Frequency = (20,000,000 – Counter Reading). See table 5.2.

Table 5.2 - Reference Oscillator Error

Counter Display	Internal Reference Osc.
999.9950 kHz	10000.050 kHz
999.9975 kHz	10000.025 kHz
1000.0000 kHz	10000.000 kHz
1000.0025 kHz	9999.975 kHz
1000.0050 kHz	9999.950 kHz

5.9 ADJUSTMENT PROCEDURE – STANDARD TCXO.

a. Apply power to the counter for one hour before attempting TCXO adjustment (see paragraph 5.8). Remove the top cover (see paragraph 5.18, "Access to P.C. Boards"). Locate the TCXO located on the Readout assembly near the rear of the counter (see figure 6.5, Readout Layout). Remove the #6 metal or nylon cap screw on the top of the reference oscillator. Use a nonmetallic alignment tool for adjustment. Some oscillators require a hexagon .075 dia. alignment tool, and others require a blade type.

b. Insert the proper adjustment tool into the #6 screw hole on the top of the reference oscillator. Adjust the TCXO until the display reads 1000.0000 kHz. Wait ten seconds and readjust the TCXO if the first adjustment was not correct. Remove the adjustment tool.

c. After the initial adjustment, replace the cap screw and the top cover. Allow 30 minutes for temperature stabilization and recheck the reading.

5.10 ADJUSTMENT PROCEDURE – OPTION 050 TCXO.

5.11 Allow the counter to temperature stabilize for one hour before adjustment and verify one hour after adjustment. Follow the procedures outlined in paragraph 5.9.

5.12 ADJUSTMENT PROCEDURE – OPTION 200 TCRO.

5.13 The object of the following procedures is to determine short term drift of the TCRO as well as to adjust the frequency. The adjustments are the COARSE and FINE controls on the rear panel. *Use only a non-metallic blade type adjustment tool for these adjustments.*

a. Set the counter controls as described in paragraph 5.8a.

b. Allow the counter to temperature stabilize for 72 hours before calibration. (It is not necessary to turn the power on during the warmup and stabilization period. The TCRO is an oven oscillator which operates from a separate +28 volt supply.) Set DISPLAY TIME to about 9 o'clock one hour before adjustment.

c. Connect a 1 or 5 MHz Frequency Standard to channel 1 of a dual channel oscilloscope. Trigger the oscilloscope on channel 1 only. Set the oscilloscope sweep rate to .02 μs per cm.

d. Connect a BNC cable to the counter INT OUT connector J106 on the rear panel. Set the REF switch S102 to the INT OUT position. Connect the other end of the BNC cable to the second channel of the oscilloscope. The oscilloscope display should indicate a stationary and a moving waveform. The moving waveform is the counter reference oscillator.

e. Remove the nylon cap screws. Adjust the COARSE adjustment (rear panel, see figure 6.8) and then the FINE adjustment until as near a completely stable waveform as possible is obtained. The channel 2 waveform will be drifting to the left or right. If the channel 2 waveform is moving to the left, the internal reference oscillator is higher in frequency than the frequency standard. If the channel 2 waveform moves to the right, the internal reference oscillator is lower in frequency than the frequency standard.

f. To determine the drift rate, measure the time it takes the oscilloscope pattern to drift the width of one cycle on channel 2. Note: 1 cycle equals 5 divisions on the oscilloscope. The oscillator drift can be determined from figure 5.1.

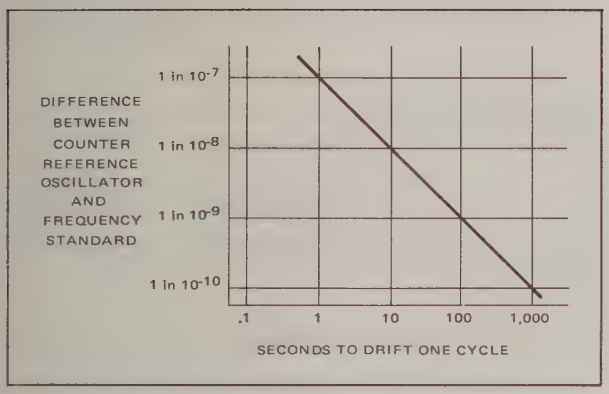


Figure 5.1 - Oscillator Drift

5.14 SIGNAL CONDITIONING CALIBRATION – CHANNEL A.

a. Set the controls as follows:

Control	Setting
A Slope	(+) Plus
A Coupling	AC
MULTIPLIER/TIMEBASE	1 second
A Trigger Level	PRESET
A Voltage Input Range	1
SEP/COM	SEP
FUNCTION	FREQ A
DISPLAY TIME	about 9 o'clock

b. Apply power to the counter 1 hour before adjustment. Do not remove the top or bottom covers during warmup.

c. Apply a 10 MHz 100 mV rms signal to channel A input. Use a DC coupled oscilloscope with .5V/cm sensitivity to compare logic levels at MD1-12 and MD2-8 on the switch board assembly. Refer to figure 6.3, Switch Board Layout, for locations.

d. Adjust the ECL level pot R17A (figures 5.3 and 6.1) so the logic levels at MD1-12 are the same as the logic levels at MD2-8.

e. Connect a 150 MHz, 40 mV RMS signal to channel A input.

f. While observing the signal at MD1-12, switch the channel A slope between (+) plus and minus (–). Note the DC voltage shift between + and – slopes. Adjust the offset pot R20A for a minimum DC shift. Notice that with no DC shift, a permissible change in peak-to-peak amplitude may occur. The signal at MD1-12 is shown in figure 5.2. The signal output in either slope must be a minimum of .4 volts peak-to-peak.

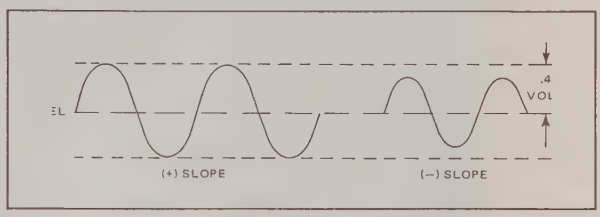


Figure 5.2 - Signal Conditioner Output

h. Check the sensitivity over the band in both + and – slopes. Nominal sensitivities are as follows:

50 mV RMS to 100 MHz, 100 mV RMS to 150 MHz.

g. Place channel A in – slope. Increase signal level to insure that the proper reading is displayed by counter. Incrementally decrease input signal level until an improper reading is observed. Then adjust R17A for the correct reading. Continue this process until maximum sensitivity is obtained.

i. Final check and adjustment should be completed after the unit is at ambient temperature with the top and bottom covers on.

5.15 SIGNAL CONDITIONING CALIBRATION – CHANNEL B (Not in 8020B).

a. Set the Controls as follows:

Control	Setting
Slope A	+
Slope B	–
Coupling A	AC
Coupling B	AC
Trigger Level A	PRESET
Trigger Level B	PRESET
Input Range A	1
Input Range B	1
SEP/COM	SEP
FUNCTION	TIA
DISPLAY TIME	about 9 o'clock
MULTIPLIER/TIMEBASE	1 second

b. Apply power to the counter 1 hour before adjustment. Do not remove top and bottom covers during warmup period.

c. Apply a 10 MHz 100 mV rms signal to channel A input. Apply the same signal to a 10 dB Attenuator. Connect the output of the attenuator to channel B input.

d. Monitor the signal output of signal conditioner at ME0-6 on the Switch Board assembly. (figure 6.3)

e. Use a DC coupled oscilloscope with .5V/cm sensitivity and compare logic levels at ME0-6 and MC1-8 on the Switch board.

f. Adjust the ECL level control R17 (figures 5.3 and 6.1) such that the logic levels at ME0-6 are the same as the logic levels at MC1-8.

g. Incrementally decrease input signal level until an improper reading is observed. Then adjust R20 for the correct reading. Continue this process until maximum sensitivity is obtained.

h. Check the sensitivity over the band in both + and – slopes. Nominal sensitivities are: 0 – 10 MHz, 50 mV RMS.

i. Final check and adjustments should be completed after the counter is at ambient temperature with both top and bottom covers on.

5.16 PERIODIC MAINTENANCE.

5.17 To determine if the counter is operating properly within specifications, perform the performance check (Section 3).

5.18 ACCESS TO PC BOARDS.

5.19 To remove top and bottom covers, proceed as follows:

a. Remove power cord.

> **NOTE**
>
> The power supplies are still active as long as the power cord is plugged into the power AC source.

b. Loosen the four captive screws, one at each corner of the top cover and remove the top cover.

c. Turn the counter upside down. Loosen the four captive screws on the bottom cover and remove the bottom cover.

5.20 PCB REMOVAL.

5.21 When removing the printed circuit board for replacement, repair, and servicing, always remove the AC power cord before disassembly. Refer to figure 5.23, page 5-15 for assembly location.

5.22 RF Assembly (figure 6.12 or 6.14).

a. Remove the six #4 phillips-head screws around the outer edge of the assembly.

b. Disconnect the two subminiature RF connectors.

c. Disconnect P10 at the rear of the counter.

d. On instruments having option 030, remove the five #4 screws holding the RF shield on the component side. Remove shield.

> **NOTE**
>
> The R.F. assembly is very sensitive to component movement. Do not move any components or recalibration will be necessary.

5.23 Signal Conditioning Assembly (figure 6.1).

a. Remove the trigger level knobs and the input range knobs.

b. Remove the two #6 phillips-head screws on the top of the signal conditioner and one #6 phillips-head screw on the bottom.

c. Remove the subminiature R.F. connectors.

d. Remove the two #6 phillips-head screws holding cable clamps on the cable between the signal conditioner and P9. Remove P9 and remove the assembly.

e. To service the attenuator switch, remove the four #4 phillips-head screws located at each corner of the printed circuit board. The printed circuit board can be moved away from the switch assembly for servicing.

5.24 Readout Assembly (figure 6.5).

a. Remove the interconnection printed circuit assembly from J4.

b. Remove P1 at the left rear of the assembly.

c. Remove P5 and the FUNCTION knob at the right front side.

d. Remove the seven #6 phillips-head screws (one in the center and six around the perimeter of the board). The Readout assembly can now be removed.

5.25 Switch Board Assembly (figure 6.3).

a. Remove the interconnection printed circuit assembly from J2.

b. Unscrew the subminiature RF connectors from the Signal Conditioning assembly and the RF assembly.

c. Remove P3 from J3.

d. Remove the six #6 phillips-head screws, two in the center and four around the perimeter of the printed circuit board. Remove the switch board assembly.

5.26 COMPONENT REPLACEMENT.

5.27 When replacing a circuit board component, use a low heat soldering iron (25 watt). Heat must be used sparingly as damage to the circuit foil may result. Plated-thru holes may be cleaned with a solder remover while heat is applied. The connection should be cleaned with a cleaning solution after the component removal and replacement.

5.28 Integrated Circuit Replacement.

5.29 Integrated circuits can be unplugged and substituted without soldering or assembly removal. The use of special tools to remove IC is not recommended. To remove an IC, place both thumbs on top of the IC and both index fingers at the ends of the IC. Gently rock the IC upward in small steps. Do not "pop" it out in one motion. To replace an IC, be sure the notched end points the same direction as the other ICs on the board. Straighten any bent pins. Align the pins on the IC with the holes in the socket and press the IC in firmly using one or two fingers.

5.30 Identification of Parts.

5.31 All parts are listed in the parts list, Section 7, by assembly. Reference designators are called out on the schematic and can be found on the layout drawings. The Dana part number and description are given in the parts list. All integrated circuits used in the counters are standard 7400 series TTL and ECL that can be purchased from your local supplier. Special parts may be obtained from Dana by writing or calling Product Service at 714-833-1234 collect in California.

5.32 Parts Location.

5.33 The integrated circuits on the Readout and Switch board assemblies are layed out on a grid pattern. Looking at the readout or switch board from the front, the ICs are numbered across the board from left to right, 1 through 12; top to bottom, A through F. Other components are designated by circuit and can be located by the schematic and layout drawing.

5.34 TROUBLESHOOTING.

5.35 This section describes methods for identifying counter troubles and determining the specific corrective action that should be taken. Familiarity with the Operation (Section 3) and Theory of Operation (Section 4) makes troubleshooting easier.

5.36 A malfunction can be rapidly defined to one of four categories.

a. Apparent trouble which is really a misplaced control setting or an erratic external signal.

b. Visual damage such as printed circuit board broken, etc.

c. Analog trouble which requires troubleshooting and component replacement.

d. Digital trouble which requires troubleshooting and IC replacement.

5.37 Repairs which require replacement of soldered-in components can be accomplished rapidly, but caution should be taken against soldering with improper procedures. Solder damage to the printed circuit boards is not covered by Dana's warranty.

5.38 Apparent Troubles.

5.39 Apparent troubles are those which appear to be equipment malfunctions, but are really controls which are misadjusted.

5.40 The counter will not operate if a function is incorrectly selected. For instance, if the unknown frequency is connected to input C and FREQ A function is selected, there will be no reading. Be sure the FUNCTION switch is in the proper mode. If the function has been changed, depress RESET to start a new reading in the new function.

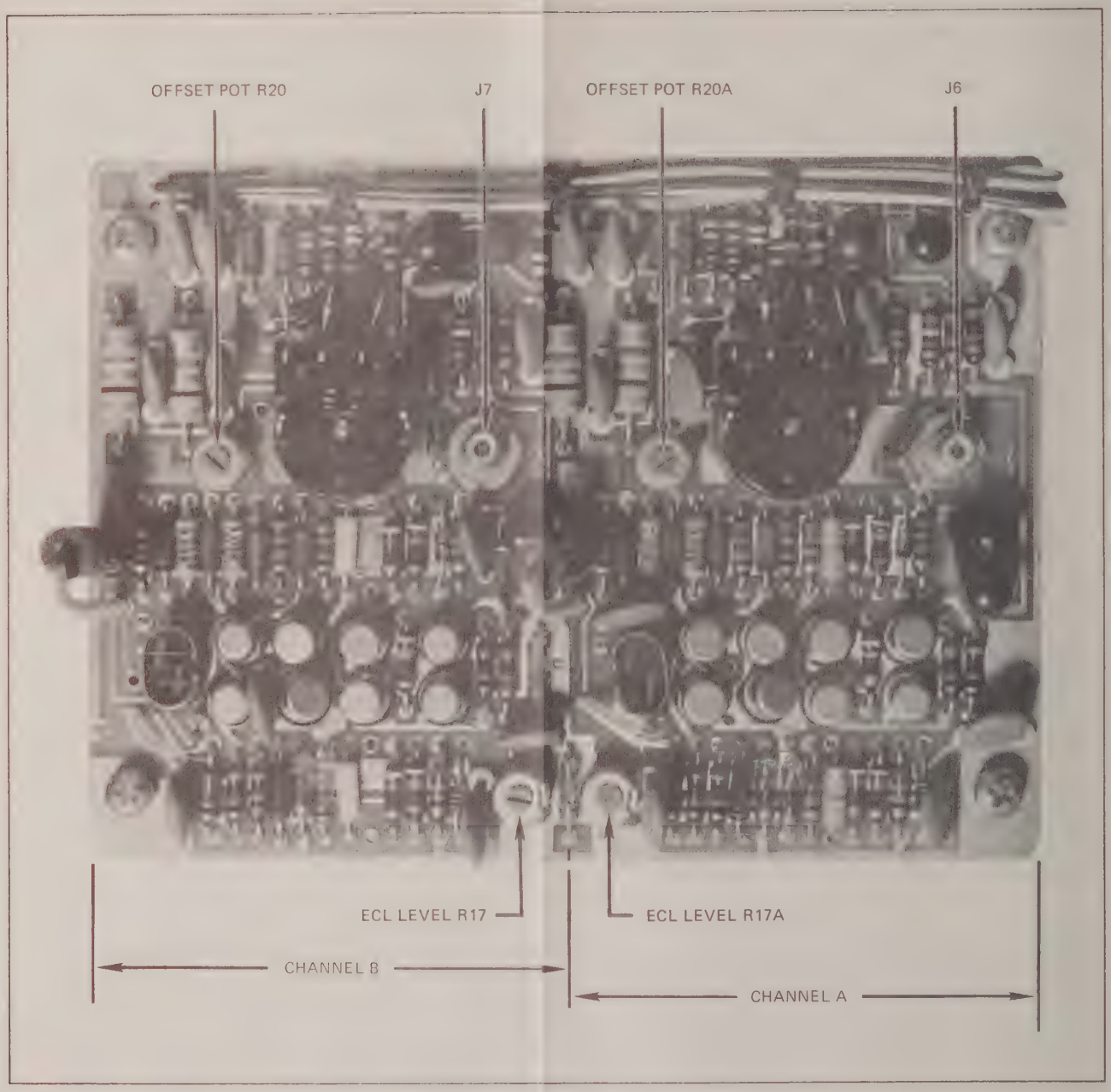


Figure 5.3 - Signal Conditioning Adjustments

Table 5.3 - Front Panel Symptoms

Type of Problem	Refer to Paragraph:
Readout	5.49
Remote Operation	5.64
Self-Check Mode	5.68
Frequency A Mode	5.70
Period Mode	5.73
Period Average Mode	5.75
Frequency C (Not in 8010B)	5.77
Totalize Mode	5.80
Time Interval Mode (Not in 8020B)	5.82
A/B (Ratio) Mode (Not in 8020B)	5.85
Time Interval Average Mode (Not in 8020B)	5.88

5.41 If the input voltage range or trigger level are improperly set, inputs A or B will not operate. Be sure that a measurable signal is present and that controls are set properly for that signal.

5.42 When input C is used (not in 8010B), the automatic gain control will inhibit readings of signals which are less than 50 mV and greater than 1V RMS. Signals will be inhibited if they are outside the measurable band (1.0 MHz to 550 MHz). With Option 030, the automatic gain control will inhibit readings of signals which are less than 1 mV and greater than 1V RMS. Signals will be inhibited if they are outside the measurable band for Option 030 (10 MHz to 500 MHz).

5.43 Due to the sensitivity of input C, open leads which might act as an antenna can cause improper readings. If open leads or probes must be used, it may be necessary to insert a low-pass filter at the counter input to discriminate against unwanted signals received through radiation. Unshielded input signals can cause unwanted signals to override the desired signal. The proper operation of input C can be verified by connecting a signal generator directly to the counter through a shielded 50-ohm terminated cable. Once proper counter operation has been verified, unwanted external signals can be attenuated with a low-phase filter.

5.44 Visual Check.

5.45 A possible source of malfunction could be short or open circuits which disable portions of the counter or load down the power supply, or both. Often these short-circuits can be located by visual inspection. A quick visual check of the counter with the covers removed may reveal foreign metal parts, frayed cable braid, discolored components, etc. which can be easily corrected. Visual checks can be more meaningful after the trouble has been localized.

5.46 Open circuits can also be located visually. Examine connector and wire harnesses for obvious breakage or opens.

5.47 Front Panel Symptoms.

5.48 Localize the trouble to one of the categories listed in table 5.3; then proceed to the appropriate paragraph and follow the suggested procedure.

5.49 READOUT INOPERATIVE.

5.50 If the readout tubes and annunciators do not light, a failure in the 150V supply is indicated. Check the line fuse. It should be .75 amp, 3 AG. If in doubt, measure the AC source at the power transformer T101 to assure that power is getting to the counter. Check the 150-volt supply as follows.

a. Turn power off; remove the power cord at the rear of the counter. The supplies are still active even with the power switch turned off. Remove the top cover and reconnect the power cord.

b. Connect a voltmeter to either side of resistor R60, 3.9K, 3W (figure 6.5). Connect the other lead of the voltmeter to ground (negative side of capacitor C7). The voltage should read about 150 volts DC.

c. Note the action that occurs when the DISPLAY TIME switch is moved clockwise from the PWR OFF position. If the voltage goes very low or to zero, there is a short in the 150V line. If no voltage is present at either side of R60, check the following: R61 (located under C6), C5, CR5 through CR8, and T101.

d. Remove P1 and check for 180 volts RMS AC at points P1-E (blue transformer lead) and P1-D (violet transformer lead).

e. If the high voltage is still not present, check the wire harness for opens or shorts. If no opens or shorts are found, T101 may be defective.

f. If the high voltage is present, reconnect P1 and recheck the 150 volt lines. If the 150 line loads down, locate and eliminate the short on the readout board.

5.51 READOUT TUBE BLURRING.

5.52 If all readout tubes blur, a faulty +5-volt supply voltage is indicated. The 5-volt supply is affected by the other power supplies, so they must all be checked.

5.53 Series regulator transistors for the +5-volt and ±18-volt supplies are mounted on a heatsink on the rear panel. A short to ground in the −18-volt supply turns off the +5-volt and +18-volt supplies. Instruments equipped with Option 200 have a separate +28-volt supply and regulator. A short in this supply also affects the other voltages. It can be measured at J4-X.

5.54 Check the power supply voltages at the points listed below. Refer to figure 6.6 for voltage levels within the power supply.

Power Supply	Measurement Point (figure 6.5)
+5V	J4-20 or CR40 anode
+18V	Cathode of CR40
−18V	Anode of CR22

5.55 If any of the power supply voltages are abnormal, disconnect the load to isolate the trouble to the supply or to the load. If the voltage returns to normal, reconnect the load and selectively unplug the interconnection board, the signal conditioning board, and the prescaler until the source of the overload is located.

5.56 If the trouble appears in only one readout tube, a bad integrated circuit (IC) driver or a bad readout tube is indicated. Driver IC's are 7441's in Row F directly behind the readout tubes. Remove power, and exchange the 7441 behind the bad readout with the neighboring driver. If the trouble moves with the driver (7441), replace the 7441 driver. If the trouble stays when the driver is moved, replace the readout tube. If none of the above solves the problem, inspect the circuit near the tube, driver, or quad latch (7475) for shorts or opens.

5.57 ANNUNCIATORS INOPERATIVE.

5.58 The "gate" and units annunciators are located in front of and below the readout tubes (figure 6.5). They are operated from the +150-volt and +5-volt power supplies. If none of the annunciators light, the power supply is probably faulty. Perform the power supply checkout procedures described in paragraph 5.49.

5.59 If the GATE annunciator does not operate, proceed as follows:

a. Set DISPLAY TIME counterclockwise, just short of the PWR OFF position.

b. Set FUNCTION switch to the CHECK mode.

c. Depress the 100 ms TIMEBASE switch (the GATE light should flash at approximately 130 ms intervals).

d. With an oscilloscope, check at the cathode of CR1 for a pulse going from zero to +4.0 volts. If the pulse is not present, check at J2-4 (see circuit, figure 5.4).

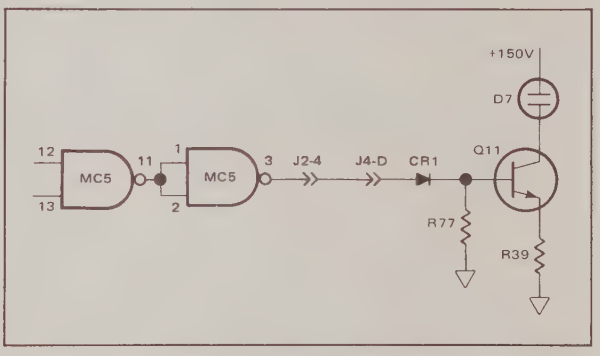


Figure 5.4 - Gate Annunciator

e. If the pulse is not present at J2-4, check the control logic on the Switch board assembly. Verify first that a "start" pulse is being generated.

5.60 If one of the units annunciators does not light, refer to table 5.4. In the table, voltage levels at the inputs and output of gates are listed. If a level differs by ±10% from that listed, the trouble is located between the correct level and the incorrect level. Integrated-circuit drivers in each circuit may be unplugged and exchanged with one of the same type known to be good. If a driver becomes shorted, the corresponding annunciator remains "on". If the driver is open, the annunciator remains "off".

5.61 DECIMAL POINT MALFUNCTION.

5.62 Should any one decimal point not turn on, perform the following decimal point check:

a. Set the FUNCTION switch to FREQ C. Select the 1 μs timebase. No decimal point should be lit. If one is lit, try substituting the readout with the one

Table 5.4 - Units Annunciators Troubleshooting

Annunciator	Function	Select Timebase/Multiplier	Measurement Point	Normal Level	Figure No.
μsec	PERIOD Mode	1 μs	E54 MB11-8	≥2.0 volts	5.5
			MB11-10 MC12-8	≤0.8 volts	
			MB11-11 MB12-3	≥2.0 volts	
			MB12-1	≤0.8 volts	
			MB12-2	≤0.8 volts	
msec	PERIOD Mode	10 μs	E50 MD10-12	≤2.0 volts	5.6
			MD10-13 MD12-8	≤0.8 volts	
			MD12-2	≥2.0 volts	
			MD12-3	≥2.0 volts	
nsec	PER AVG Mode	10^6	E52 MD11-11	≥2.0 volts	5.7
			MD11-13 MC11-8	≤0.8 volts	
			MD11-12	≥2.0 volts	
			MD11-8	≥2.0 volts	
sec	PERIOD Mode	10 ms	E51 MD11-3	≥2.0 volts	5.8
			MD11-1 MC11-6	≤0.8 volts	
			MC11-2	≥2.0 volts	
			MC11-3	≥2.0 volts	
KHz	FREQ A Mode	10s	E53 MB12-8	≥2.0 volts	5.9
			MB12-9 MB12-6	≤0.8 volts	
			MB12-4	≥2.0 volts	
			MB12-5	≥2.0 volts	
MHz	FREQ A Mode	1s	E49 MD10-2	≥2.0 volts	5.10
			MD10-1 MC9-8	≤0.8 volts	
			MC9-1 MA12-6	≥2.0 volts	
			MA12-5 MB8-3	≥2.0 volts	
			MB8-1	≥2.0 volts	
			MB8-2	≥2.0 volts	
			MC9-13	≥2.0 volts	

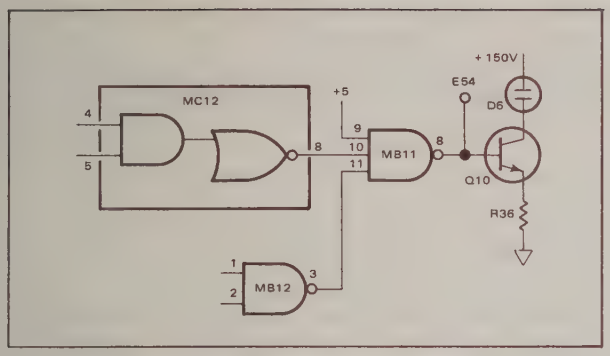


Figure 5.5 - "μsec" Annunciator

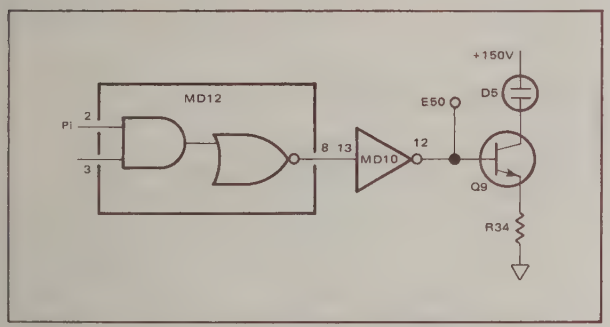


Figure 5.6 - "msec" Annunciator

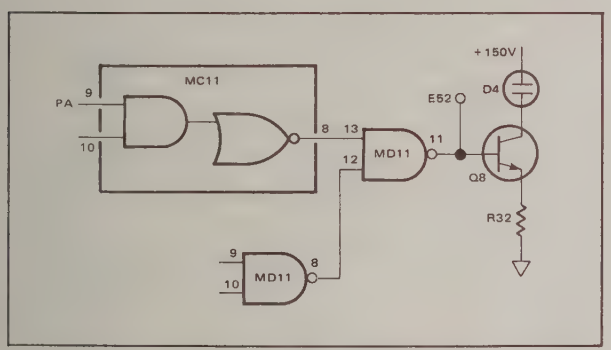


Figure 5.7 - "nsec" Annunciator

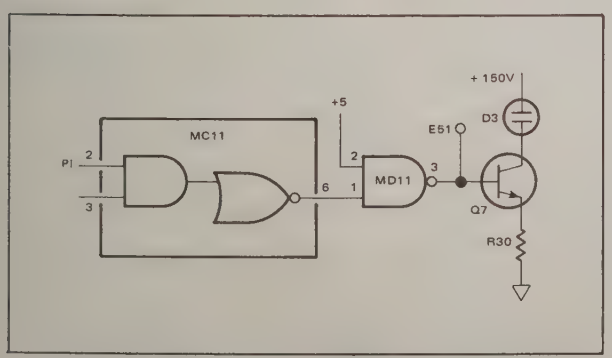


Figure 5.8 - "sec" Annunciator

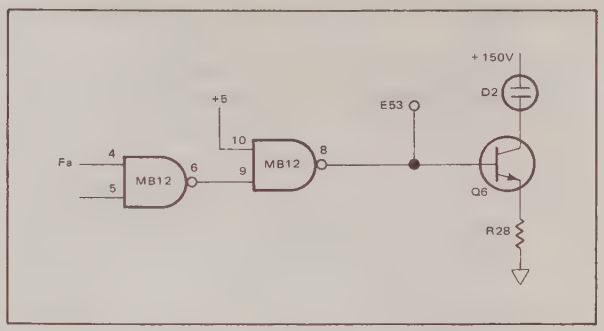


Figure 5.9 - "KHz" Annunciator

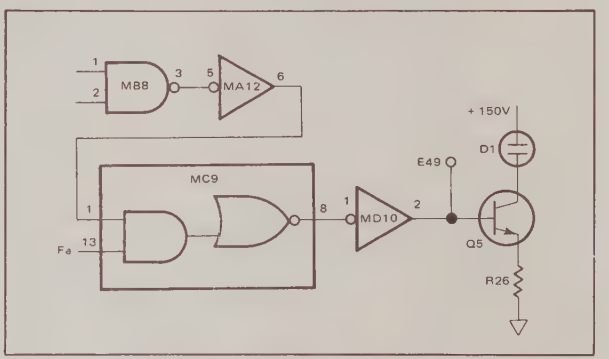


Figure 5.10 - "MHz" Annunciator

next to it. Each decimal point is driven by a transistor which, if open or shorted, causes a decimal point to remain off or on continuously.

b. Depress the 10 μs to 100s TIMEBASE switches; the decimal point should light as shown in table 5.5.

5.63 Procedures for signal tracing through the DP logic are listed in table 5.6.

Table 5.5 - Decimal Point Placement

Timebase	Decimal Point Display								
	V9	V8	V7	V6	V5	V4	V3	V2	V1
10 μs	0	0	0	0	0	0	0	0	.0
100 μs	0	0	0	0	0	0	0	.0	0
1 ms	0	0	0	0	0	0	.0	0	0
10 ms	0	0	0	0	0	.0	0	0	0
100 ms	0	0	0	0	.0	0	0	0	0
1s	0	0	0	.0	0	0	0	0	0
10s	0	0	.0	0	0	0	0	0	0
100s	0	.0	0	0	0	0	0	0	0
	↑	DP8	DP7	DP6	DP5	DP4	DP3	DP2	DP1

Models with Option 004 (9th digit)

Table 5.6 - Troubleshooting Procedure - DP Logic

Decimal Pt.	Select Timebase	Measurement Point(s)	Normal Level	Figure No.
DP1	10 μs	E70 MC7-6	≥2.0 volts	5.11
		MC7-5 MA9-8	≤0.8 volts	
		MA9-4 MA9-5	≥2.0 volts	
DP2	100 μs	E71 CR26 anode CR27 anode	≥2.0 volts	5.12
		MC7-11	≥2.0 volts	
		MC7-12 MC8-6	≥2.0 volts	
		MC7-13 MB9-8	≤0.8 volts	
		MB9-4 MB9-5	≥2.0 volts	
DP3	1 ms	E72 MB7-12	≥2.0 volts	5.13
		MB7-13 MC9-6	≤0.8 volts	
		MC9-4 MC9-5	≥2.0 volts	
DP4	10 ms	E73 MB7-6	≥2.0 volts	5.14
		MB7-5 MA10-8	≤0.8 volts	
		MA10-4 MA10-5	≥2.0 volts	
DP5	100 ms	E74 MB7-4	≥2.0 volts	5.15
		MB7-3 MB10-8	≤0.8 volts	
		MB10-2 MB10-3	≥2.0 volts	
DP6	1s	E75 MC7-8	≥2.0 volts	5.16
		MC7-9 MC10-6	≤0.8 volts	
		MC10-2 MC10-3	≥2.0 volts	
		MC8-8 MC7-10	≥2.0 volts	

Table 5.6 - Troubleshooting Procedure - DP Logic (continued)

Decimal Pt.	Select Timebase	Measurement Point(s)	Normal Level	Figure No.
DP7	10s	E76 MB7-2	≥2.0 volts	5.17
		MB7-1 MC10-8	≤0.8 volts	
		MC10-1 MC10-13	≥2.0 volts	
		MA12-12	≥2.0 volts	
DP8	100s	E77 MB7-10	≥2.0 volts	5.18
		MB7-11 MC8-3	≤0.8 volts	
		MC8-1 MC8-2	≥2.0 volts	
		MA7-10	≥2.0 volts	

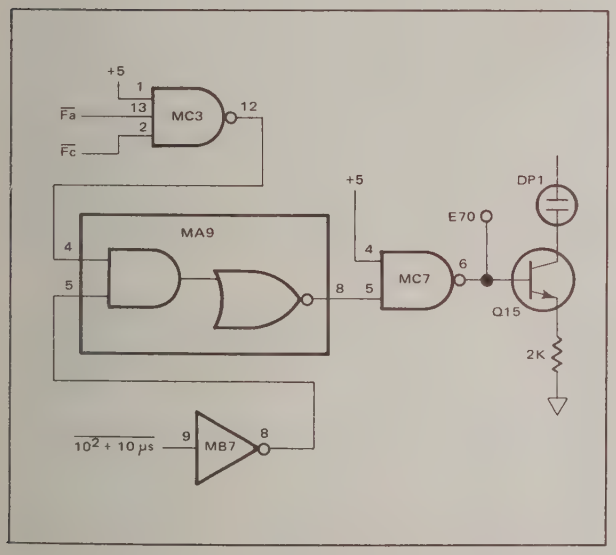


Figure 5.11 - DP1 Decimal Point Logic

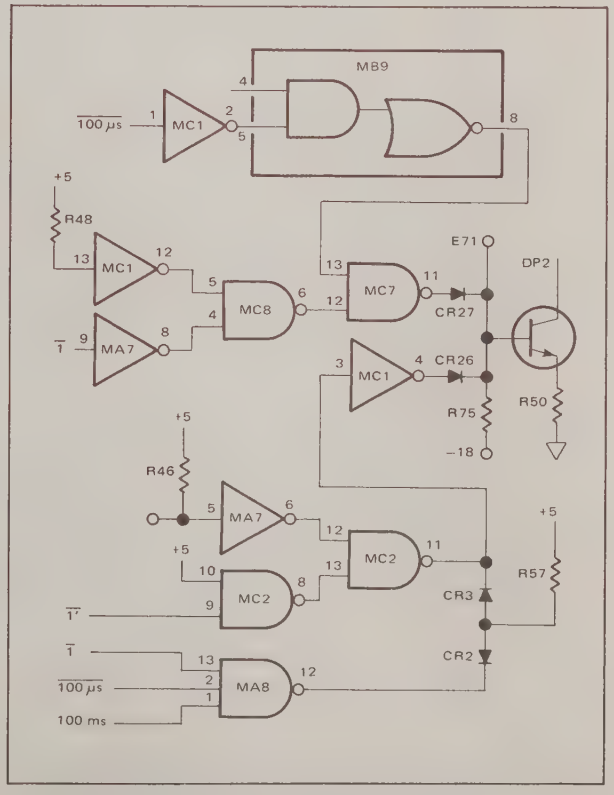


Figure 5.12 - DP2 Decimal Point Logic

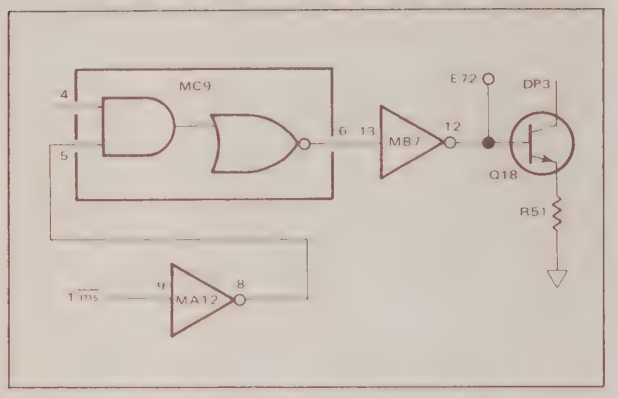


Figure 5.13 - DP3 Decimal Point Logic

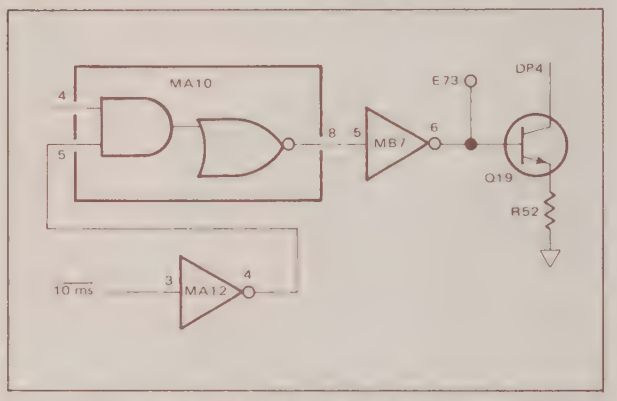


Figure 5.14 - DP4 Decimal Point Logic

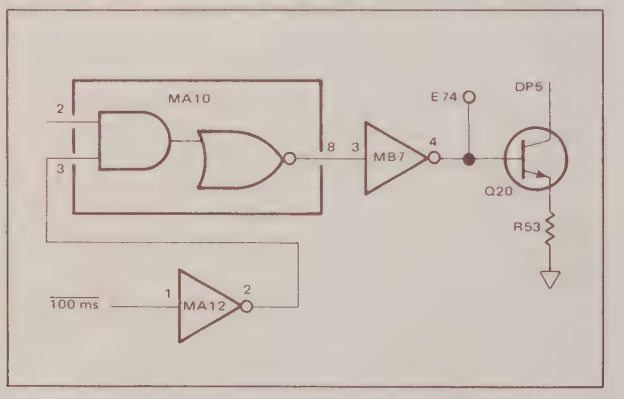


Figure 5.15 - DP5 Decimal Point Logic

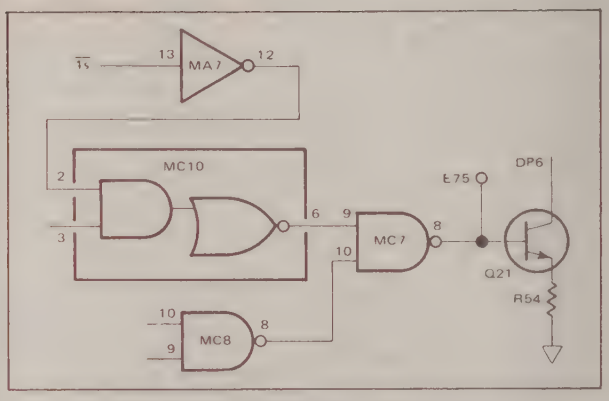


Figure 5.16 - DP6 Decimal Point Logic

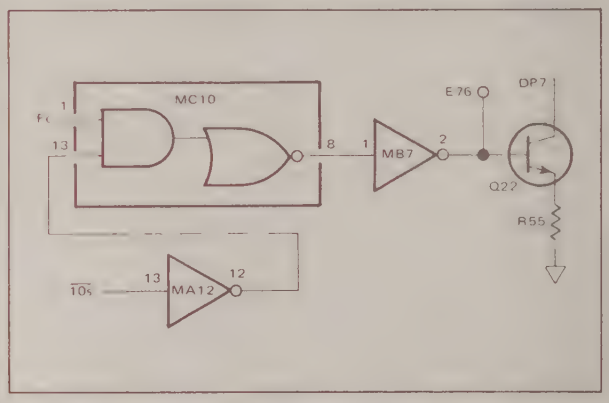


Figure 5.17 - DP7 Decimal Point Logic

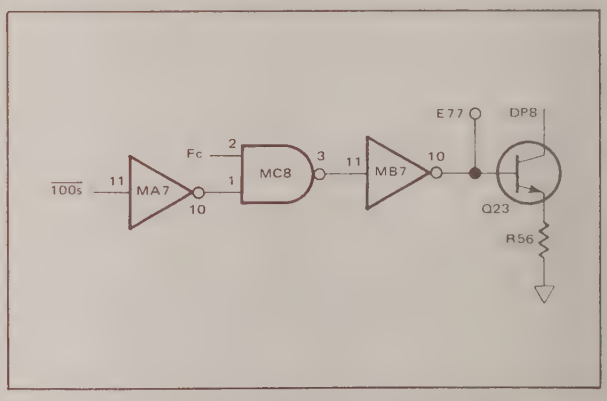
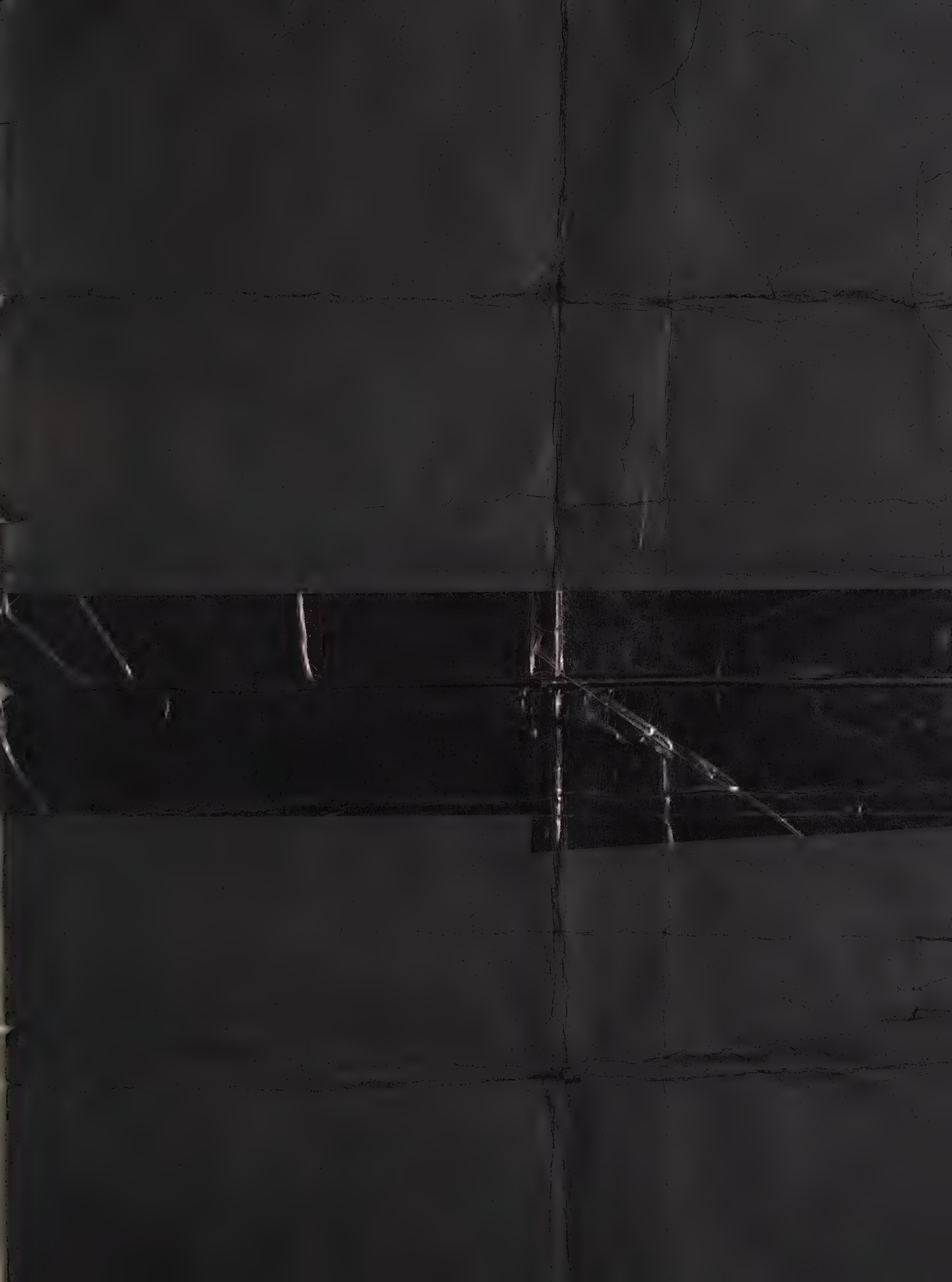


Figure 5.18 - DP8 Decimal Point Logic



5.64 Faulty Remote Operation.

5.65 Normally, problems occurring with the remote programming option occur also in local operation. Verify that transistor Q7 on the Switch board turns off with REMOTE selected. If Q7 operates properly, a malfunction can be traced by following the procedures for troubleshooting a specific operating mode. Also verify that there are no opens or wiring errors in the external circuits.

5.66 Faulty Operation In One Mode.

5.67 Figures 5.25 through 5.33 show the signal flow through the instrument in each mode of operation. Logic levels are given at significant check points to assist in signal tracing.

5.68 CHECK MODE (Figure 5.25).

5.69 In Check mode, the reference oscillator frequency is routed to the counting decades and to the timebase decades.

5.70 FREQUENCY A MODE (Figure 5.28).

5.71 The signal for Frequency A mode is routed through the Signal Conditioning assembly where the trigger slope and trigger point are selected. Attenuation of the signal also takes place in the attenuator section of the signal conditioning. Frequency A (f_a) is routed to the counting decades. The time that the counting decades are allowed to count is controlled by the Reference Oscillator, Timebase Decades, and the Control Logic. Be sure that the FUNCTION switch is positioned to FREQ A and that the range and trigger level controls are set correctly.

5.72 Connect an oscilloscope to E2 and E1 on the Switch board assembly. Connect a signal to the Frequency A input and adjust the counter accordingly. An ECL square wave should be seen varying between 3.4V and 4.2 volts dc. Try moving the trigger level control over its range. If no signal is found, the trouble is in the Attenuator or Signal Conditioning Module. Refer to the schematic of the Signal Conditioning module for troubleshooting (figure 6.2).

5.73 PERIOD MODE (Figure 5.26).

5.74 The signal in the Period mode is routed through the Attenuator and the Signal Conditioning assembly where the trigger slope and trigger level are selected. The signal (f_a) is routed to the Control Logic which controls the time that the counting decades are allowed to count the Reference Oscillator or a frequency division of the Reference Oscillator. Follow the procedure in paragraph 5.72. If the signal is present at E2 and E1, refer to the Period Signal Flow schematic for gate levels and signal flow.

5.75 PERIOD AVERAGE MODE (Figure 5.27).

5.76 The signal in Period Average mode is routed through the Attenuator to the Signal Conditioning assembly and to the Multiplier Timebase Decades. The output of the Timebase Decades (f/n) goes to the start/stop logic and on to the Control Logic which controls the counting decades. The Reference Oscillator is routed to the fast counting decades. The counting decades are controlled by Δt. Δt's time is determined by f_a and the multiplier selected on the front panel. Follow the procedure in paragraph 5.72. If the signal is present at E_2 and E_1, refer to the Period Average Signal Flow schematic for gate levels and signal flow.

5.77 FREQUENCY C MODE (Figure 5.29, not in 8010B).

5.78 Frequency C is much like Frequency A operation. The signal is connected to the Frequency C input and routed into the Frequency C RF Assembly. The signal is amplified. The amplification is controlled by an automatic gain control circuit (AGC). The signal is divided by two through a discrete flip-flop and divided again by two through a ECL flip-flop. The signal is routed to E4 and E3 on the Switch board assembly. The signal (f_c) goes to a ECL gate and to the counting decades. The Reference Oscillator is gated through to a divide-by-four flip-flop to the Timebase Decades.

5.79 To determine if the Frequency C signal reaches the Switch board, connect an oscilloscope to E4 and E3 on the Switch board. Set the FUNCTION switch to FREQ C. Connect a signal to Input C. A ECL square wave should be seen on the oscilloscope varying between 3.4V and 4.2 volts dc. If no signal is found, the trouble is in the Frequency C RF assembly. Refer to figure 6.12 or 6.13 or figures 6.14 and 6.15 for Option 030 (1 mV, 10 MHz – 500 MHz) for the schematic of the RF assembly.

5.80 TOTALIZE MODE (Figure 5.30).

5.81 The signal in the Totalize mode is routed through the A input to the Attenuator and Signal Conditioning Module where the trigger level and slope are selected. The output of the Signal Conditioner is gated to the counting decades. The counting decades are controlled by the manual start/stop circuit which develops Δt, the gate time for the

count. The input signal divided by 10 ($f_a/10$) is routed to the Timebase Decades and to the scaled output connector for external use.

5.82 TIME INTERVAL MODE (Figure 5.31, not in 8020B).

5.83 The signals in the Time Interval mode are routed through the A and B inputs to the A and B Signal Conditioning Modules. The Signal Conditioning circuits determine the trigger points and trigger slope. The output of A is at E2 and E1 on the Switch board. The output of B is at E6 and E5 on the Switch board. The Reference Oscillator is gated to the Multiplier Timebase Decades. The Multiplier Timebase Decades are gated to the counting decades. The counting decades are controlled by the Control Logic which is controlled by the stop/start logic. The signal from input A determines the start time and the input B signal determines the stop time. The start and stop circuits define the gate time.

5.84 Verify that the input controls are set correctly. Observe E2 and E1, and E6 and E5 to determine that a square wave pulse is being generated at the correct time. If a signal is not present, refer to the Signal Conditioning schematic, figure 6.2.

5.85 A/B (RATIO) MODE (Figure 5.32, not in 8020B).

5.86 The signals in the Ratio mode are routed through the Inputs A and B. The signal from Input A goes to the Attenuator and Signal Conditioning circuits where the trigger level and slope are selected. The output of the A Signal Conditioner (f_a) is routed to the counting decades. The output of B Signal Conditioner (f_b) is routed to the Multiplier Timebase Decades and to the Control Logic. The Control Logic starts and stops the counting decades.

5.87 Verify that there is a signal at the output of the A Signal Conditioner (E2, E1). Verify that there is also a signal at the output of the B Signal Conditioner (E6, E5). If either of these signals are missing, refer to the Signal Conditioner schematic, figure 6.2.

5.88 TIME INTERVAL AVERAGE MODE (Figure 5.33, not in 8020B).

5.89 The signals in the Time Interval Average mode are routed through Inputs A and B. The signals are attenuated at the Attenuator. The trigger level and the slope are selected in the A and B signal conditioners. Signals f_a and f_b are routed to the Switch board at points E2 and E1 (A) and E6 and E5 (B). Signal f_a is routed to two type-D flip-flops. The signal is synchronized with the Reference Oscillator. When signal f_a goes high, the reference clock enables the counting decades. Signal f_b is synchronized with the Reference Oscillator and disables the reference clock to the counting decades at the end of the incoming signal. Signal f_b also produces f_b SYN which goes to the Timebase Decades. Signal f_b SYN is generated once per measurement period. Thus, the Timebase Decades count f_b SYN. Depending on the multiplier selected, 1 to 10^9, one measurement or 1000 million measurements will be made and averaged.

5.90 Verify that the signals f_a and f_b, at ECL levels, appear at points E2 and E1 (A), and E6 and E5 (B). If a signal is not present, check the controls for proper setting. Refer to figure 6.2 for schematic of the Signal Conditioner. If both signals f_a and f_b are present, refer to the signal flow schematic.

5.91 Troubleshooting The Signal Conditioning Assembly.

5.92 For disassembly refer to paragraph 5.23. Follow the calibration procedures in paragraphs 5.14 and 5.15 (dual channel). If this does not reveal the problem, refer to the schematic, figure 6.2. Voltage levels and signal level are given on the schematic.

5.93 Channel A and channel B (except on 8020B) are schematically the same. The reference designators are suffixed with an "A" in the channel A circuits. To verify that Q1 and Q10 are matched to each other, proceed as follows:

a. Ground the bases of Q4 and Q8.

b. Measure between the bases of Q2 and Q9. Verify the operation of R20; the voltage should vary from negative, through zero, to positive. If this voltage range cannot be obtained, either Q1 and Q10 are not matched or there is a component failure in the circuit.

5.94 The following pairs of transistors in this circuit are matched as indicated.

Q4 and Q8; V_{be} (base-to-emitter voltage)

Q2 and Q9; V_{be} (base-to-emitter voltage)

Q1 and Q10; R_{ds} (resistance, drain-to-source)

5.95 Troubleshooting The RF Assembly.

5.96 For disassembly, refer to paragraph 5.22. Note: *Do not move any components unless that component is known to be defective.* The RF Assembly is very sensitive to component location. Recalibration will be required if a component is replaced in a critical area. Voltage levels are

given on the schematic figures 6.13 or 6.15. However, it is recommended that the RF assembly be returned to Dana's Product Service for repair and calibration.

5.97 BASIC LOGIC DEFINITION.

5.98 TTL Logic.

5.99 A majority of the integrated circuits used in the 8000B counters are TTL type integrated circuits. TTL circuits operate up to ≅15 MHz. The basic Nor function is shown in figure 5.19. Logic levels are:

Logical 0: ≤.8V Logical 1: ≥2.0V

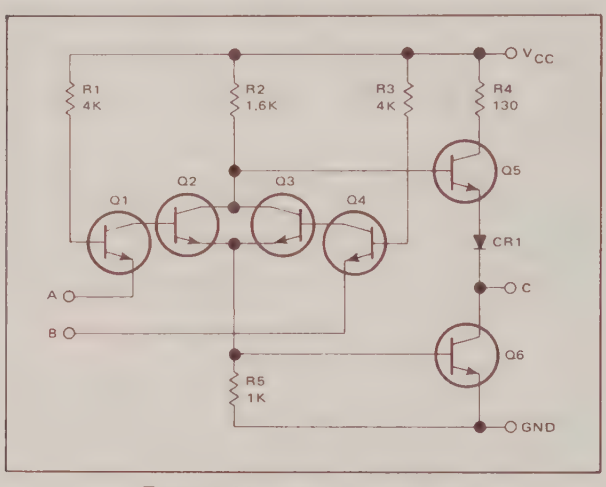


Figure 5.19 - Basic TTL Nor Gate

5.100 The Nor gate is comprised of six transistors. The two input transistors, Q1 and Q4, are used as diode or gates (figure 5.20). Transistors Q2 and Q3 are voltage phase inverters. Transistors Q5 and Q6 form a totem-pole output. The totem-pole circuit has a low output resistance for both a high and low level.

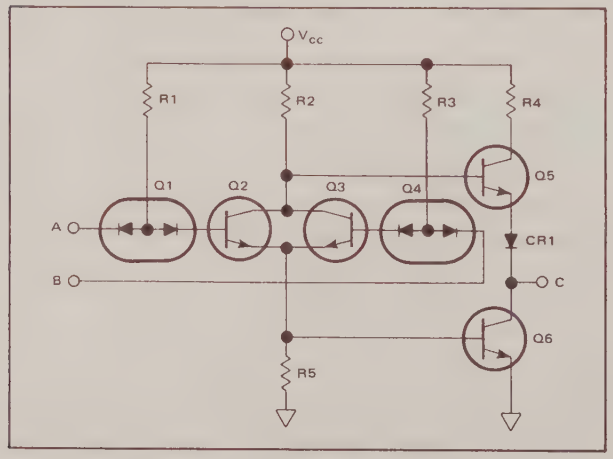


Figure 5.20 - Equivalent Circuit

5.101 Assume a Logical "0" level exists at both A and B inputs. Transistor Q1 and Q4 are conducting. Therefore, the collectors of Q1 and Q4 are at logical "0" level. The logical "0" level from the collectors of Q1 and Q4 are applied to the bases of Q2 and Q3 causing them to turn off. The collectors of Q2 and Q3 are connected together and to the base of Q5. The logical "1" on the base of Q5 causes Q5 to conduct. Output C is connected to the emitter of Q5 via CR1. Diode CR1 prevents an indeterminate output. The output of the Nor gate is two diode drops (1.4V) lower than the base voltages of Q5 or 3.6V.

5.102 Assume a logical "1" level is applied to input A. Base current for Q2 is supplied through R1 and the base-collector junction of Q1. Transistor Q2 is turned on. The collector of Q2 is connected to the base of Q5 and turns Q5 off. The emitter of Q2 is connected to the base of Q6. Q2 supplies base current to Q6 base; therefore Q6 is turned on and output C is low.

5.103 A logical "1" level applied to either or both inputs A or B result in a logical "0" level at output C. The truth table is shown in table 5.7.

Table 5.7 - Truth Table

A	B	C
1	1	0
1	0	0
0	1	0
0	0	1

5.104 Emitter Coupled Logic (ECL).

5.105 BASIC NOR FUNCTION.

5.106 A number of ECL integrated circuits are used in the counter. ECL circuits are used wherever high-speed switching is required. The basic Nor function is shown in figure 5.21. Logic levels used are:

Logical 0: 3.5V Logical 1: 4.2V

5.107 The gate is comprised of differential amplifier Q2 and Q3, input transistors Q1 and Q2, and emitter follower output transistor Q4. Transistor Q3 and resistors R3 and R4 form a fixed bias circuit.

5.108 Assume Logical "0" levels exist at both A and B inputs. Transistors Q1 and Q2 are cut off; therefore, the collectors of Q1 and Q2 are at a logical "1" level. The logical "1" level from the collectors of Q1 and Q2 is applied

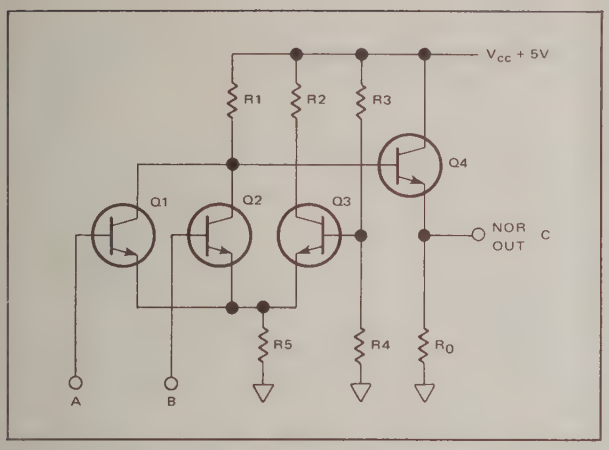


Figure 5.21 - Basic ECL Nor Gate

to the base of Q4, causing Q4 to conduct. The output at the emitter of Q4 is a logical "1" level (output C).

5.109 Assume that a logical "1" level is applied to input A. Transistor Q1 conducts and a logical "0" level results at the Q1 collector due to the drop across R1. The logical "0" level is applied to the base of Q4 causing Q4 to cut off providing a logical "0" level at output C.

5.110 A logical "1" level applied to either or both input A or B results in a logical "0" level at output C. The circuit therefore performs a Nor function; the truth table is shown in table 5.8.

Table 5.8 - ECL NOR Truth Table

A	B	C
0	0	1
1	0	0
0	1	0
1	1	0

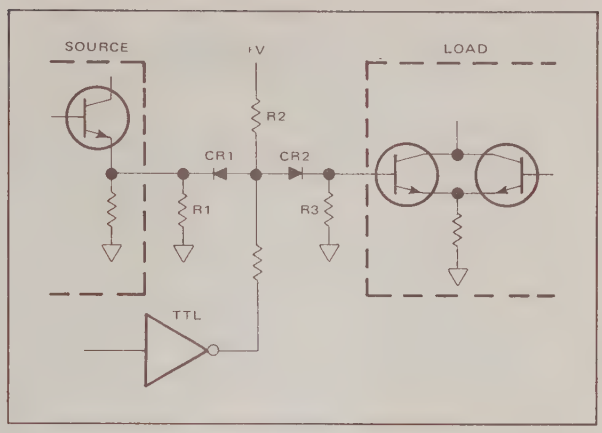


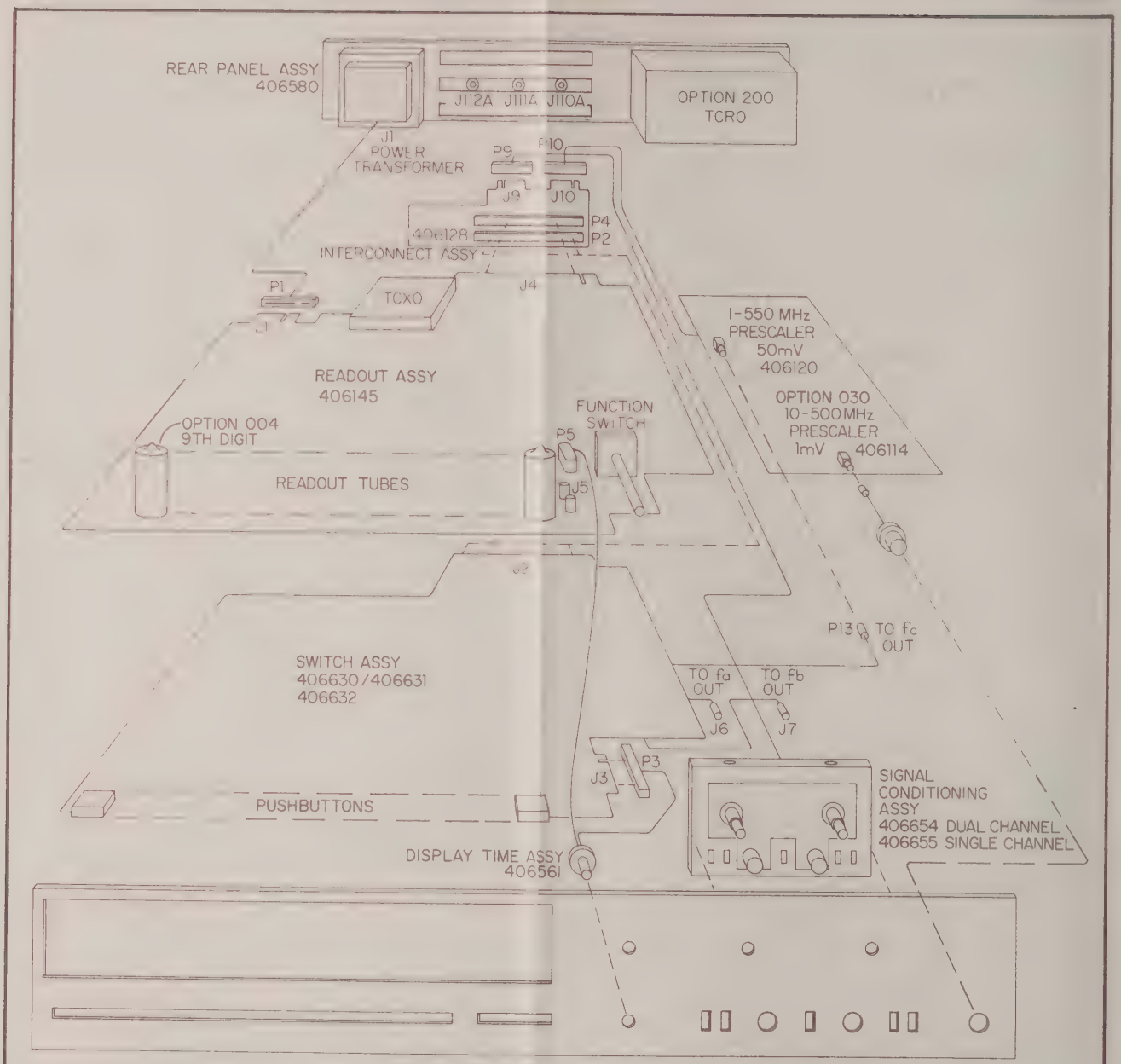
Figure 5.22 - Diode Gate

5.111 DIODE GATE.

5.112 The purpose of a diode gate (figure 5.22) is to control a ECL level signal with a TTL gate. The diode gate is much faster than TTL logic and speed is required in these circuits. Diode CR2 is always in forward conduction with the current provided through resistor R2 from V. The state of CR1 depends on the output of TTL gate. If the TTL gate is high, the CR1 conducts. If the TTL gate is low, then CR1 is reverse-biased and the signal is not transferred from the source to the load. If the output of the TTL gate and CR1 is forward biased, a low insertion loss signal path is provided between the source and the load. DC levels are maintained between the source and load as shown in table 5.9 due to CR1 and CR2 being connected back-to-back.

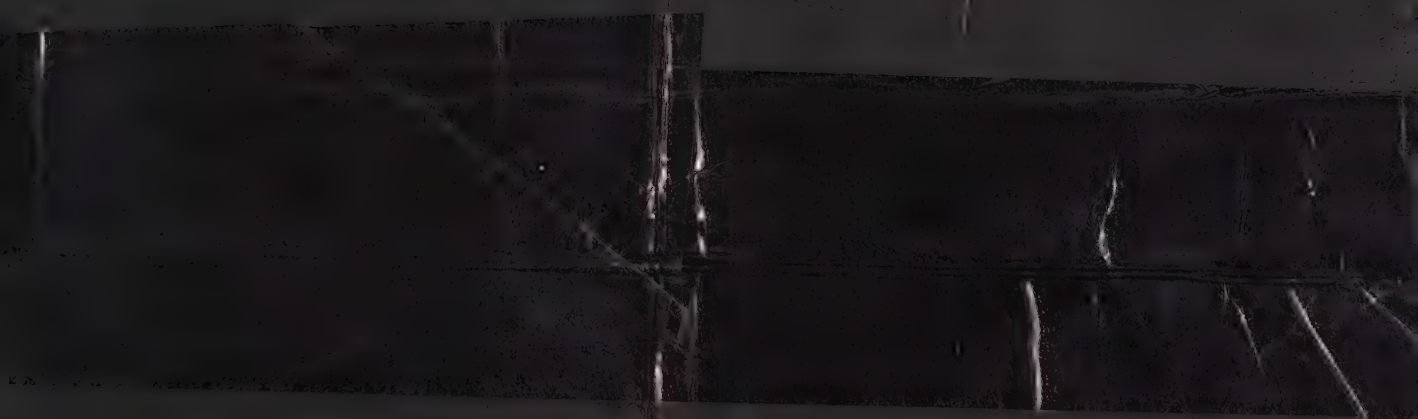
Table 5.9 - DC Levels

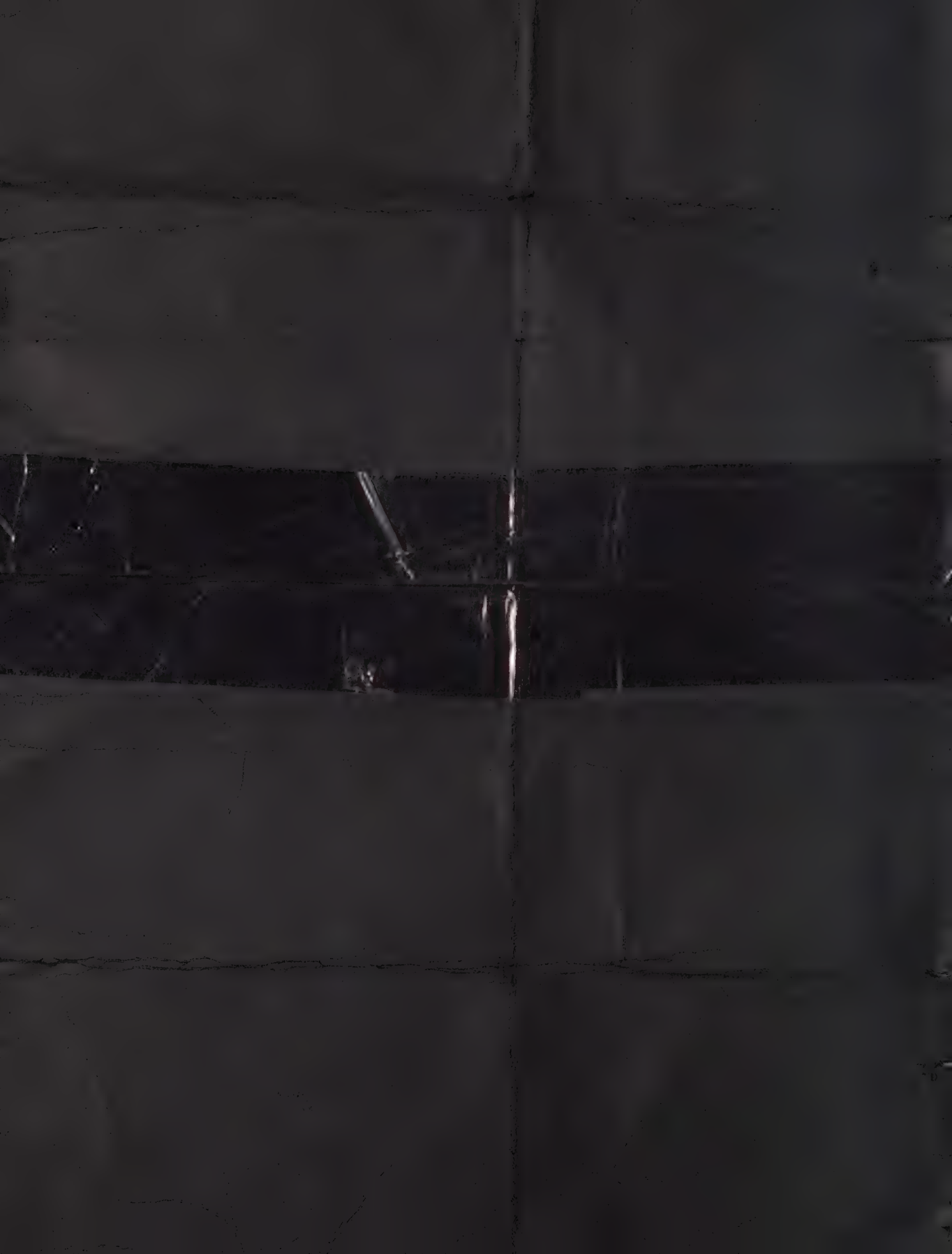
	TTL Gate High		TTL Gate Low	
V Source Output	3.4	4.2	3.4	4.2
V Load Input	3.4	4.2	3.14	3.14



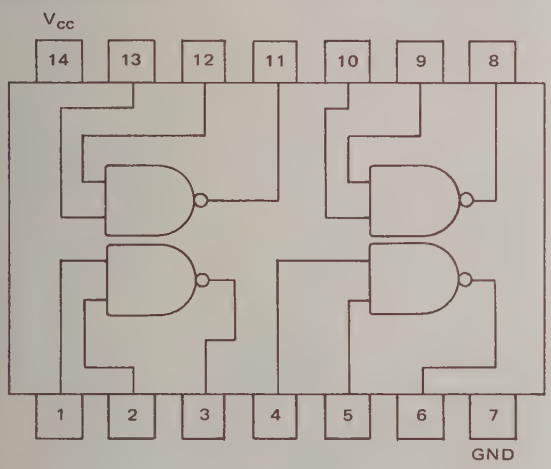
ASSEMBLY NAME	MODEL		
	8010B	8020B	8030B
SIGNAL CONDITIONING	406654	406655	406654
SWITCH BOARD	406631	406630	406632
READOUT BOARD	406145	406145	406145
REAR PANEL	406580	406580	406580
550 MHz PRESCALER	NOTE ONLY 1 PRESCALER PER COUNTER	406120	406120
500 MHz PRESCALER OPTION 030		406114	406114
DISPLAY TIME CONTROL	406561	406561	406561
INTERCONNECT BOARD	406128	406128	406128
FRONT PANEL	730552	730554	730555

Figure 5.23 - Exploded View



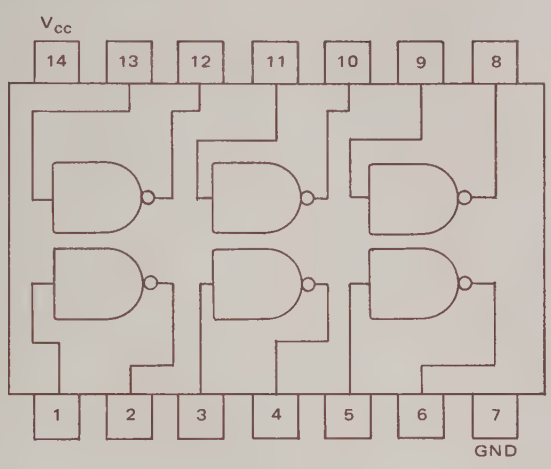


7400 / 74H00
QUADRUPLE 2-INPUT POSITIVE NAND GATE



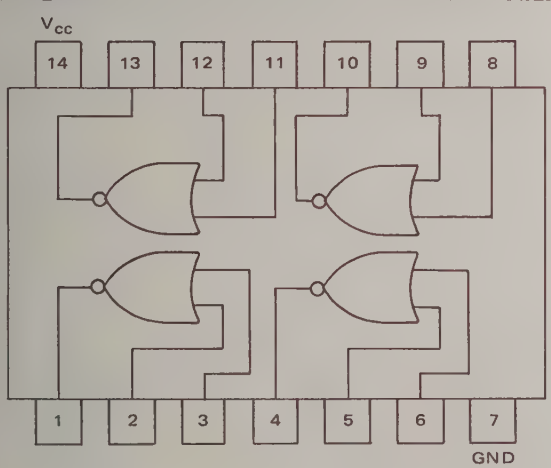
A	B	C
1	1	0
0	1	1
1	0	1
0	0	1

7404
HEX INVERTER



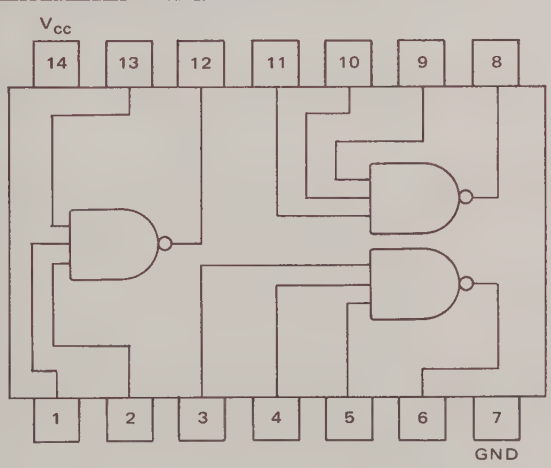
A	B
1	0
0	1

7402
QUADRUPLE 2-INPUT POSITIVE NOR GATE



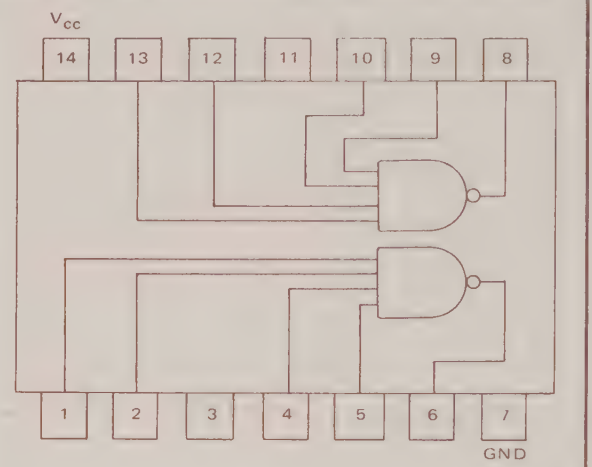
A	B	C
0	0	1
1	1	0
1	0	0
0	1	0

7410
TRIPLE 3-INPUT POSITIVE NAND GATE



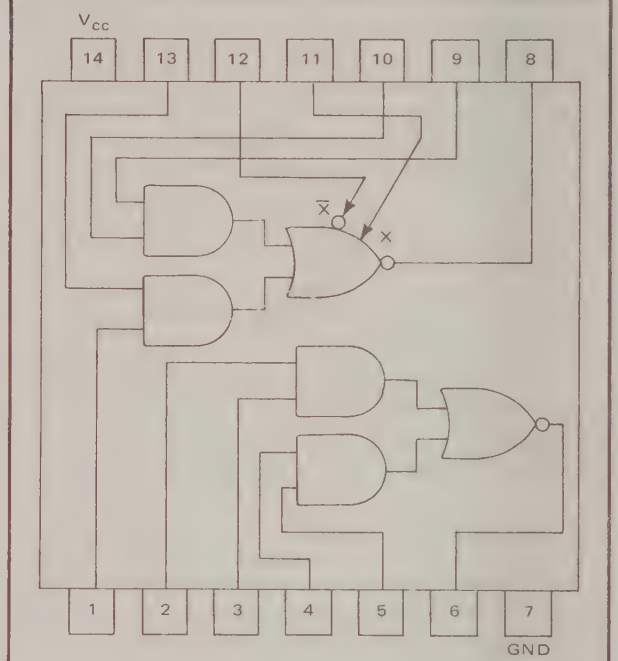
A	B	C	D
1	1	1	0
1	1	0	1
1	0	0	1
0	0	0	1

7420
DUAL 4-INPUT POSITIVE NAND GATE

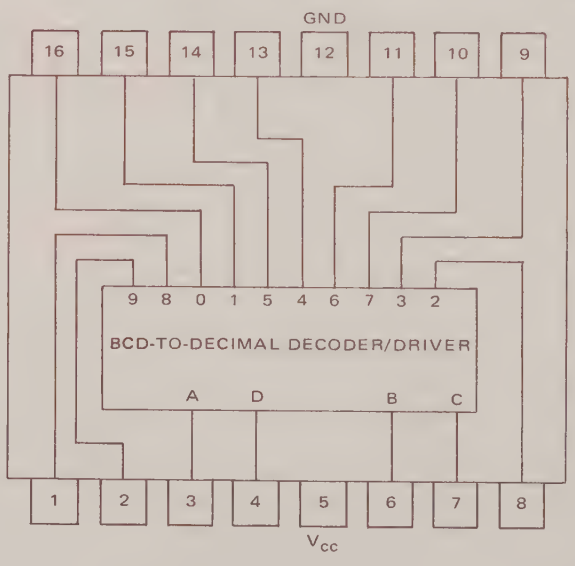


A	B	C	D	E
1	1	1	1	0
1	1	1	0	1
1	1	0	0	1
1	0	0	0	1
0	0	0	0	1

7451
EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES



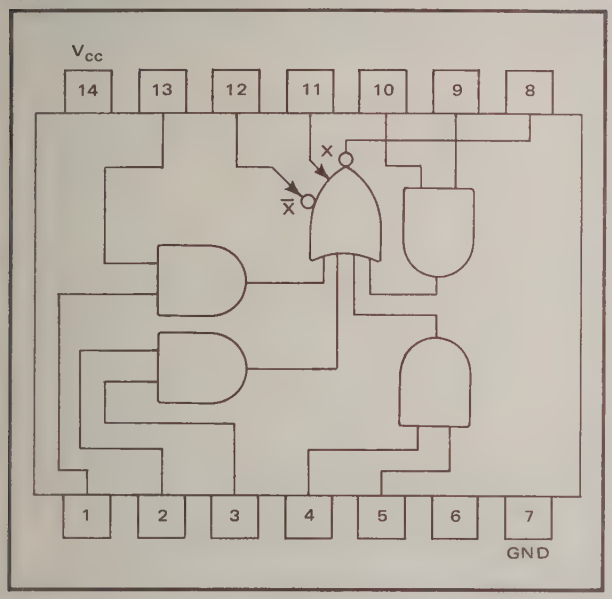
7441
BCD-TO-DECIMAL DECODER/DRIVER



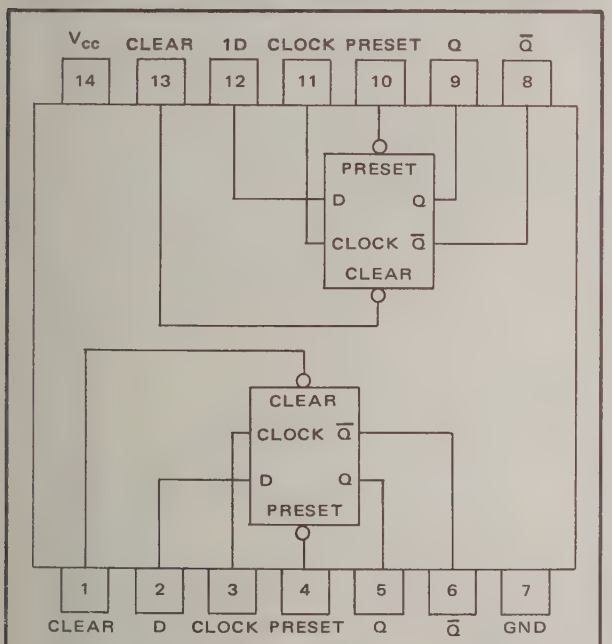
D	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

Figure 5.24 - Integrated Circuits

7454
4-WIDE 2-INPUT AND-OR-INVERT GATE



74H74
DUAL D-TYPE EDGE TRIGGERED FLIP-FLOP



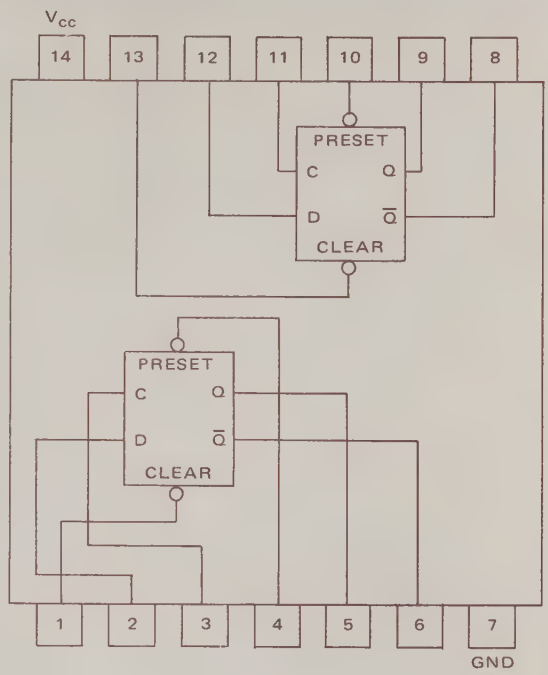
(Each Flip-Flop)		
t_n	t_{n+1}	
Input	Output	Output
D	Q	Q
L	L	H
H	H	L

H = High Level, L = Low Level

NOTES:

1. t_n = bit time before clock pulse
2. t_{n+1} = bit time after clock pulse

7474
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP



D_n	Q_{n+1}	$\overline{Q}_{n+1}$
1	1	0
0	0	1

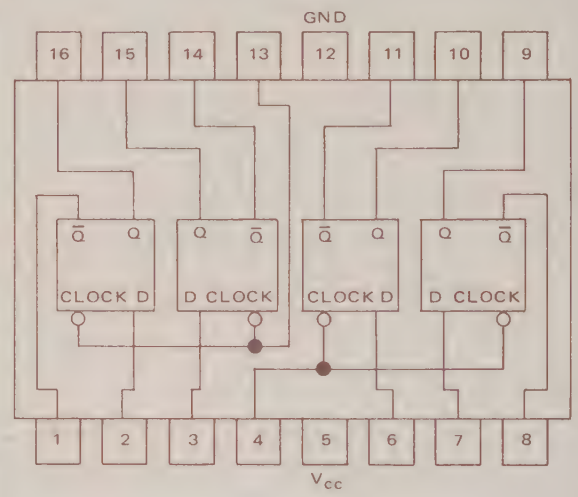
Preset	Clear	Q
1	1	Q
1	0	0
0	1	1
0	0	†

† Both outputs in 1 state

n is time prior to clock

n + 1 is time following clock

7475
QUADRUPLE BISTABLE LATCH

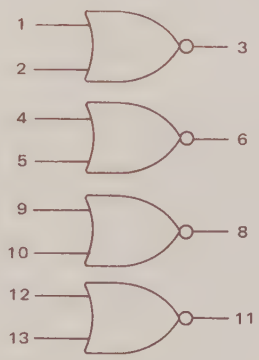


(Each Latch)		
t_n	t_{n+1}	
D	Q	$\bar{Q}$
1	1	0
0	0	1

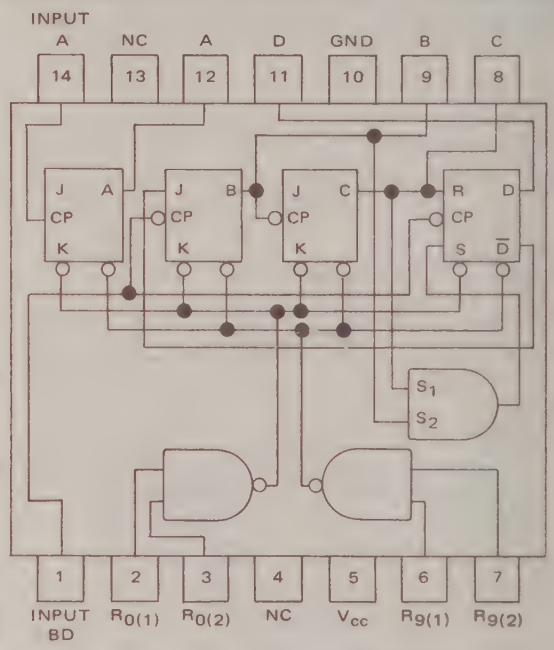
NOTES:

1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. These voltages are with respect to network ground terminal.

MC1010
QUAD 2-INPUT GATES



7490
DECADE COUNTER



BCD COUNT SEQUENCE (See Note 1)

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	0
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

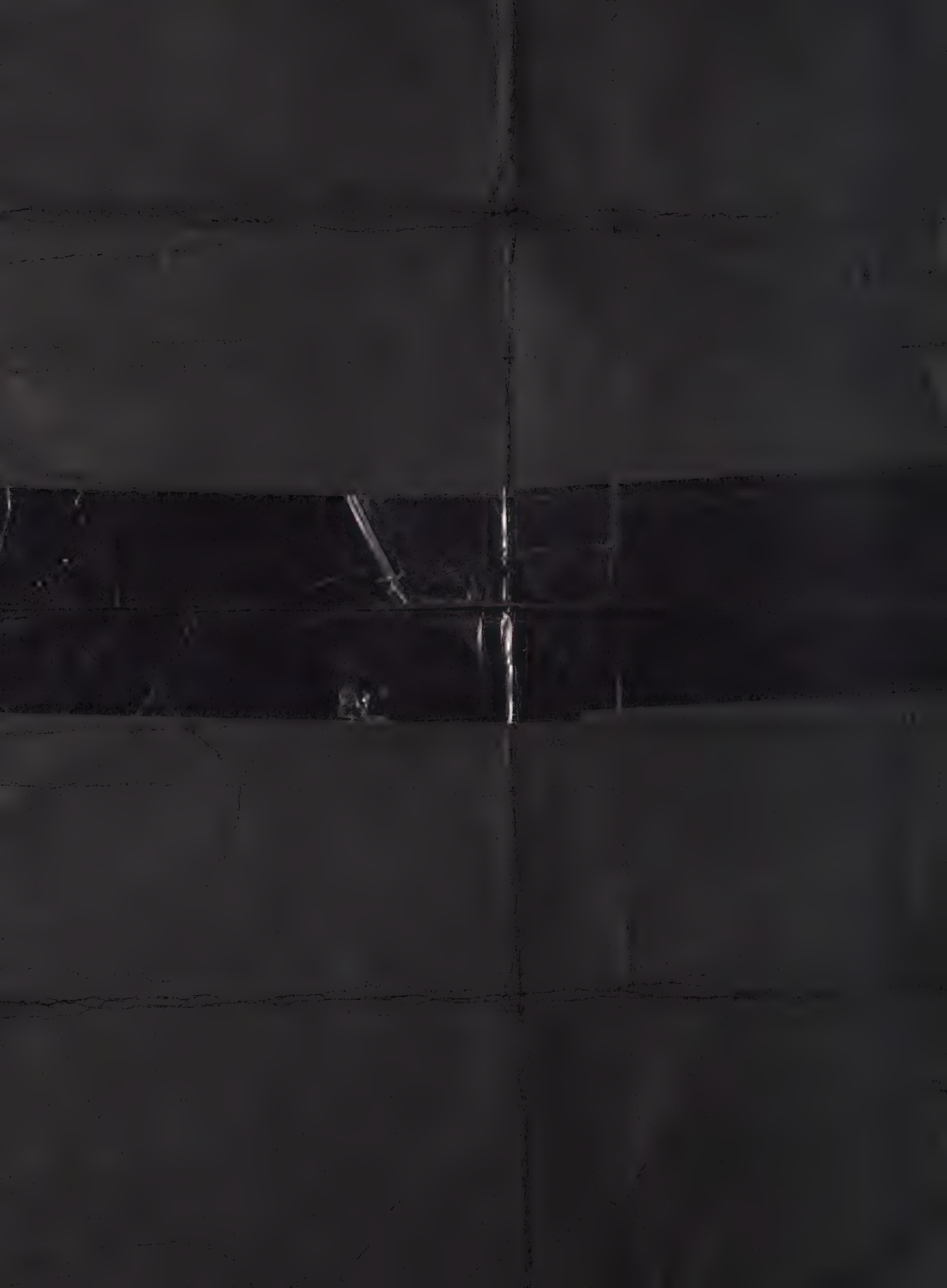
RESET/COUNT (See Note 2)

RESET INPUTS				OUTPUT			
$R_{0(2)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D	C	B	A
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	COUNT			
0	X	0	X	COUNT			
0	X	X	0	COUNT			
X	0	0	X	COUNT			

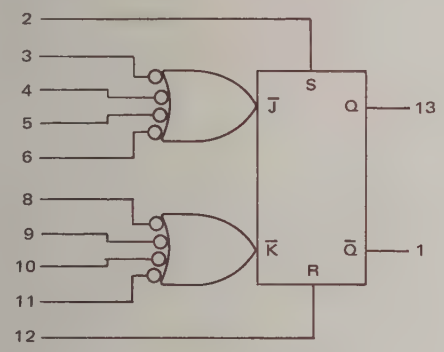
NOTES:

1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 of a logical 0 may be present.
3. Fanout from output A to input BD and to 10 additional Series 54/74 loads is permitted.

Figure 5.24 - Integrated Circuits continued



MC1013 / MC1027
AC-COUPLED J-K FLIP-FLOP



MC1013
DC Input Loading Factor = 1
DC Output Loading Factor = 25
tpd = 6.0 ns typ
Power Dissipation = 125 mW typ

MC1027
DC Input Loading Factor = 2
DC Output Loading Factor = 25
tpd = 4.0 ns typ
Power Dissipation = 250 mW typ

R-S TRUTH TABLE

	R	S	Q^{n+1}
Pin No.	12	2	13
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	N.D.

All $\overline{J}$-$\overline{K}$ inputs are static.
N.D. = Not defined.

$\overline{J}_D$ - $\overline{K}_D$ TRUTH TABLE

	$\overline{J}_D$	$\overline{K}_D$	Q^{n+1}
Pin No.	*	*	13
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\overline{Q}^n$

All other $\overline{J}$-$\overline{K}$ inputs and the R-S inputs are at a "0" level.

CLOCKED $\overline{J}$-$\overline{K}$ TRUTH TABLE

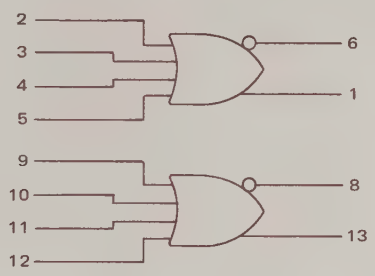
	$\overline{J}$	$\overline{K}$	$\overline{C}_D$	Q^n
Pin No.	*	*	**	13
	Ø	Ø	0	Q^n
	0	0	1	$\overline{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

All other $\overline{J}$-$\overline{K}$ inputs and the R-S inputs are at a "0" level.
Ø = Either state will result in the desired output.

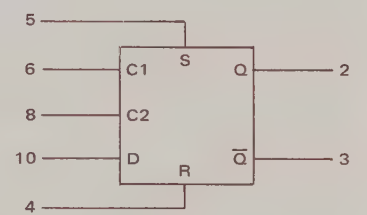
* Any $\overline{J}$ or $\overline{K}$ input, not used for $\overline{C}_D$.
** $\overline{C}_D$ obtained by connecting one $\overline{J}$ and one $\overline{K}$ input together.

The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} − 0.6V). Clock $\overline{C}_D$ is obtained by tying one $\overline{J}$ and one $\overline{K}$ input together.

MC1023
DUAL 4-INPUT CLOCK DRIVER



MC1034
TYPE D FLIP-FLOP



DC Input Loading Factor:
C = 1, D = 2, R and S = 6
DC Output Loading Factor = 25
Power Dissipation = 185 mW typical using external 600-ohm pull-down resistors
240 mW typical using internal pull-down resistors

R-S TRUTH TABLE

	R	S	Q^{n+1}	$\overline{Q}^{n+1}$
Pin No.	4	5	2	3
	0	0	Q^n	$\overline{Q}^n$
	0	1	1	0
	1	0	0	1
	1	1	N.D.	N.D.

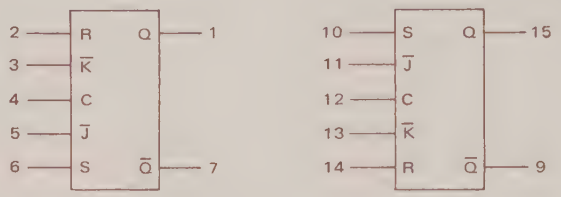
N.D. = Not Defined

CLOCKED TRUTH TABLE

	D	C	Q^{n+1}	$\overline{Q}^{n+1}$
Pin No.	10	6 or 8	2	3
	0	0	Q^n	$\overline{Q}^n$
	1	0	Q^n	$\overline{Q}^n$
	0	1*	0	1
	1	1*	1	0

*A "1" or Clock input is defined for this flip-flop as a change in level from a low state to a high state of the clock.

MC1032
100-MHz AC-COUPLED DUAL J-K FLIP-FLOP



V_{CC} = Pin 16
V_{EE} = Pin 8

DC Input Loading Factor:
Clock = 2
$\bar{J}$, $\bar{K}$, S, R = 1
DC Output Loading Factor = 25
tpd = 4.5 ns typ
Power Dissipation = 180 mW typ

R-S TRUTH TABLE

	R	S	Q^{n+1}
Pin No.	2 & 14	6 & 10	1 & 15
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	N.D.

All $\bar{J}$-$\bar{K}$ inputs and Clock inputs are static
N.D. = Not defined

$\bar{J}_D$-$\bar{K}_D$ TRUTH TABLE

	$\bar{J}$	$\bar{K}$	Q^{n+1}
Pin No.	*	*	1 & 15
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\bar{Q}^n$

All Clock inputs and the R-S inputs are at a "0" level.

CLOCKED $\bar{J}$-$\bar{K}$ TRUTH TABLE

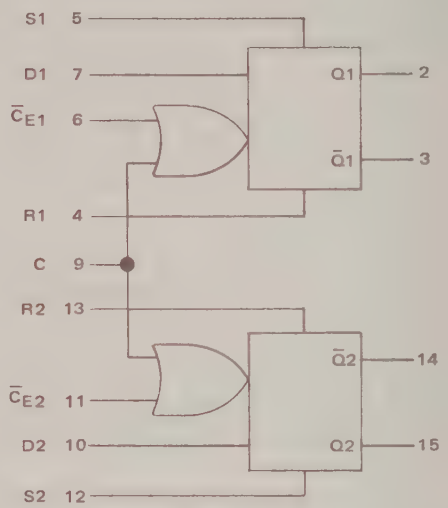
	$\bar{J}$	$\bar{K}$	Clock	Q^n
Pin No.	*	*	4 & 12	1 & 15
	Ø	Ø	0	Q^n
	0	0	1	$\bar{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

All other $\bar{J}$-$\bar{K}$ inputs and the R-S inputs are at a "0" level.
Ø = Either state will result in the desired output.

* Any $\bar{J}$ or $\bar{K}$ input

The $\bar{J}$ and $\bar{K}$ inputs refer to logic levels while the clock input refers to dynamic logic swings. The $\bar{J}$ and $\bar{K}$ inputs should be changed to a logic "1" only while the clock input is in a logic "1" state. (Clock maximum "1" level = V_{CC} – 0.7V.)

MC10131
DUAL TYPE D MASTER-SLAVE FLIP-FLOP



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

R-S TRUTH TABLE

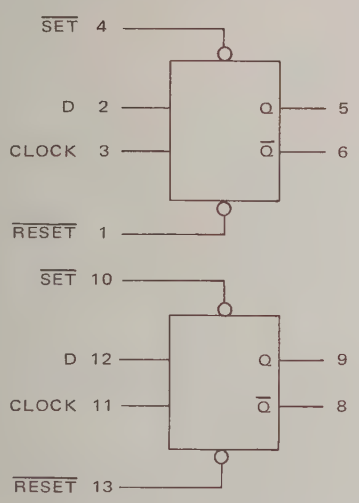
R	S	Q^{n+1}	$\bar{Q}^{n+1}$
L	L	Q^n	$\bar{Q}^n$
L	H	H	L
H	L	L	H
H	H	N.D.	N.D.

N.D. = Not Defined

SEQUENTIAL TRUTH TABLE

D	C	$\bar{C}_E$	Q_{n+1}
L	L	L	Q_n
L	L	H	L
L	H	L	Q_n
L	H	H	Q_n
H	L	L	Q_n
H	L	H	H
H	H	L	Q_n
H	H	H	Q_n

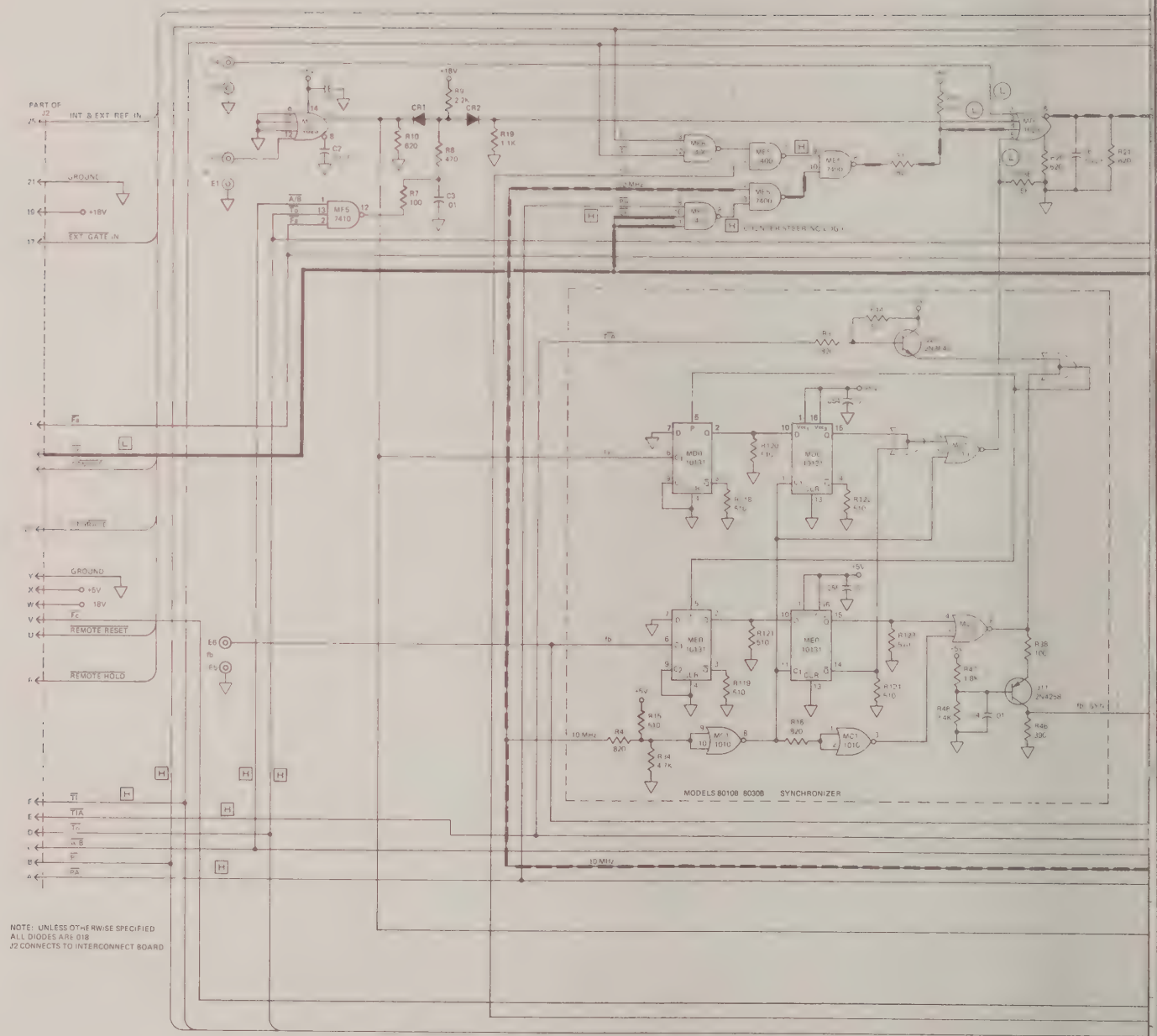
DUAL TYPE D FLIP-FLOP MC3060F



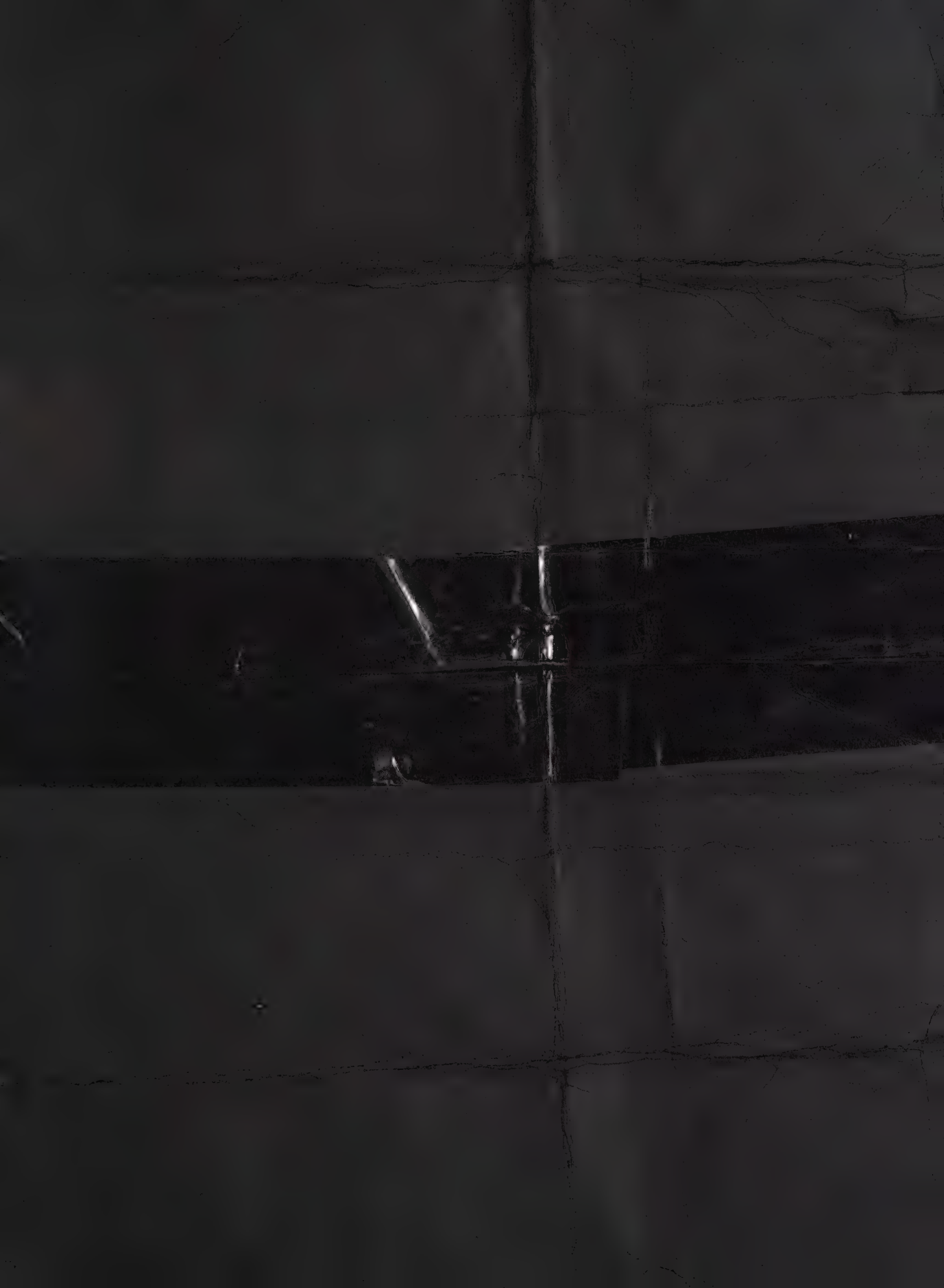
TRUTH TABLE

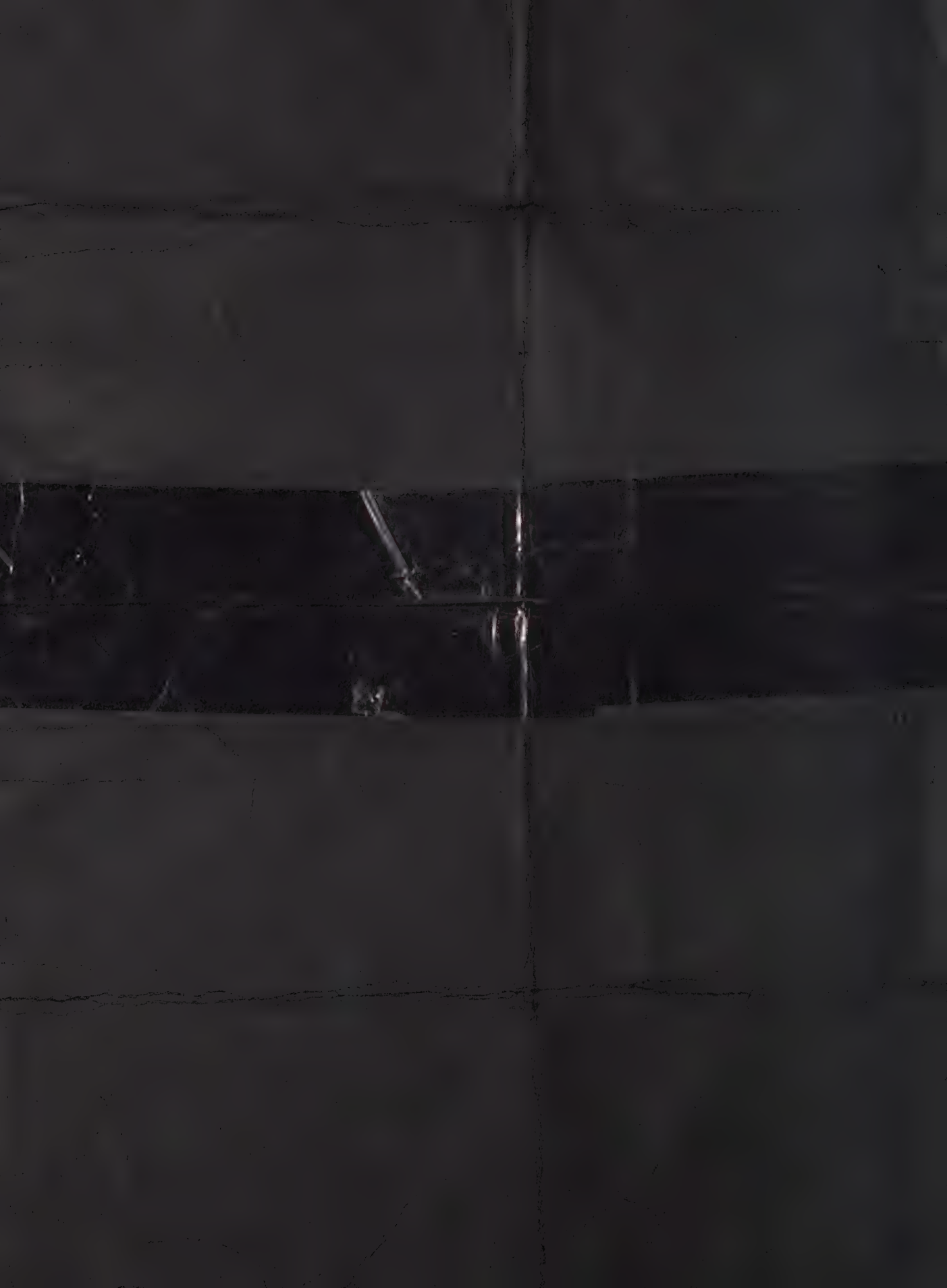
D	Q^n	Q^{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

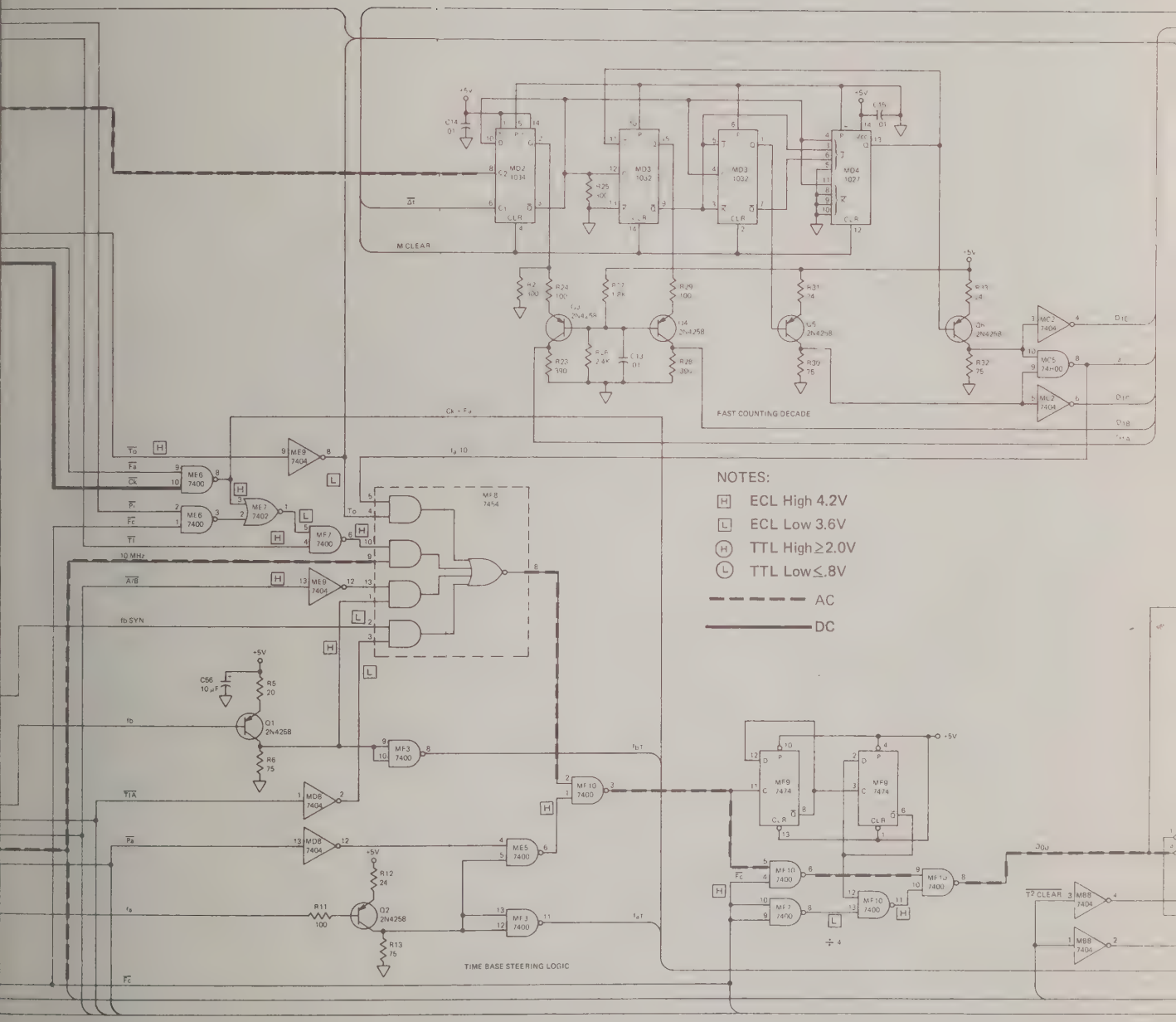
$Q^{n+1} = D^n$

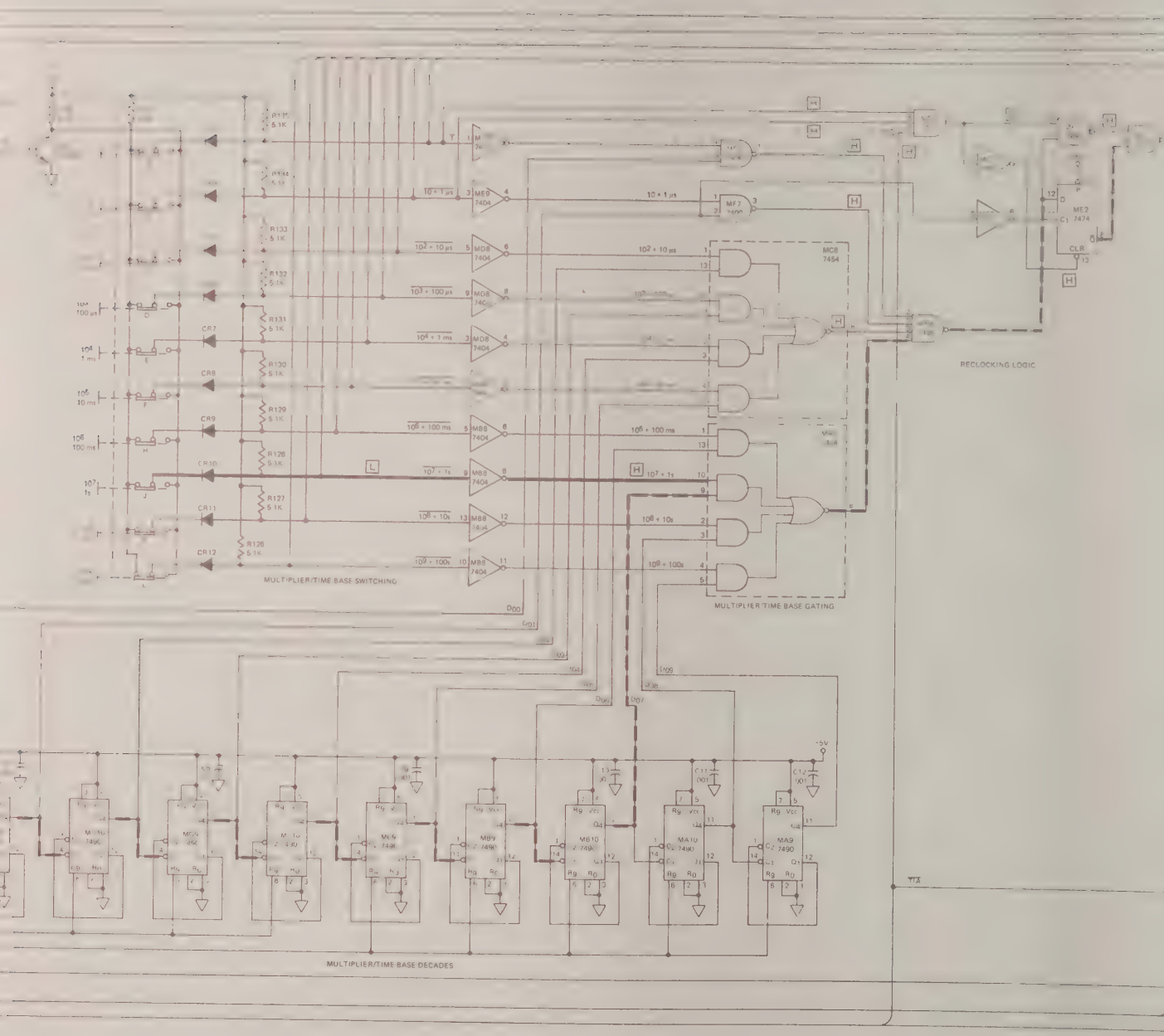


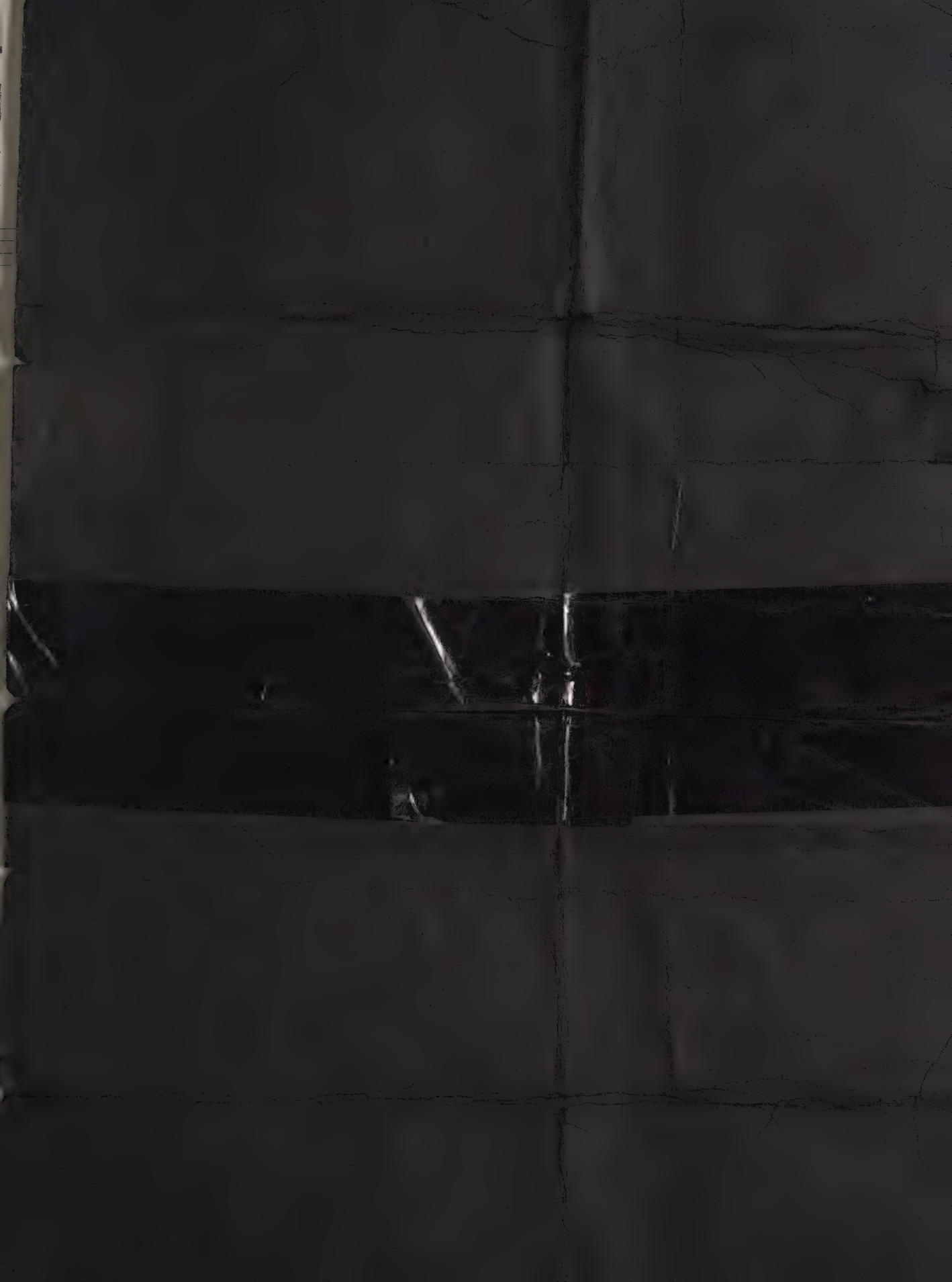
5-20 Figure 5.25 - Signal Flow for Check Mode

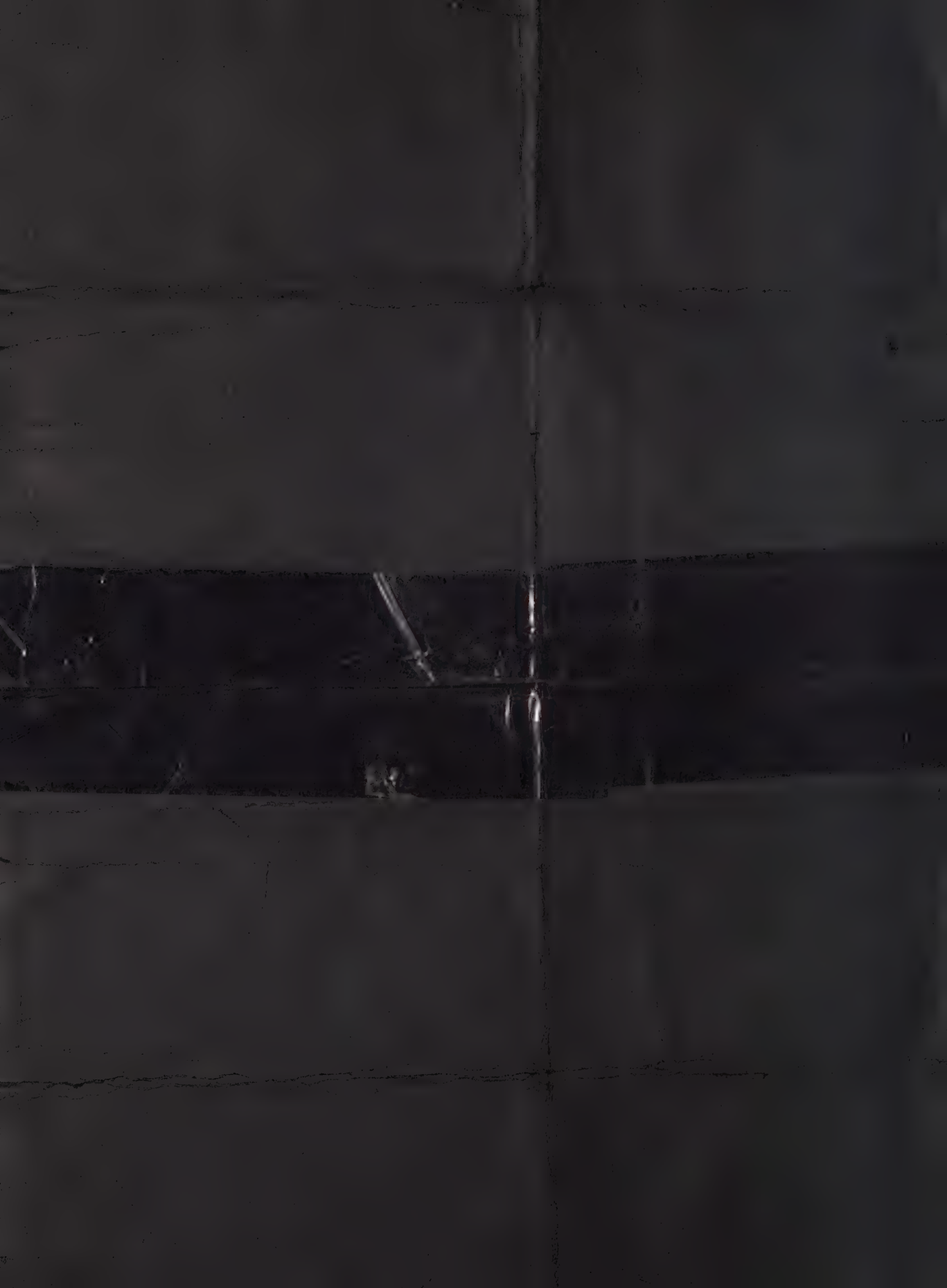





NOTES:
H ECL High 4.2V
L ECL Low 3.6V
(H) TTL High ≥2.0V
(L) TTL Low ≤.8V
AC
DC
FAST COUNTING DECADE
TIME BASE STEERING LOGIC
M CLEAR
÷ 4


MULTIPLIER/TIME BASE SWITCHING
MULTIPLIER/TIME BASE GATING
RECLOCKING LOGIC
MULTIPLIER/TIME BASE DECADES





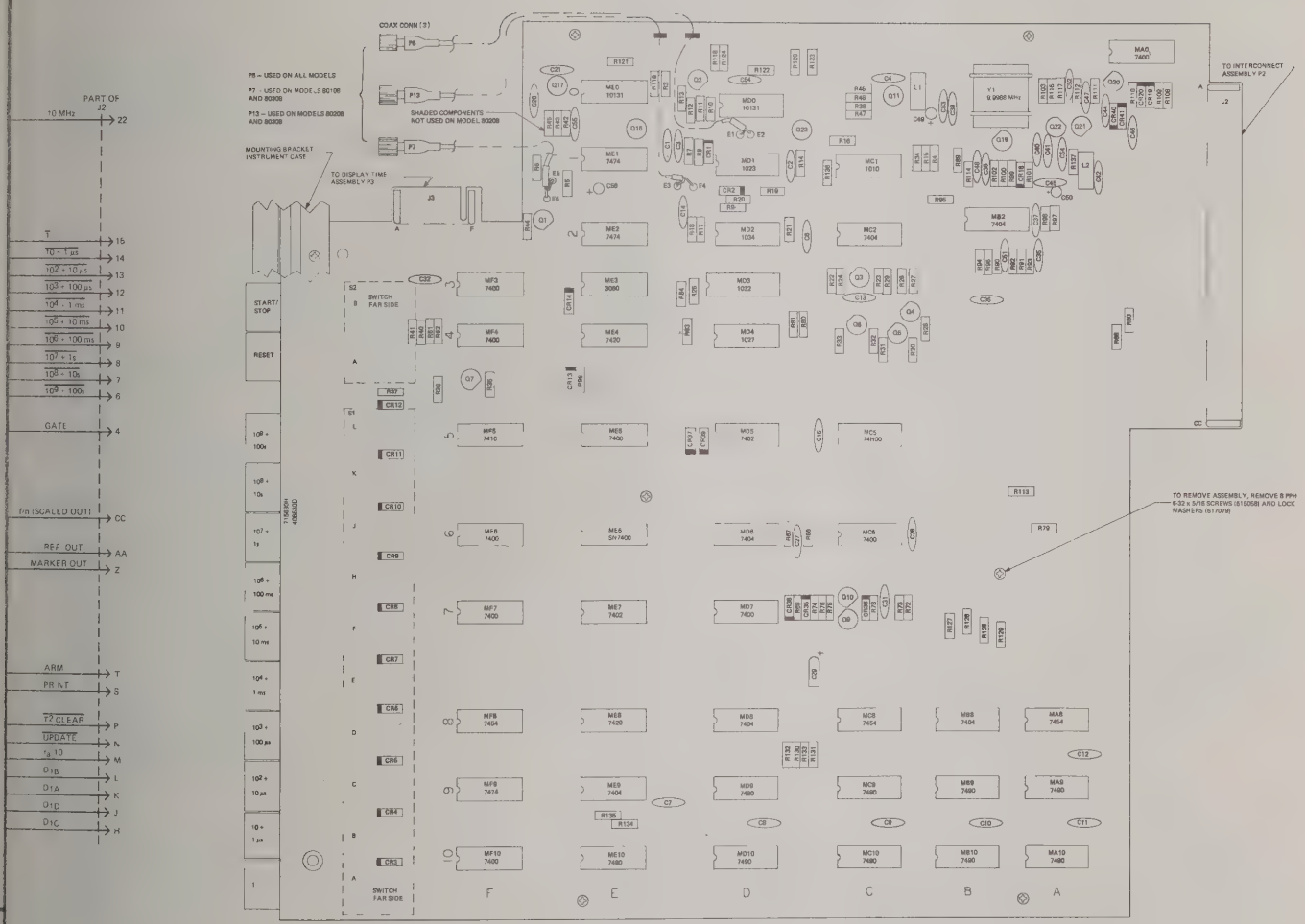
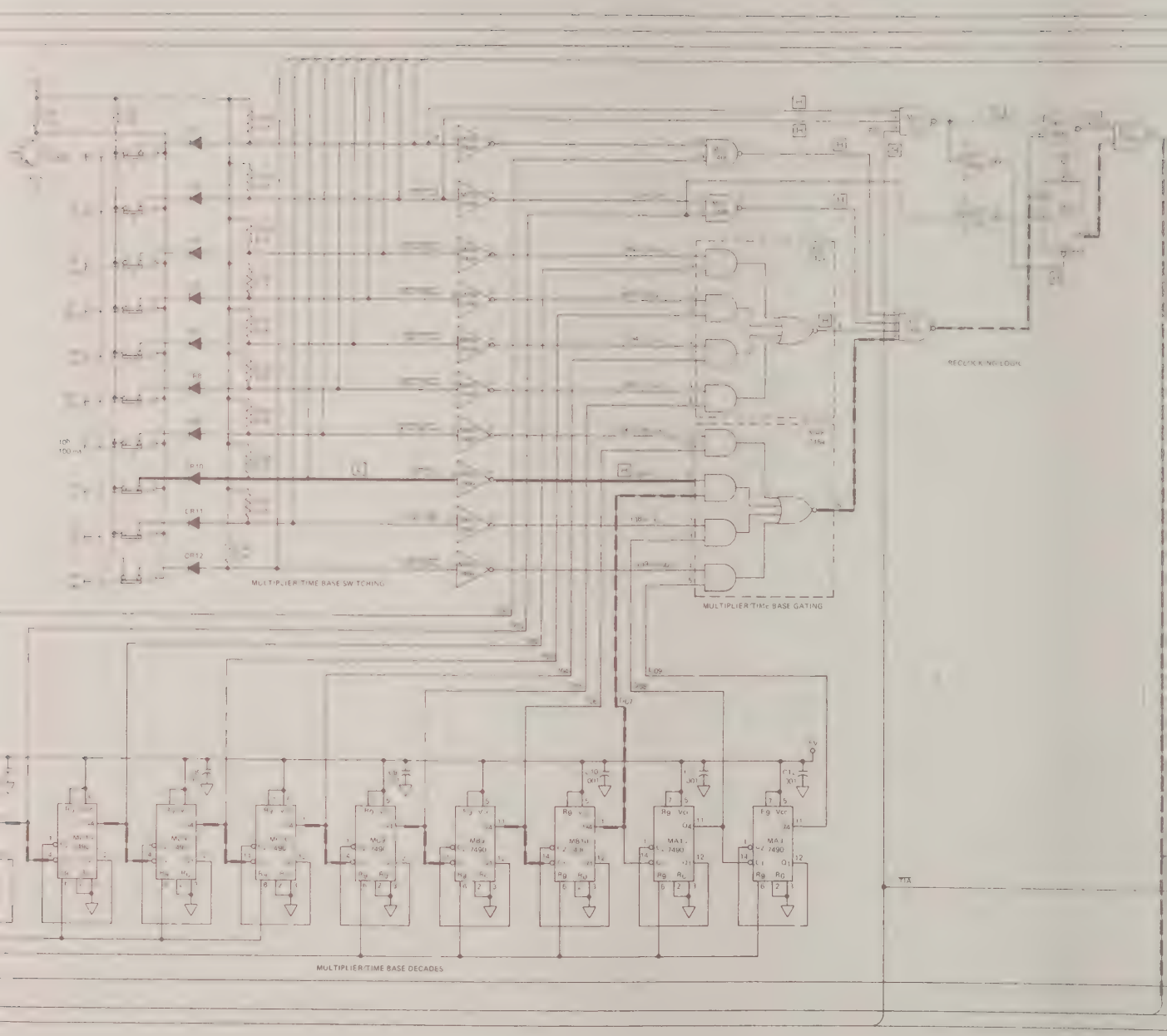
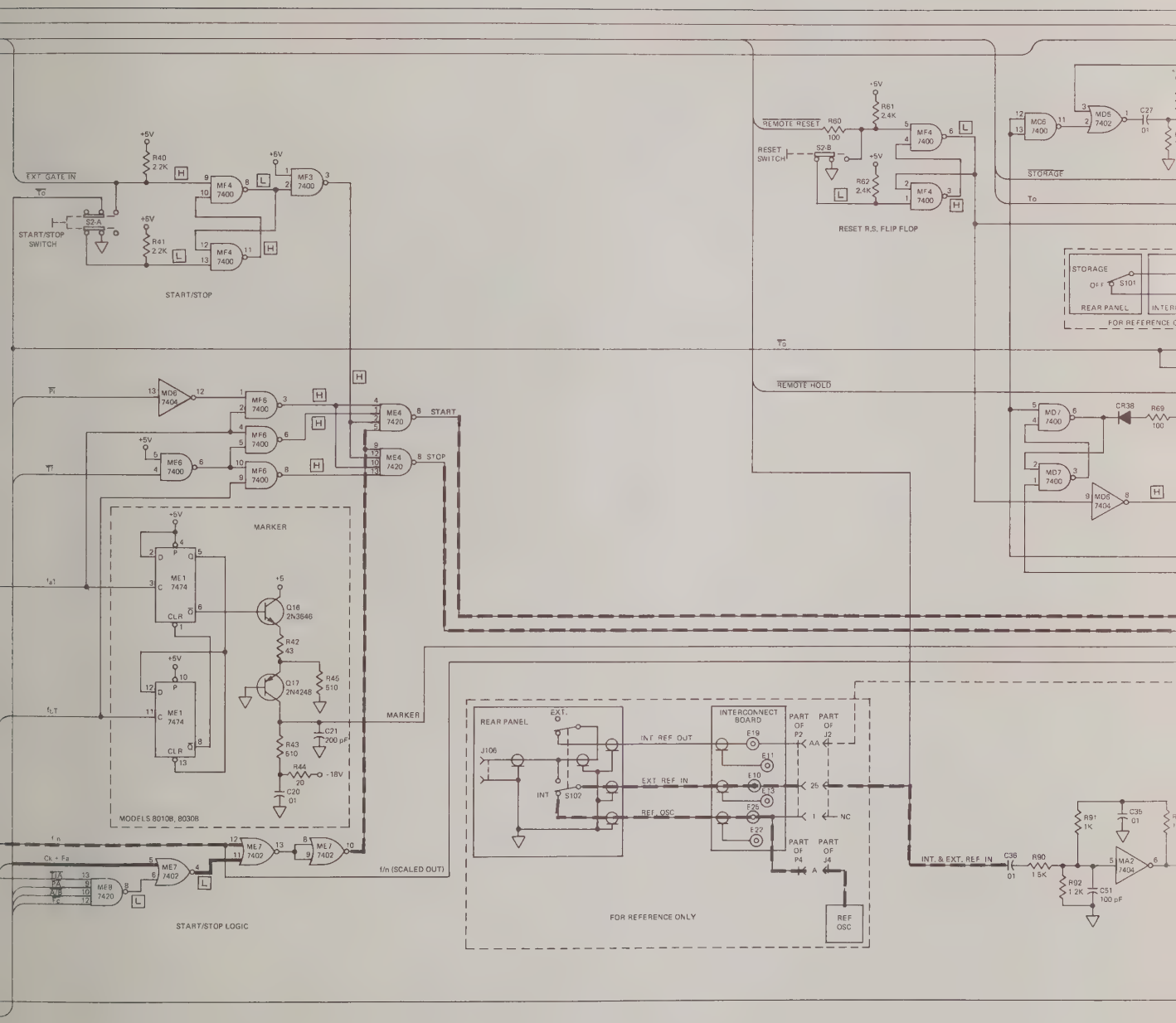
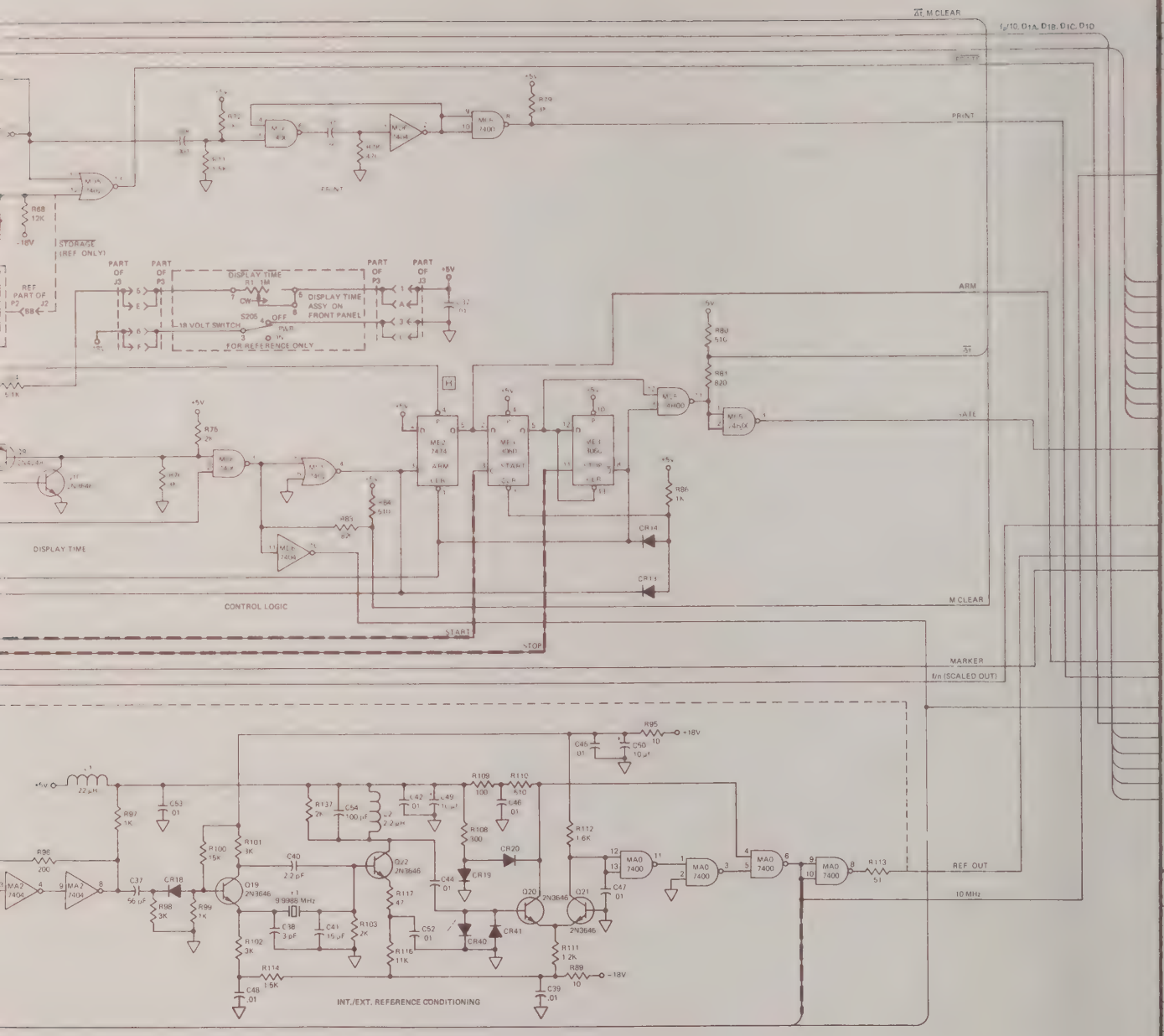
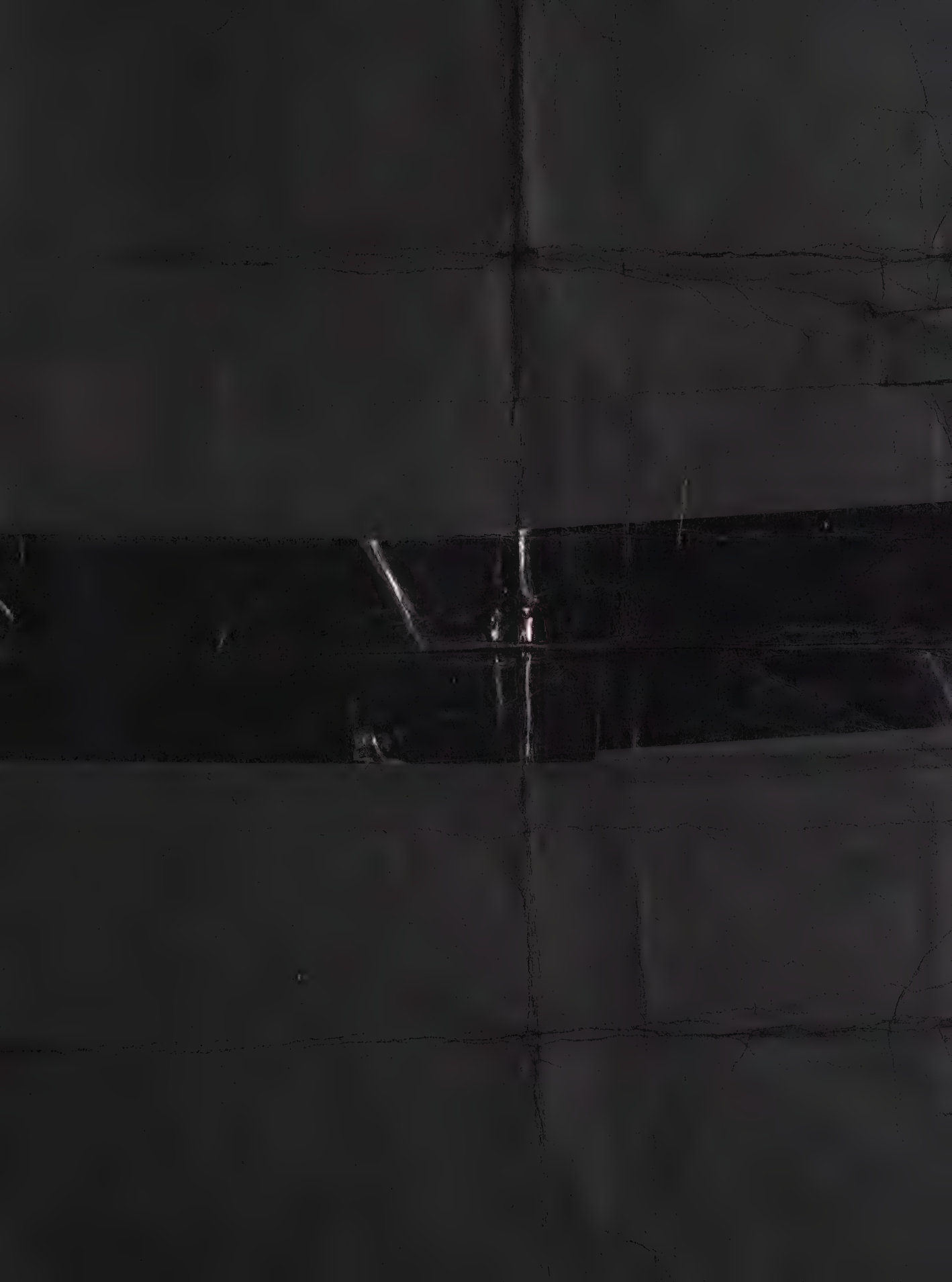


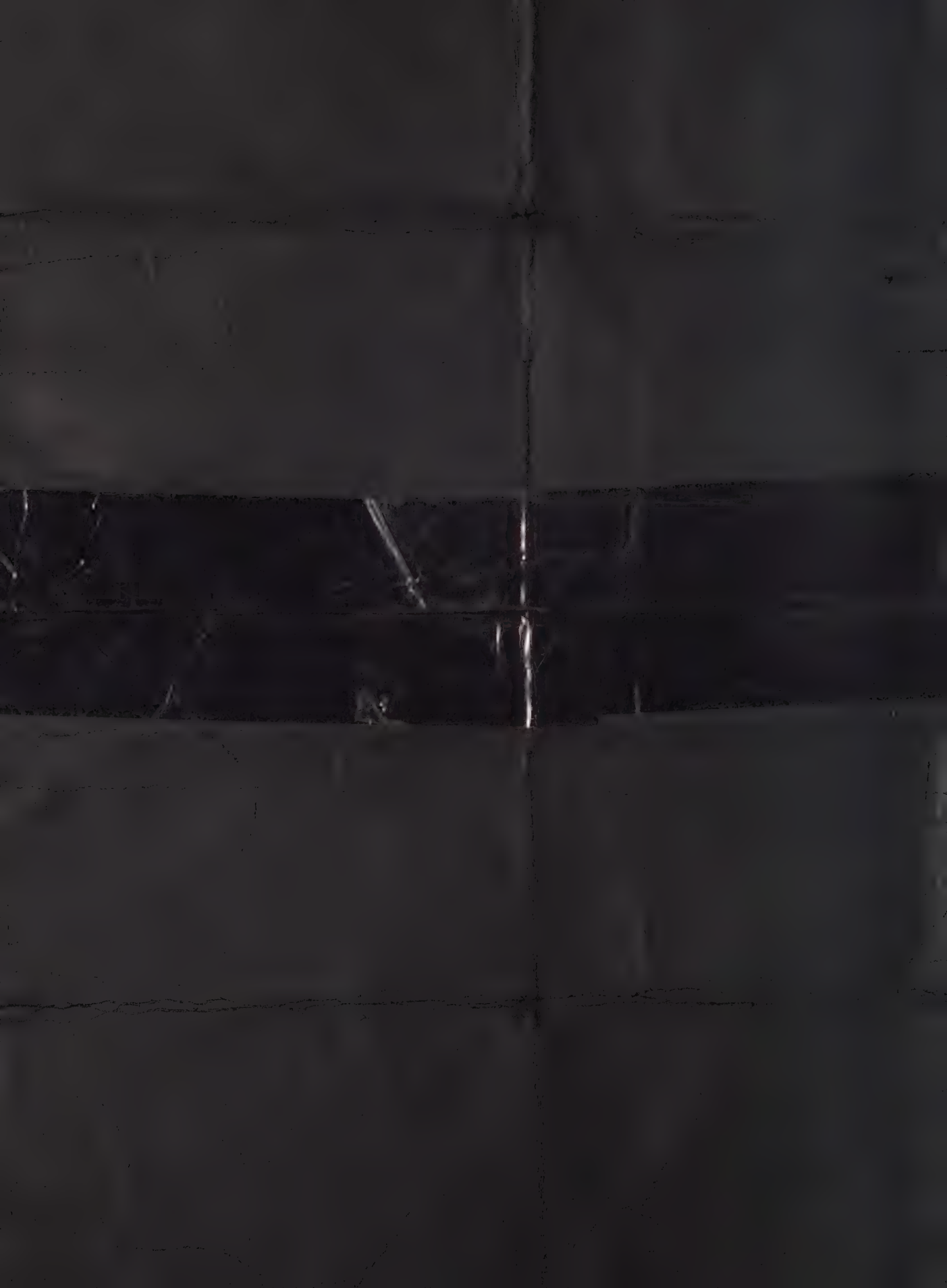
Figure 5.25 - Signal Flow for Check Mode 5-21


MULTIPLIER TIME BASE SWITCHING
MULTIPLIER TIME BASE GATING
MULTIPLIER TIME BASE DECADES


EXT GATE IN
START/STOP SWITCH
S2-A
START/STOP
REMOTE RESET
RESET SWITCH
S2-B
RESET R.S. FLIP FLOP
STORAGE
S101
REAR PANEL
REMOTE HOLD
START
STOP
MARKER
MODELS 8010B, 8030B
Q16 2N3646
Q17 2N4248
INTERCONNECT BOARD
REAR PANEL
INT REF OUT
EXT REF IN
REF OSC
INT
S102
J106
FOR REFERENCE ONLY
REF OSC
INT. & EXT. REF. IN
f/n (SCALED OUT)
START/STOP LOGIC


ΔT, M CLEAR
PRINT
ARM
ΔT
GATE
M CLEAR
MARKER
1/n (SCALED OUT)
REF OUT
10 MHz
STORAGE (REF ONLY)
DISPLAY TIME
DISPLAY TIME ASSY ON FRONT PANEL
18 VOLT SWITCH
FOR REFERENCE ONLY
CONTROL LOGIC
START
STOP
INT./EXT. REFERENCE CONDITIONING
9.9988 MHz
2N3646
7400





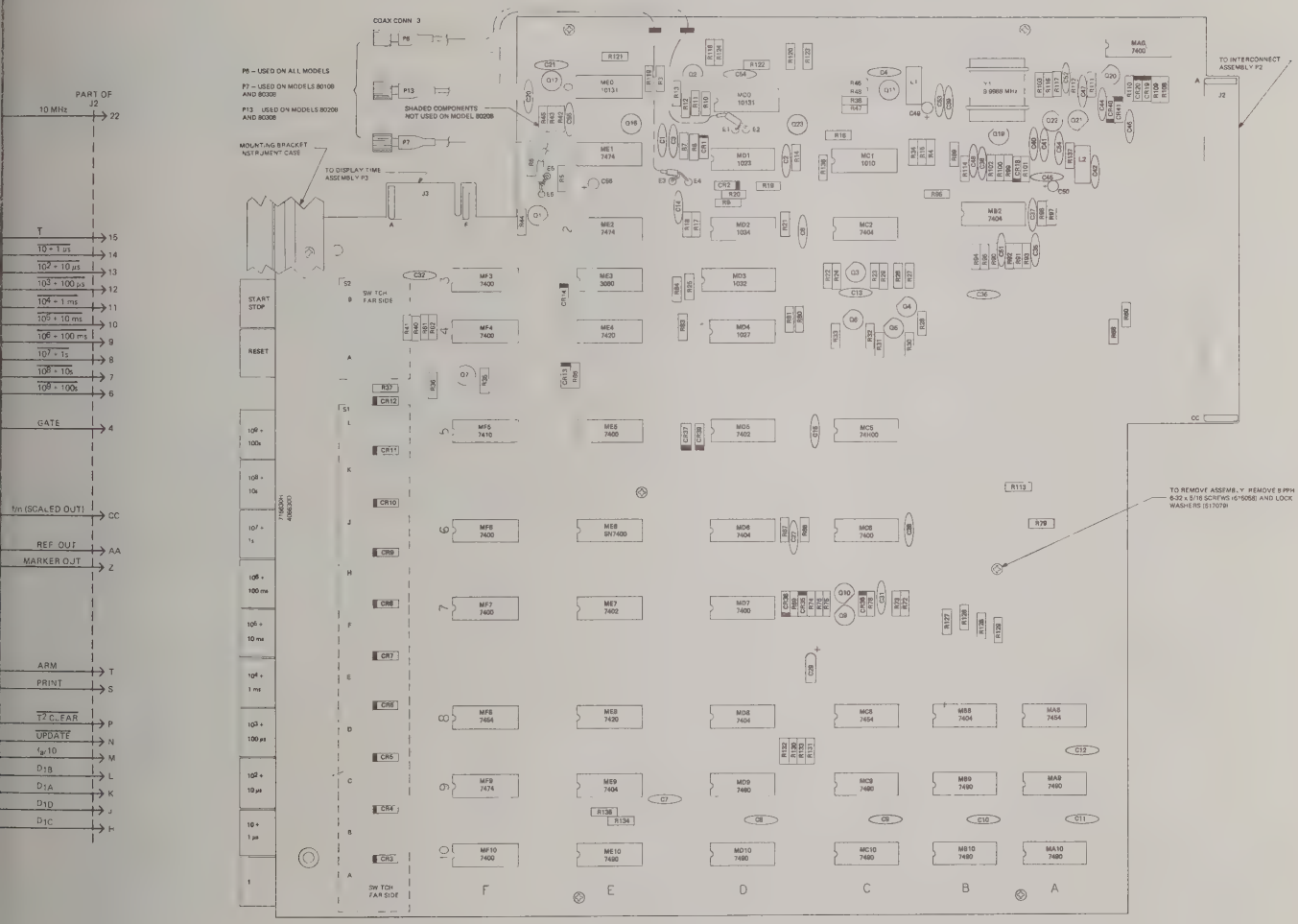
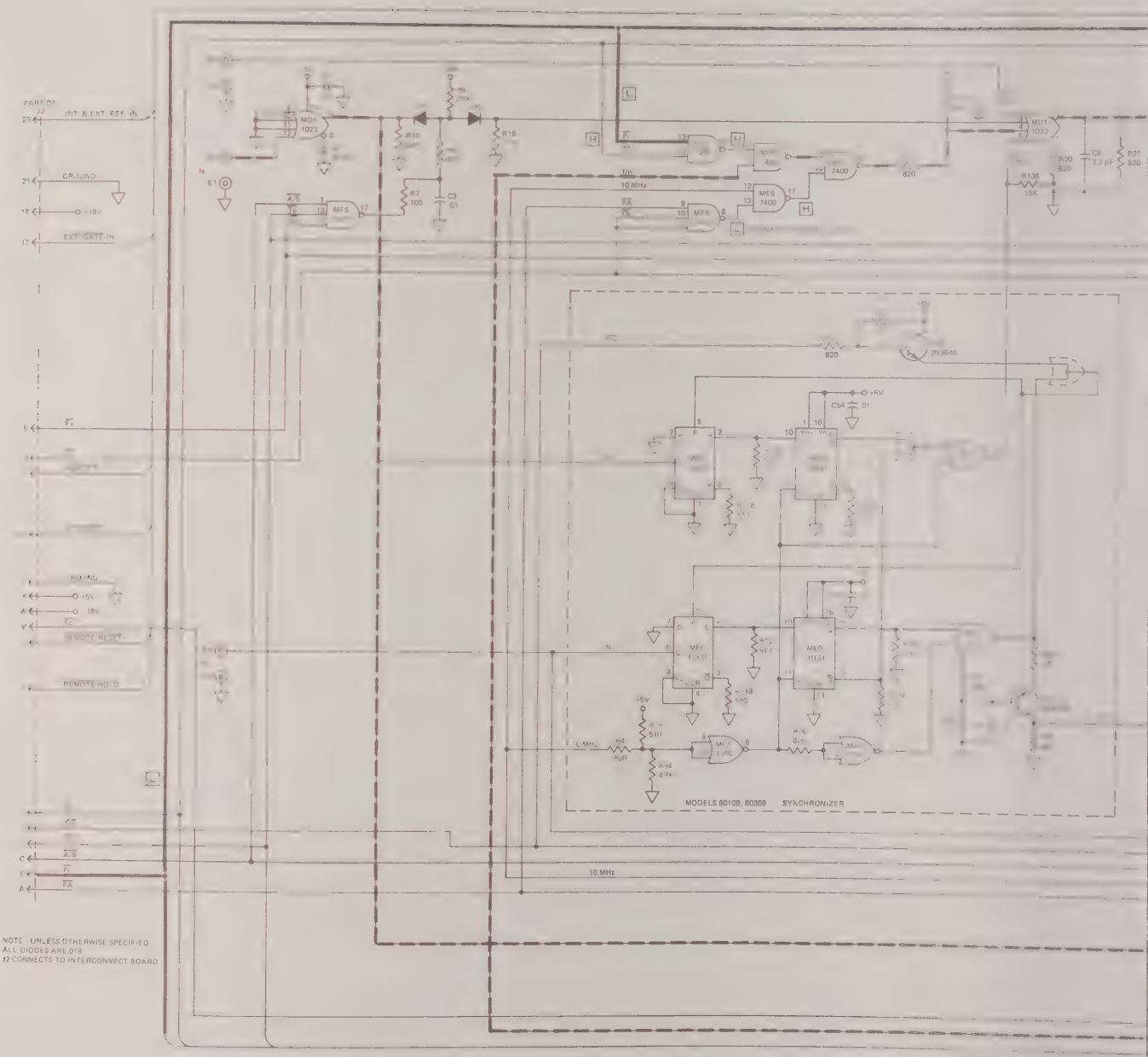
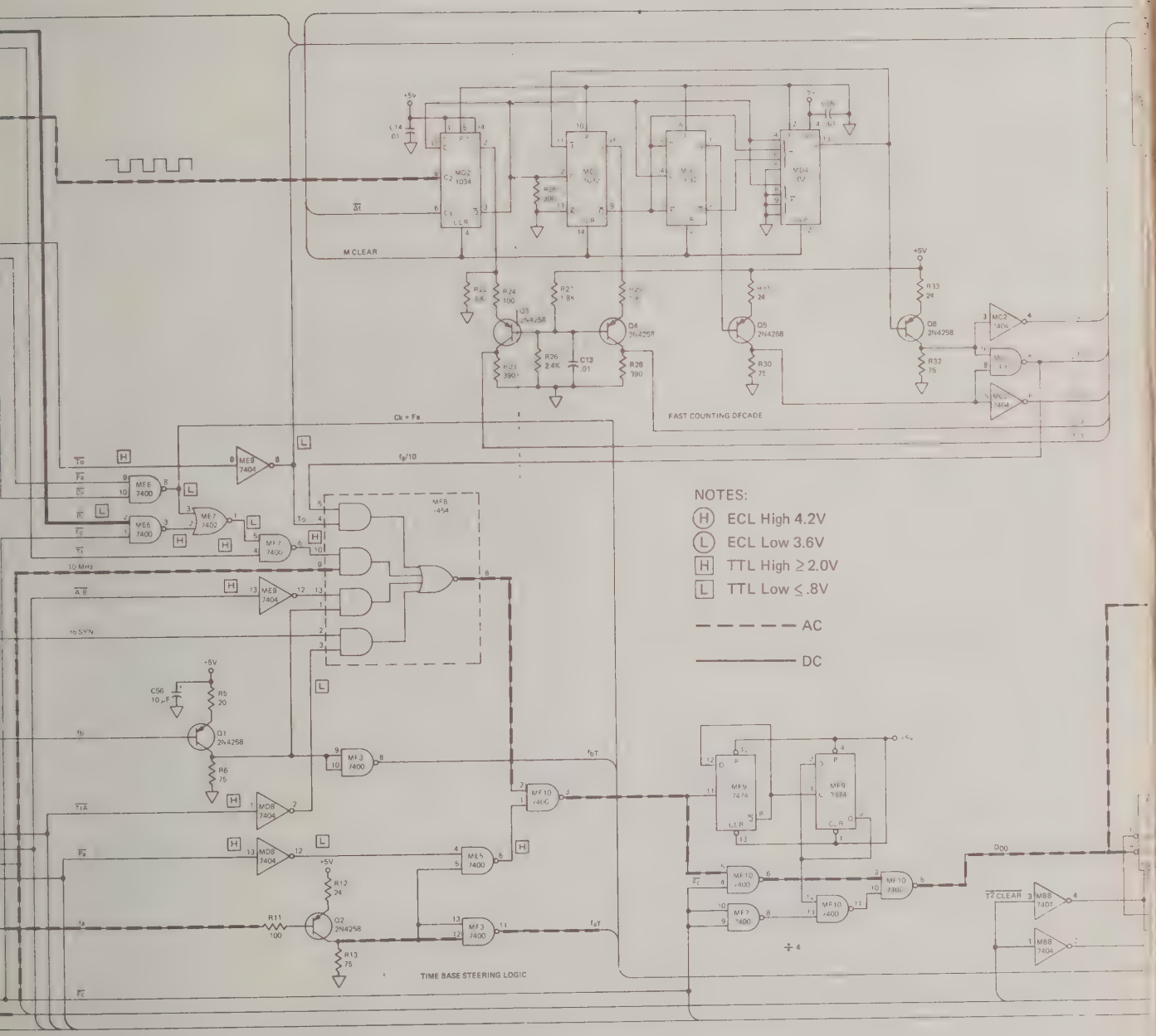
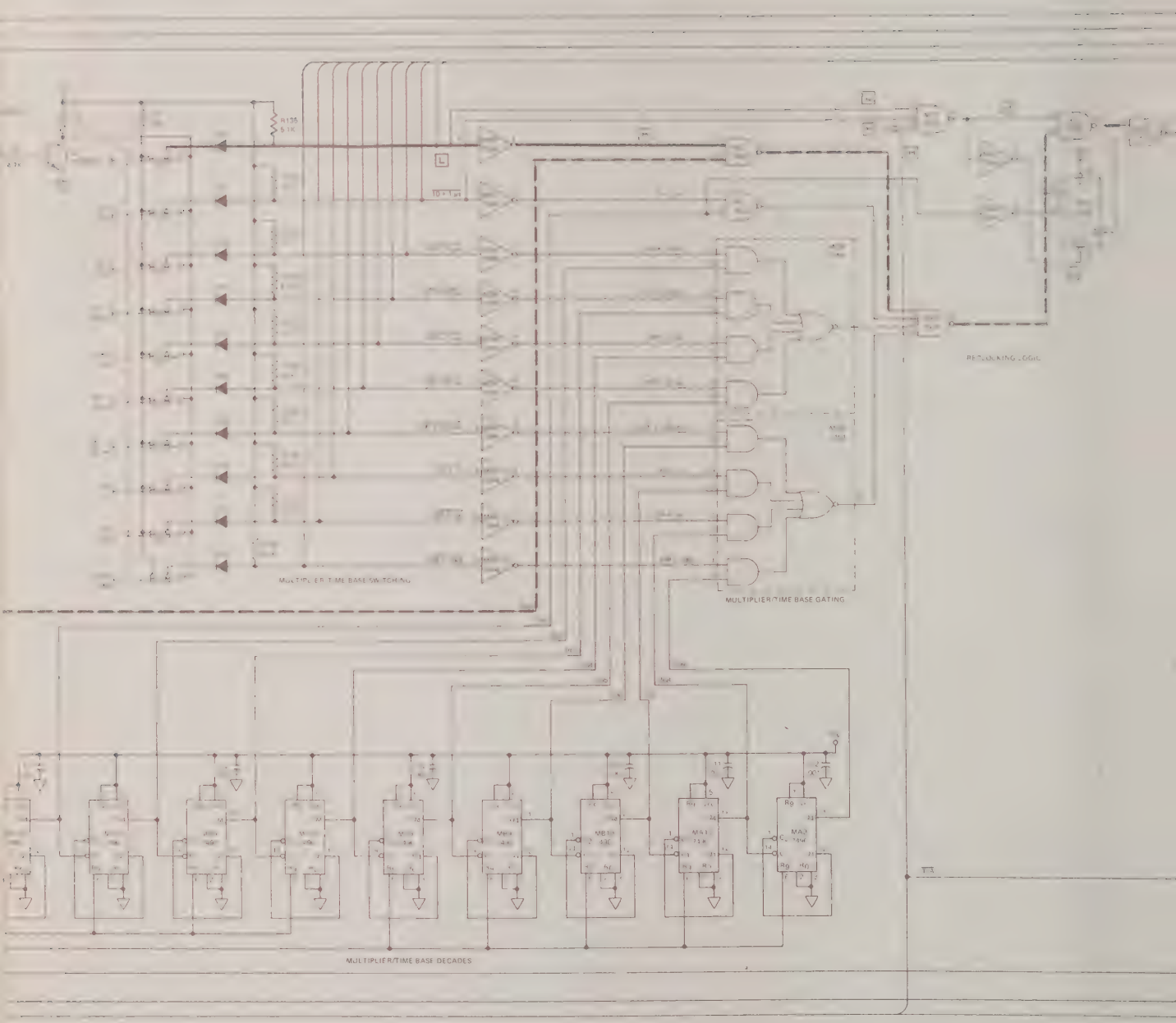


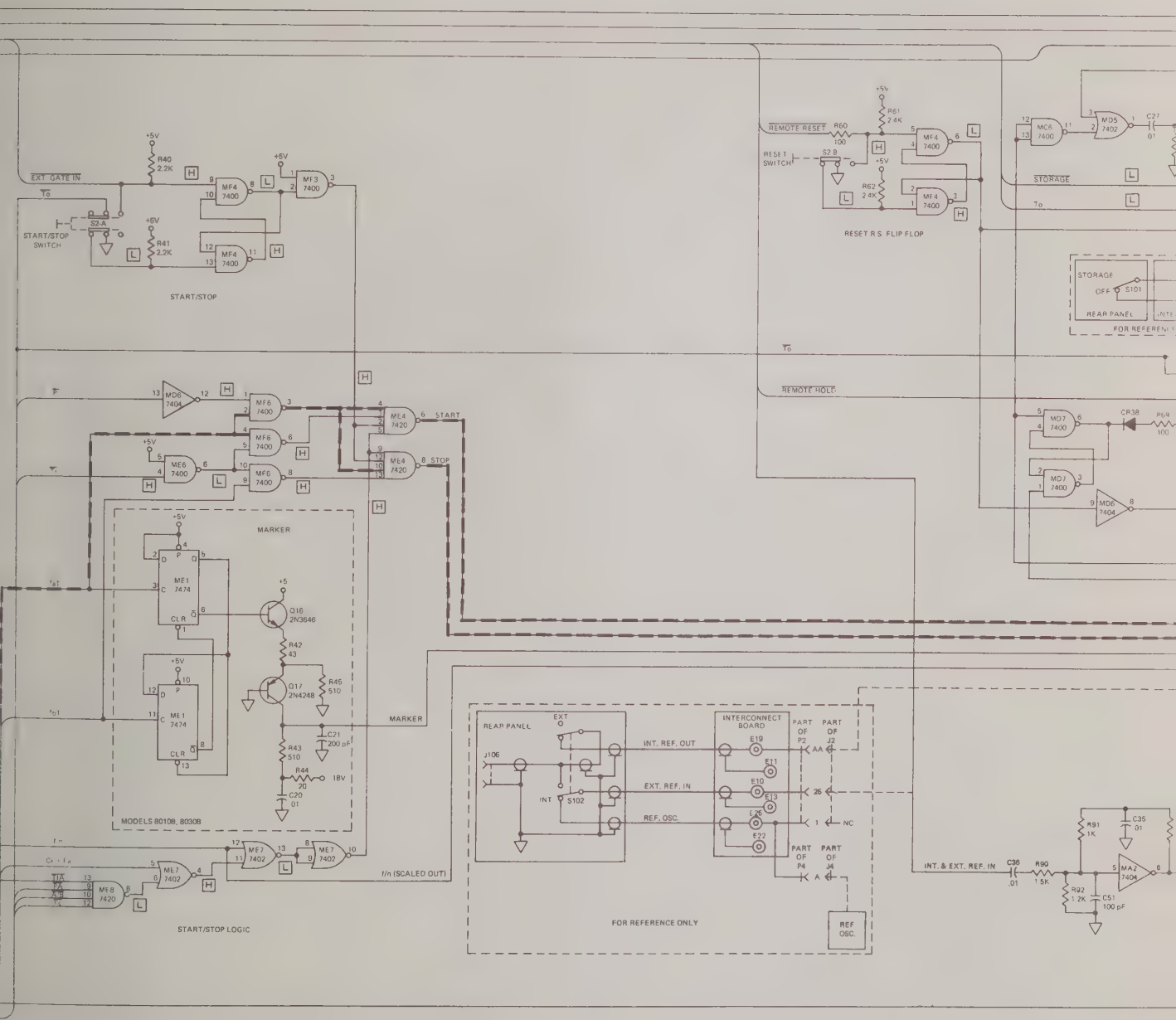
Figure 5.25 - Signal Flow for Check Mode 5-21

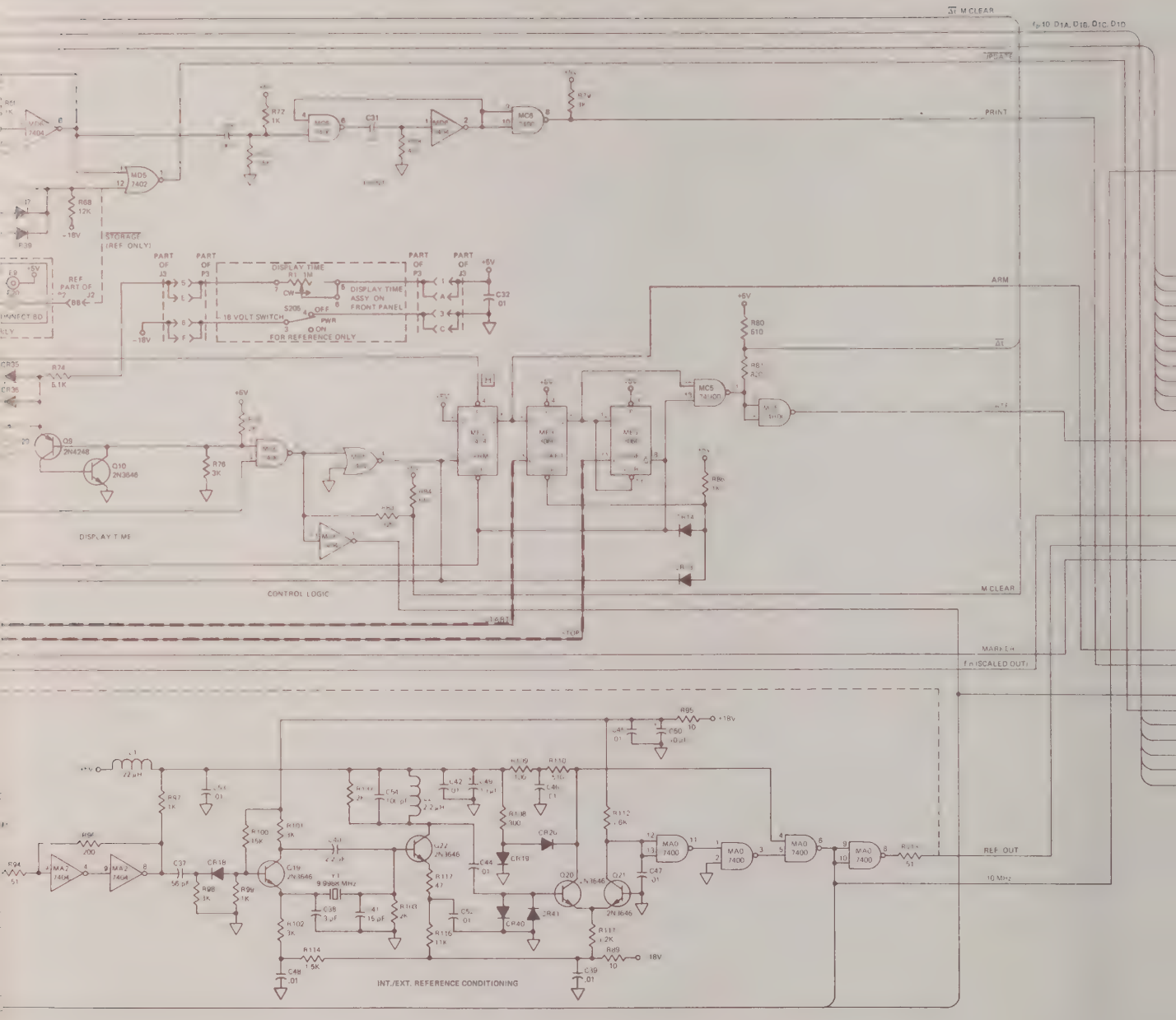

INT & EXT REF IN
GROUND
+18V
EXT GATE IN
REMOTE RESET
REMOTE HOLD
10 MHz
MODELS 8010B, 8030B SYNCHRONIZER
NOTE UNLESS OTHERWISE SPECIFIED
ALL DIODES ARE 018
J2 CONNECTS TO INTERCONNECT BOARD

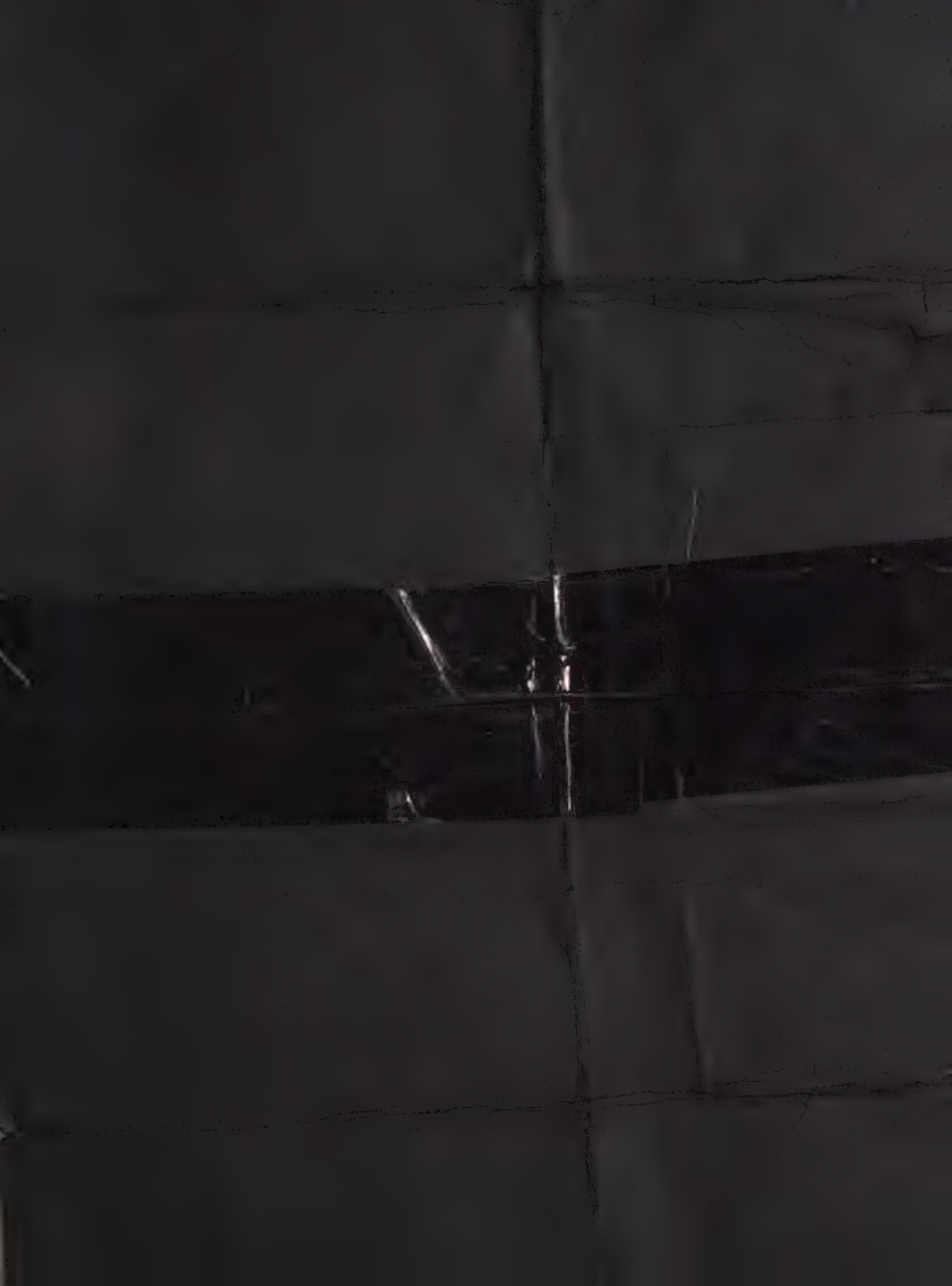

M CLEAR
FAST COUNTING DECADE
Ck + Fa
fp/10
10 MHz
to SYN
TIME BASE STEERING LOGIC
÷ 4
T2 CLEAR
NOTES:
(H) ECL High 4.2V
(L) ECL Low 3.6V
[H] TTL High ≥ 2.0V
[L] TTL Low ≤ .8V
AC
DC

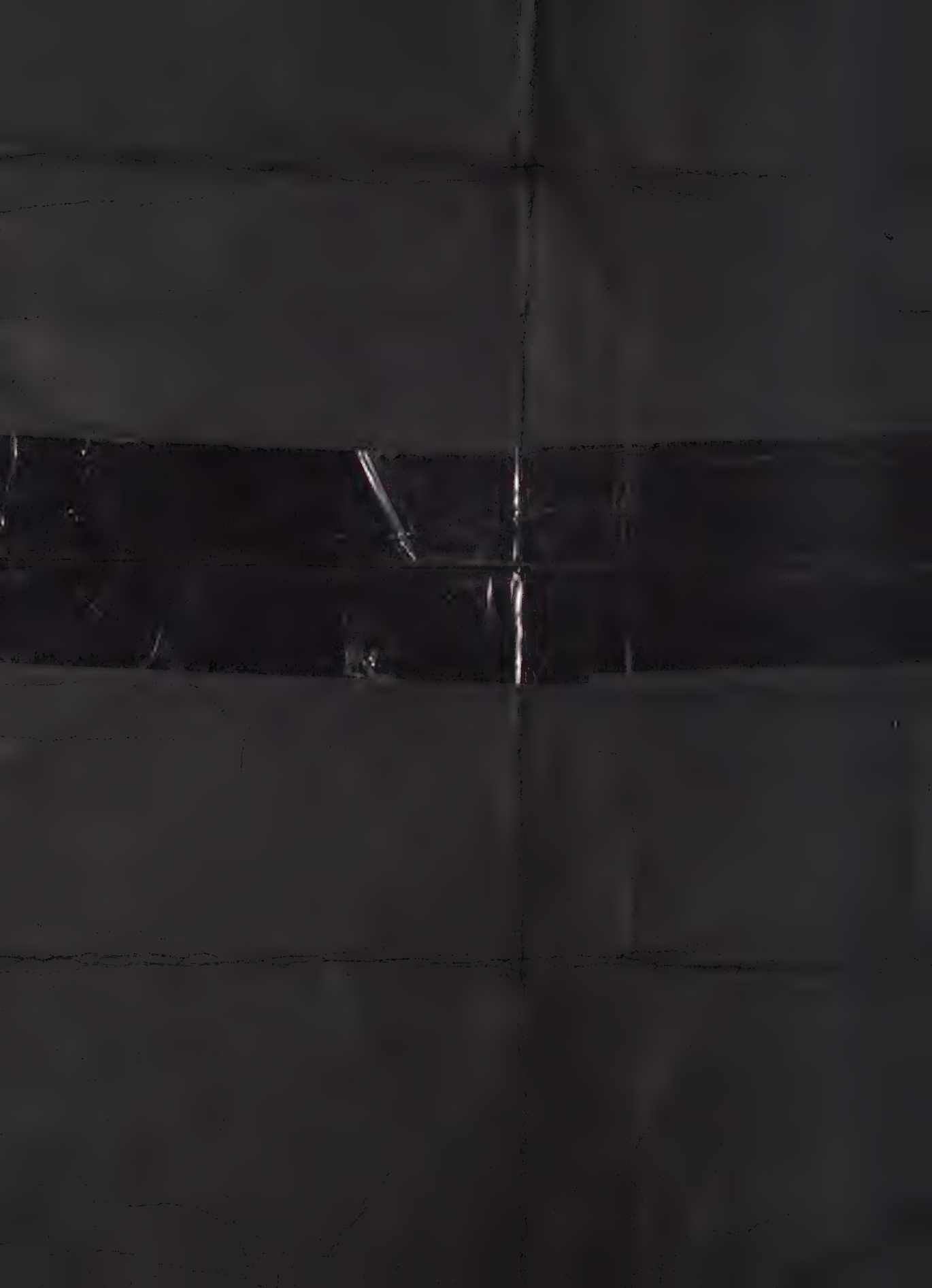


5-22 Figure 5.26 - Signal Flow for Period Mode


EXT. GATE IN
START/STOP SWITCH
S2-A
START/STOP
REMOTE RESET
RESET SWITCH
S2 B
RESET R.S. FLIP FLOP
STORAGE
OFF
S101
REAR PANEL
REMOTE HOLD
START
STOP
MARKER
MODELS 8010B, 8030B
INTERCONNECT BOARD
REAR PANEL
J106
INT
S102
INT. REF. OUT
EXT. REF. IN
REF. OSC.
FOR REFERENCE ONLY
REF OSC.
INT. & EXT. REF. IN
f/n (SCALED OUT)
START/STOP LOGIC


M CLEAR
PRINT
ARM
M CLEAR
MARKER
SCALED OUT
REF OUT
10 MHz
STORAGE (REF ONLY)
DISPLAY TIME
CONTROL LOGIC
INT./EXT. REFERENCE CONDITIONING
18 VOLT SWITCH
FOR REFERENCE ONLY





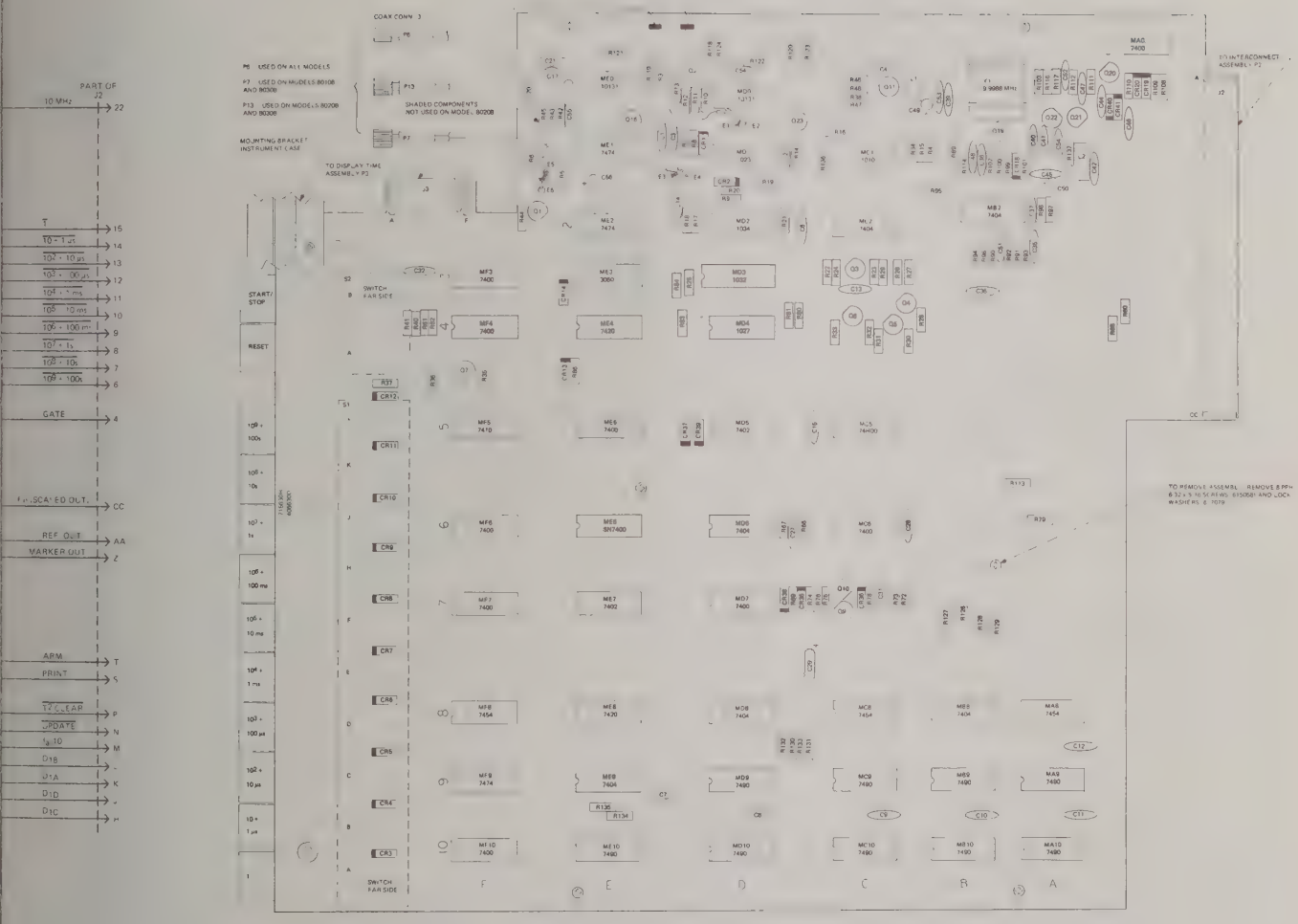
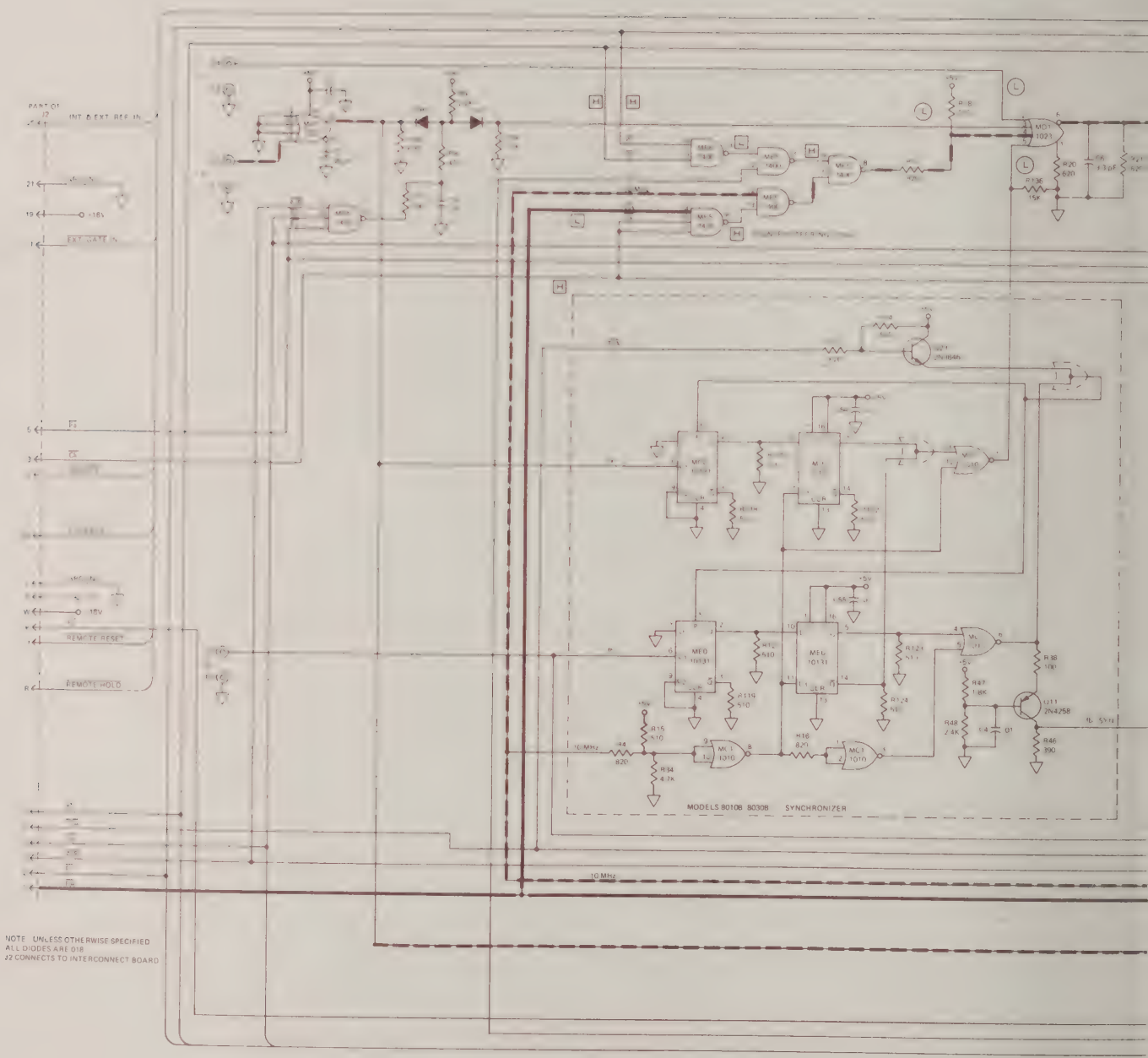
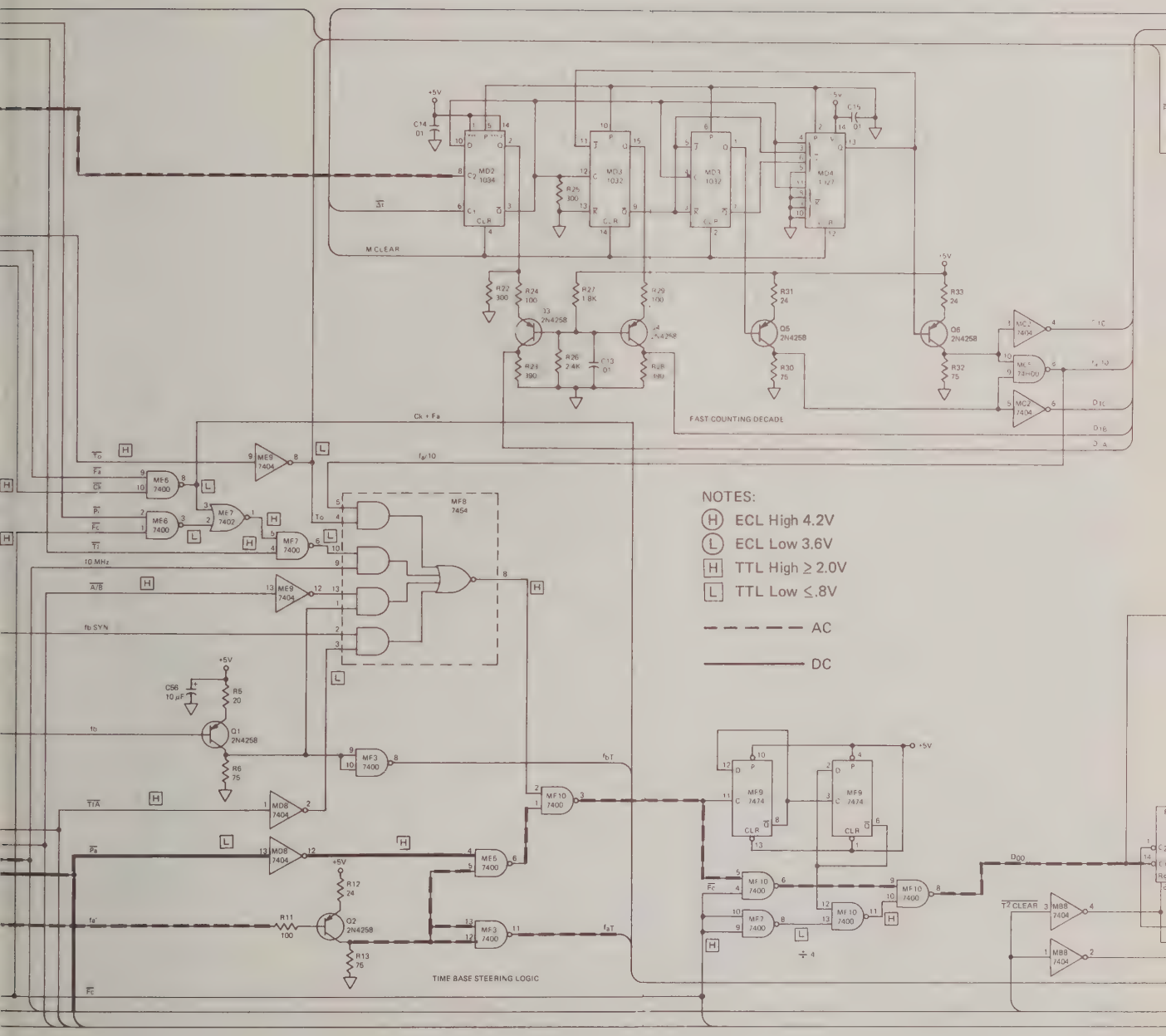
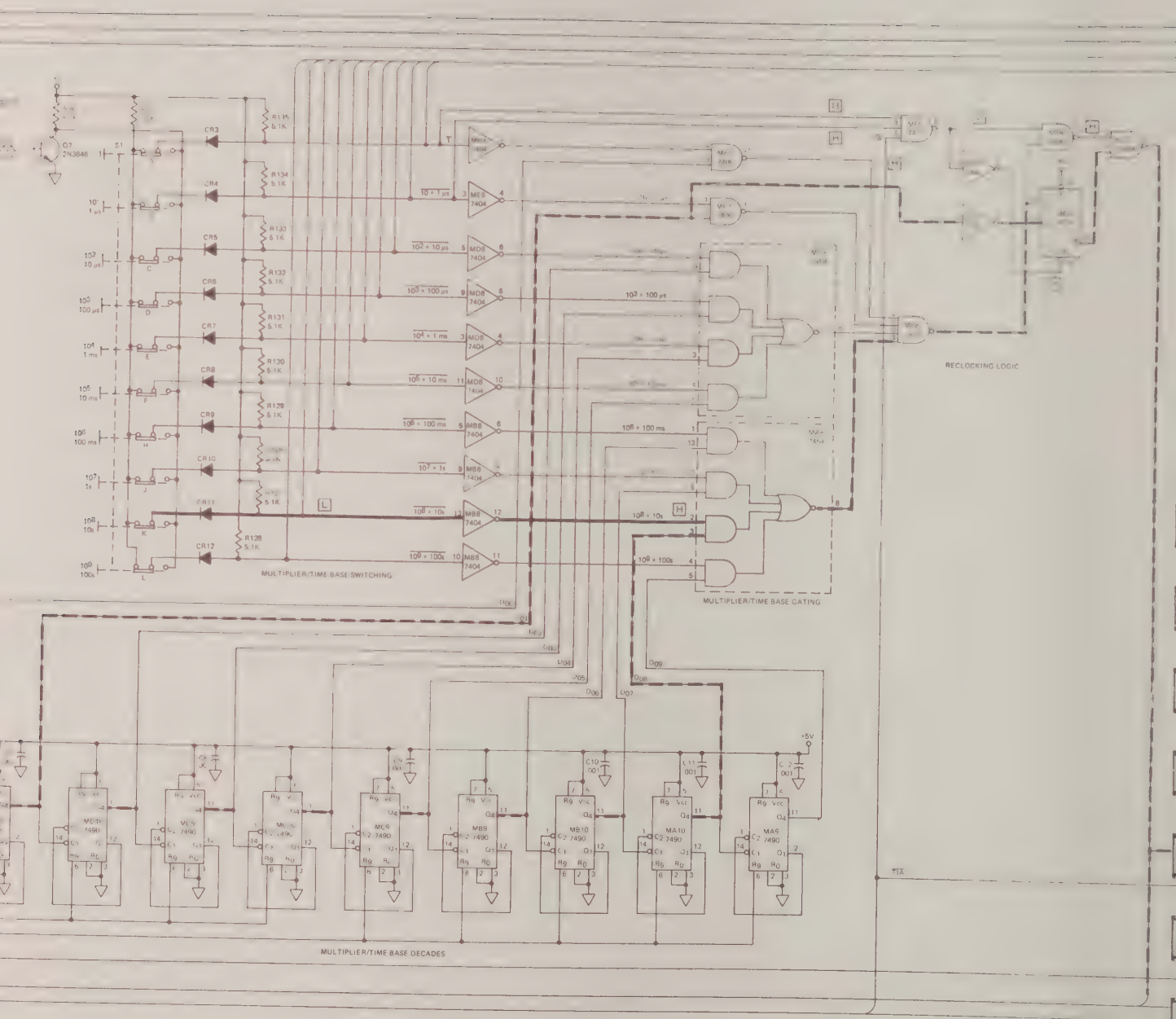


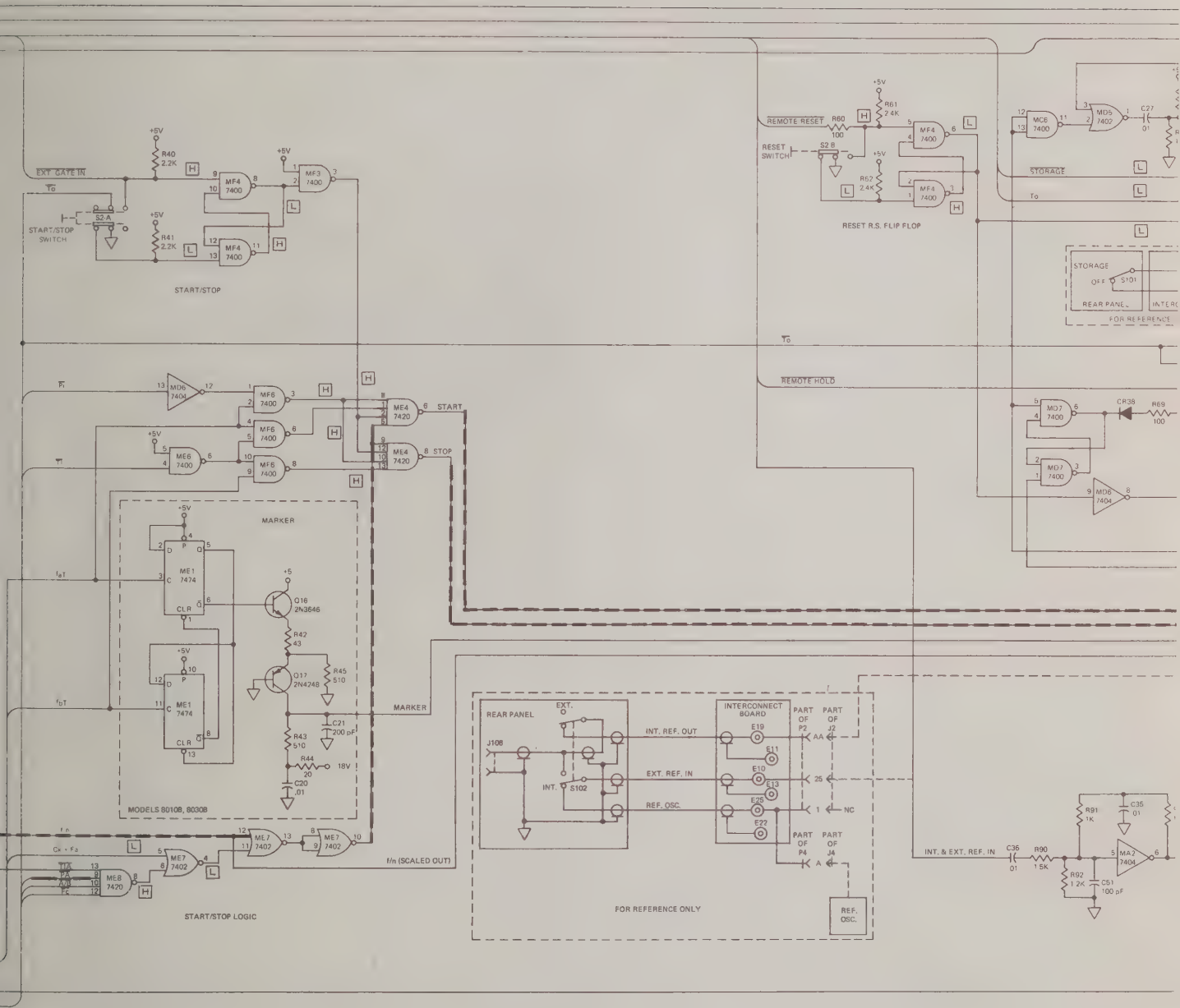
Figure 5.26 - Signal Flow for Period Mode 5-23

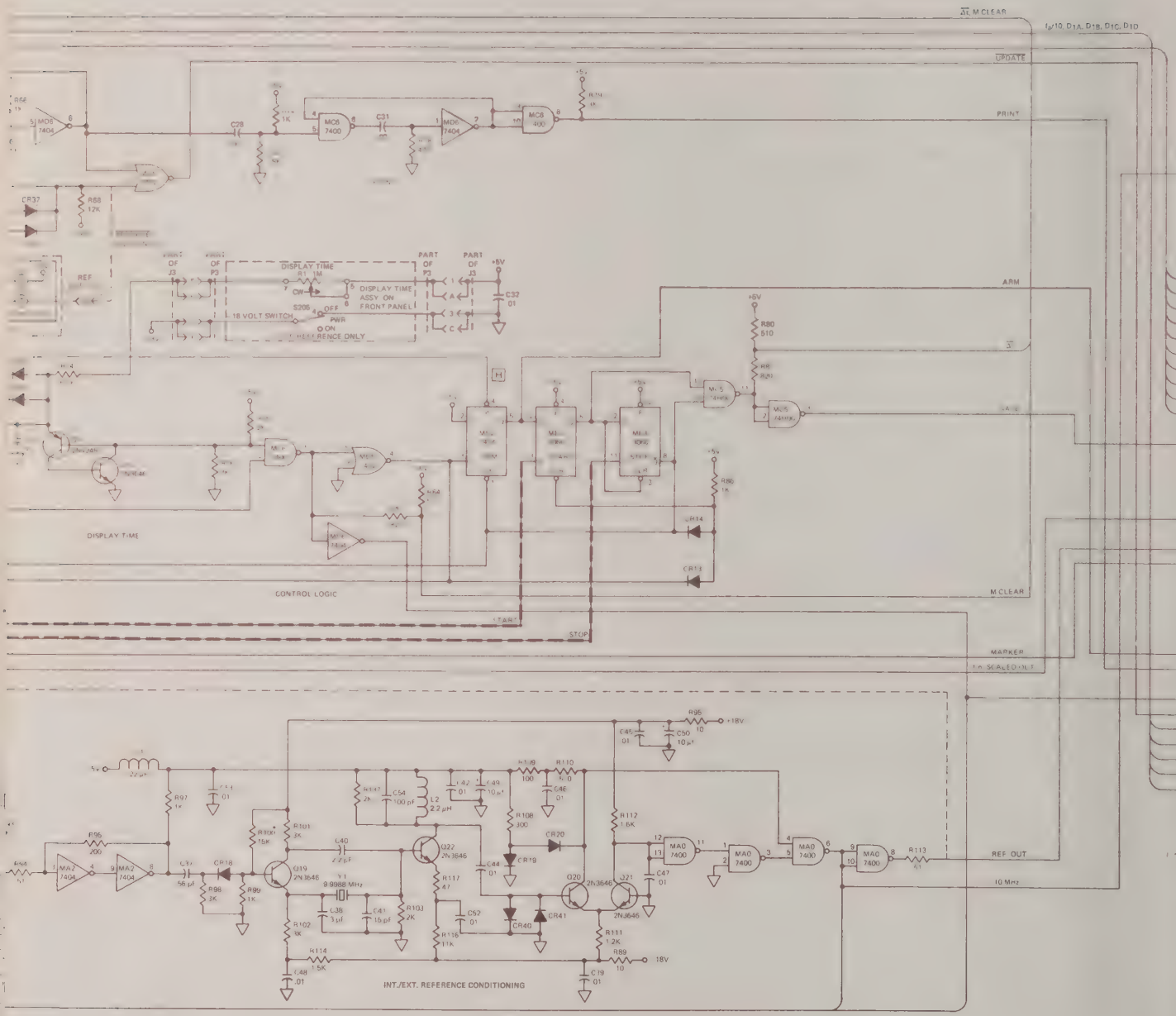

INT & EXT REF IN
EXT GATE IN
REMOTE RESET
REMOTE HOLD
10 MHz
MODELS 8010B 8030B SYNCHRONIZER
NOTE UNLESS OTHERWISE SPECIFIED
ALL DIODES ARE 01B
J2 CONNECTS TO INTERCONNECT BOARD

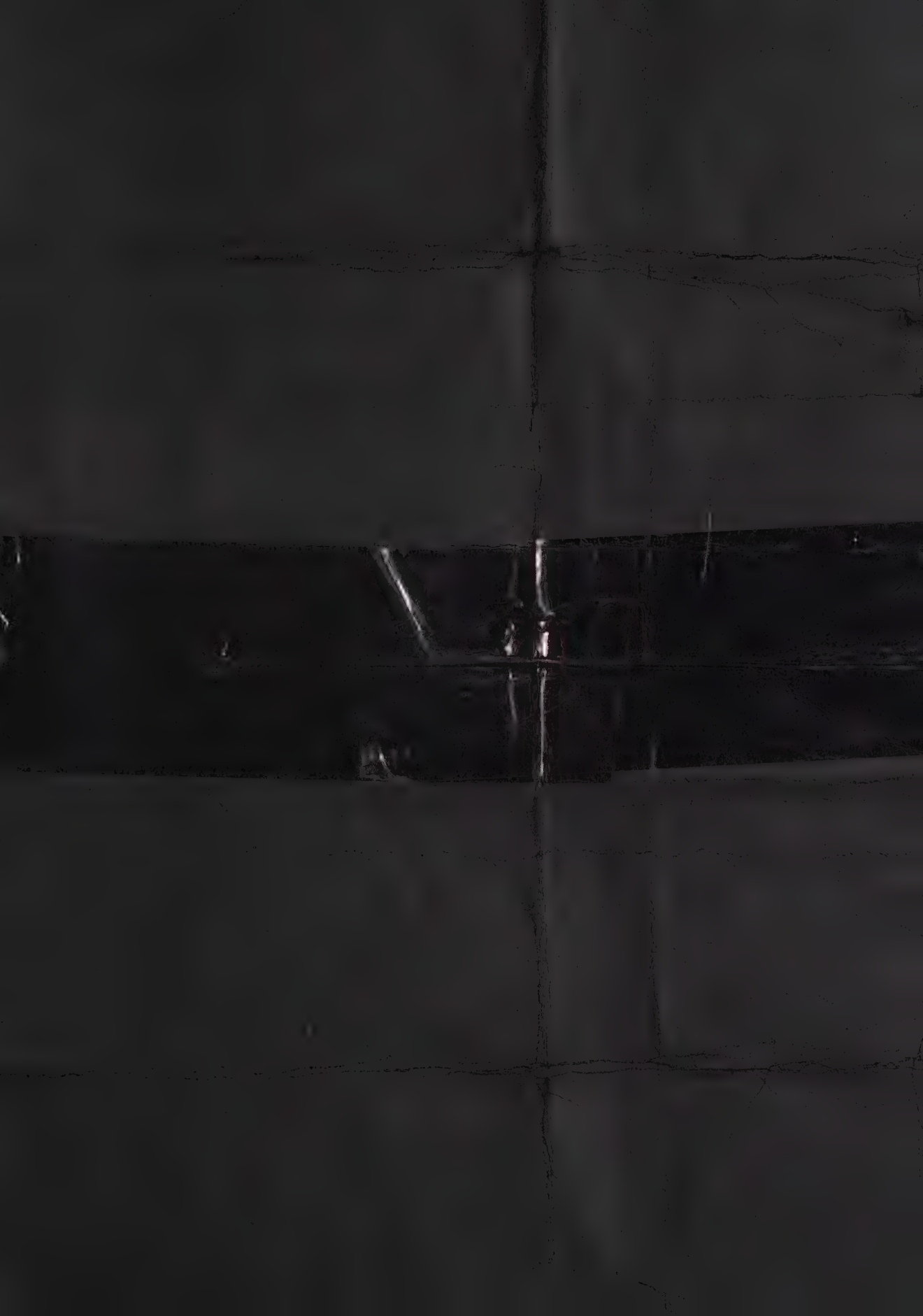

NOTES:
(H) ECL High 4.2V
(L) ECL Low 3.6V
[H] TTL High ≥ 2.0V
[L] TTL Low ≤.8V
AC
DC
FAST COUNTING DECADE
TIME BASE STEERING LOGIC
M CLEAR
Ck + Fa
10 MHz
fb SYN
÷ 4

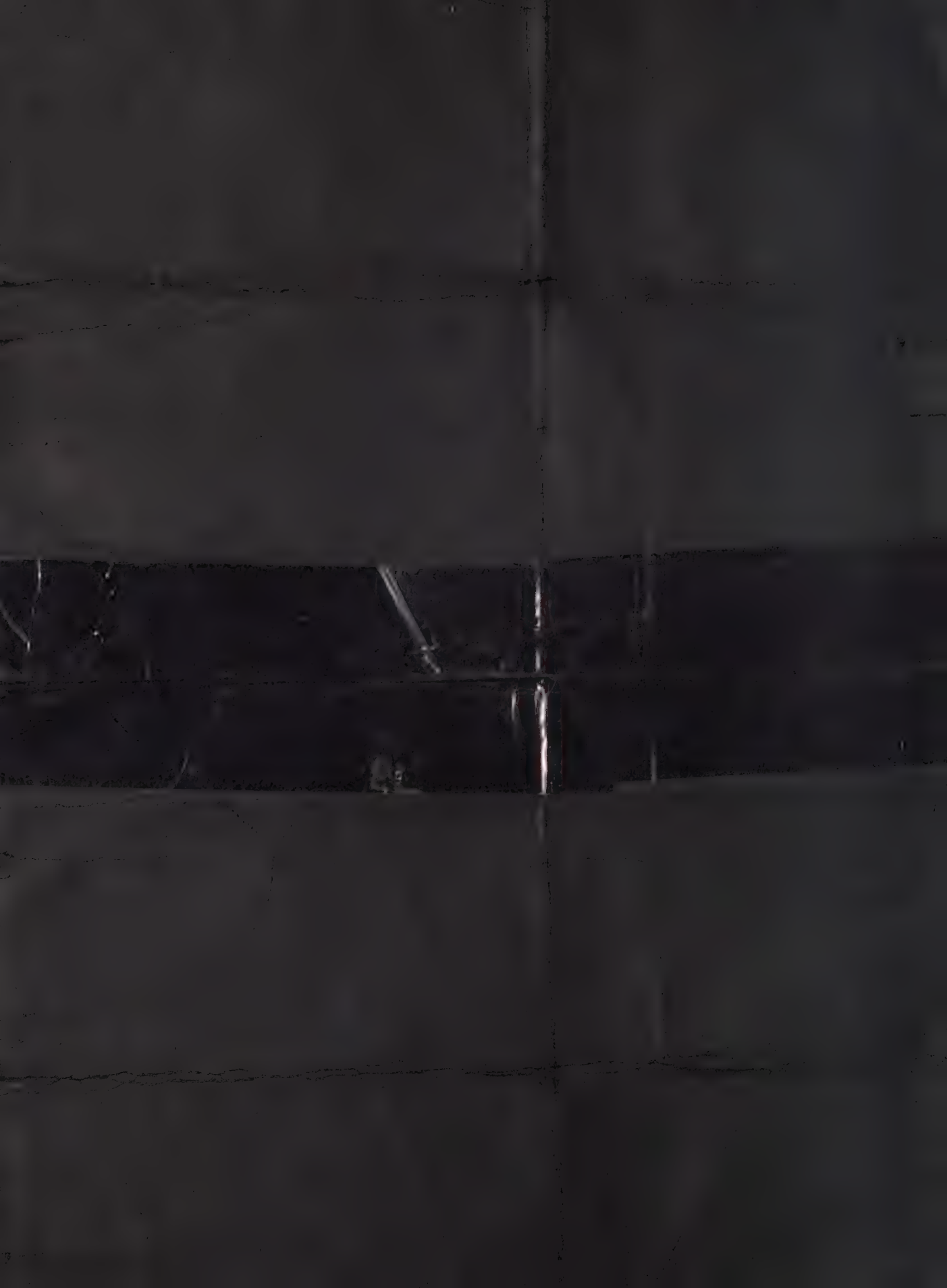


5-24 Figure 5.27 - Signal Flow for Period Average Mode


EXT GATE IN
START/STOP SWITCH
START/STOP
START/STOP LOGIC
MARKER
MODELS 8010B, 8030B
REMOTE RESET
RESET SWITCH
RESET R.S. FLIP FLOP
REMOTE HOLD
STORAGE
REAR PANEL
FOR REFERENCE
START
STOP
REAR PANEL
INTERCONNECT BOARD
INT. REF. OUT
EXT. REF. IN
REF. OSC.
FOR REFERENCE ONLY
REF. OSC.
INT. & EXT. REF. IN
f/n (SCALED OUT)
MARKER


M CLEAR
UPDATE
PRINT
ARM
MARKER
REF OUT
10 MHz
DISPLAY TIME
CONTROL LOGIC
INT./EXT. REFERENCE CONDITIONING





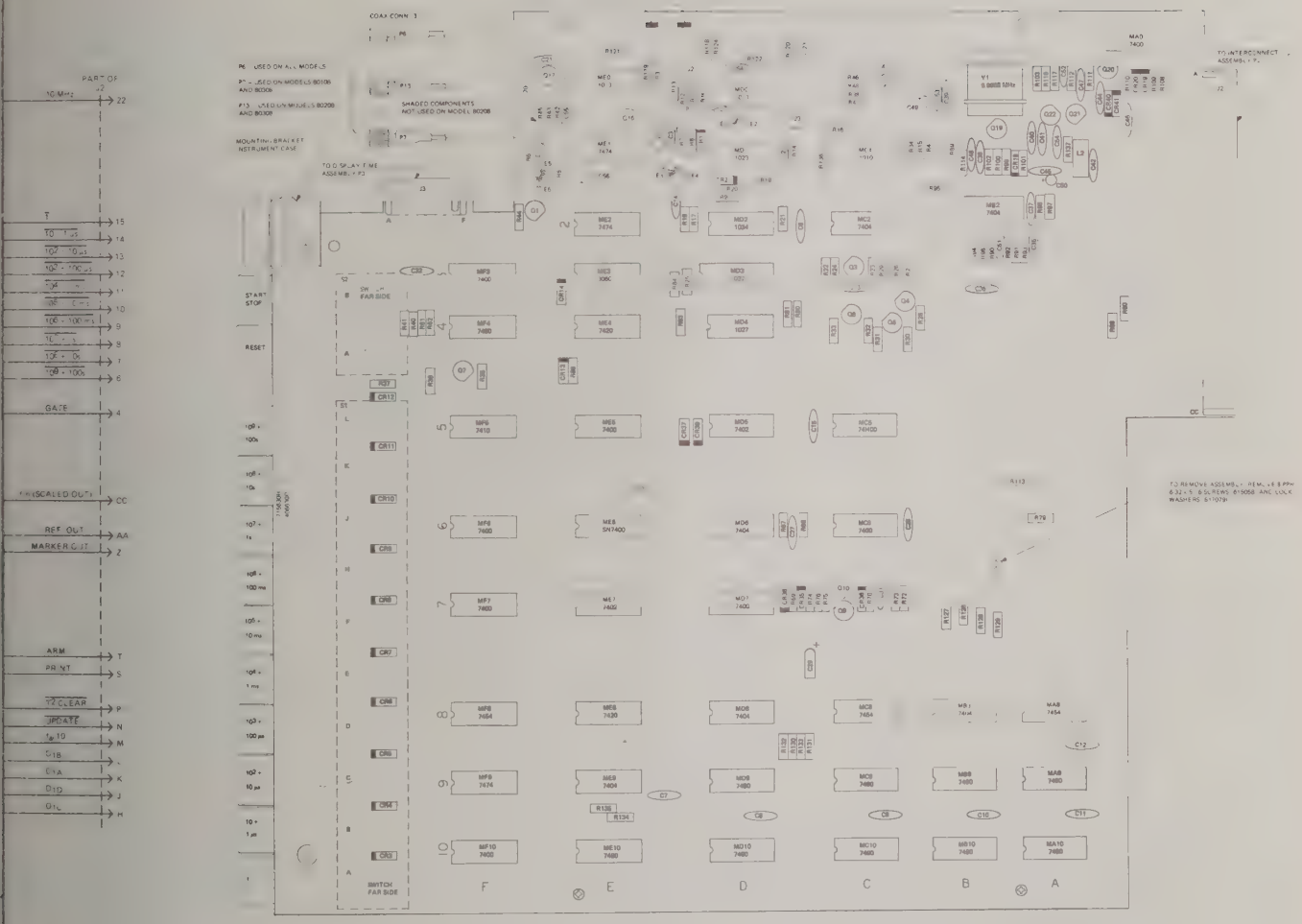
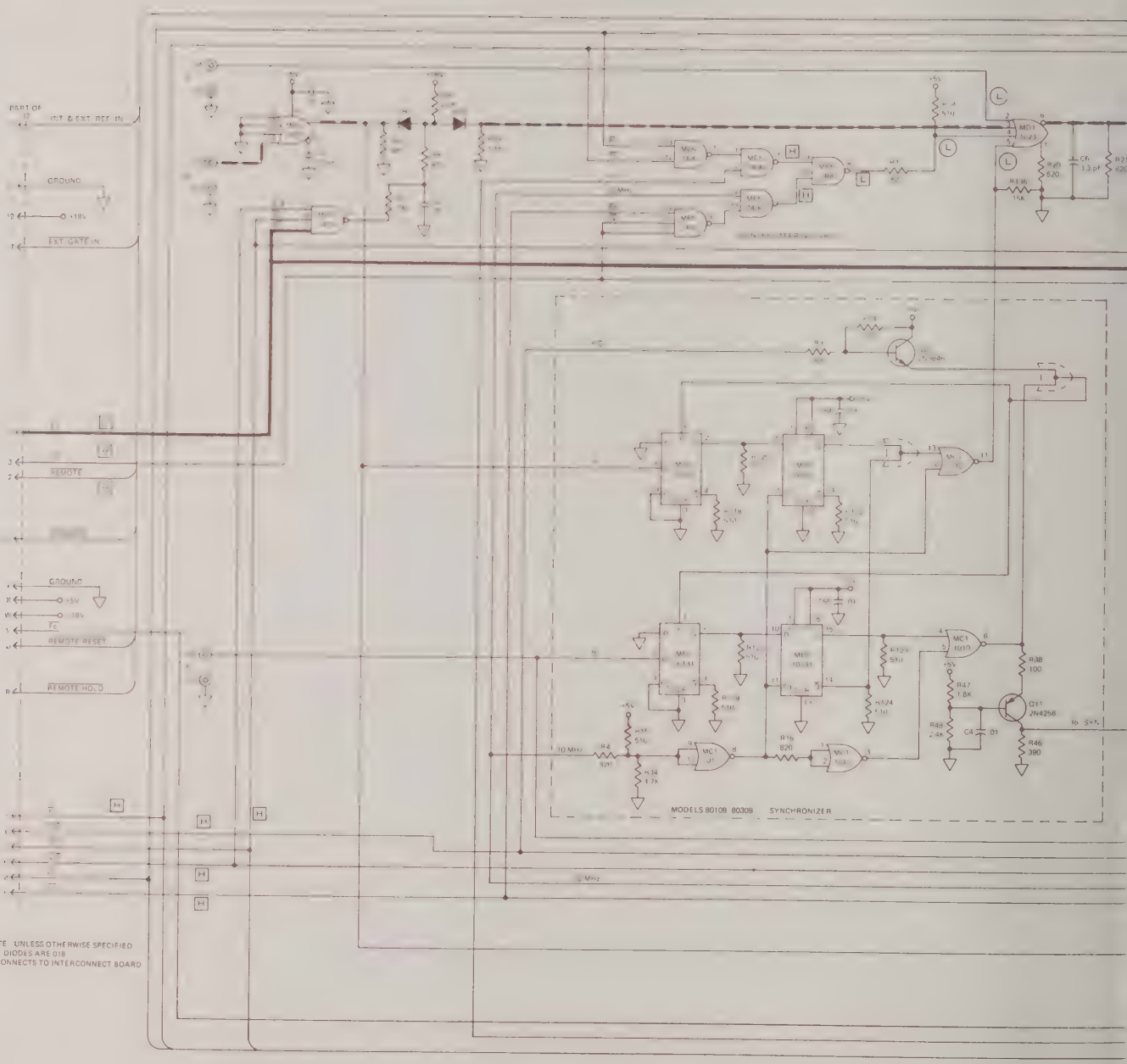
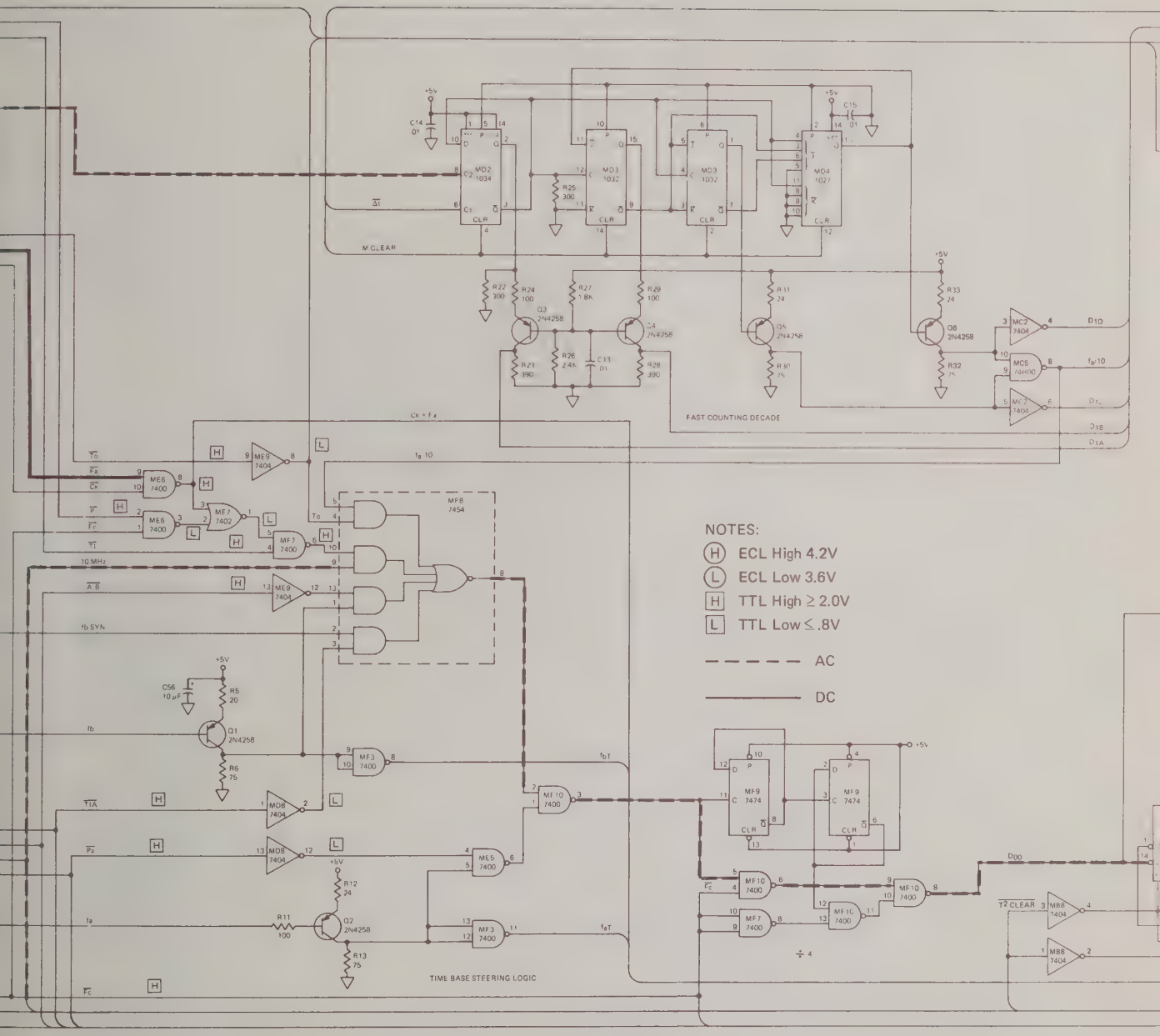
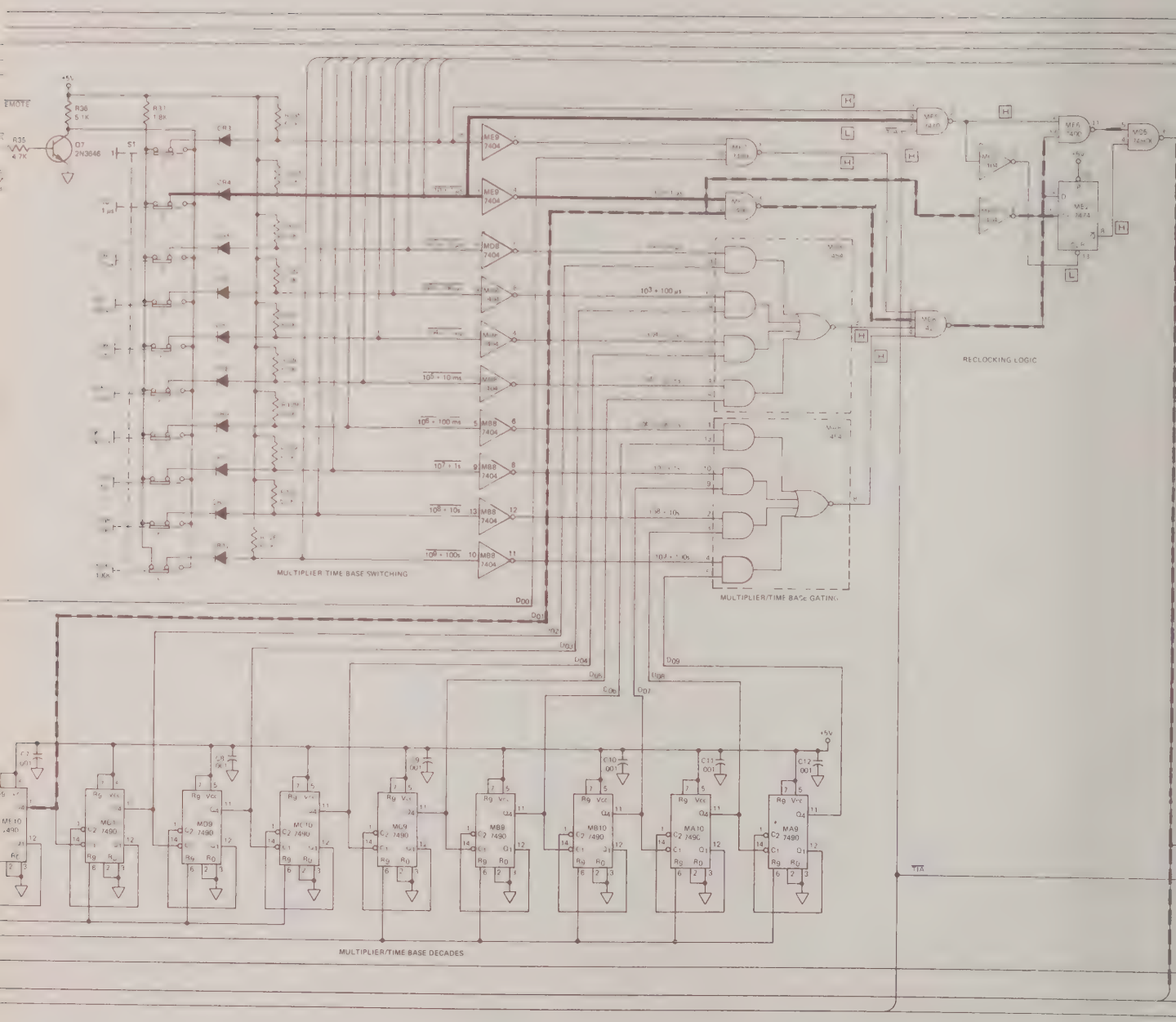


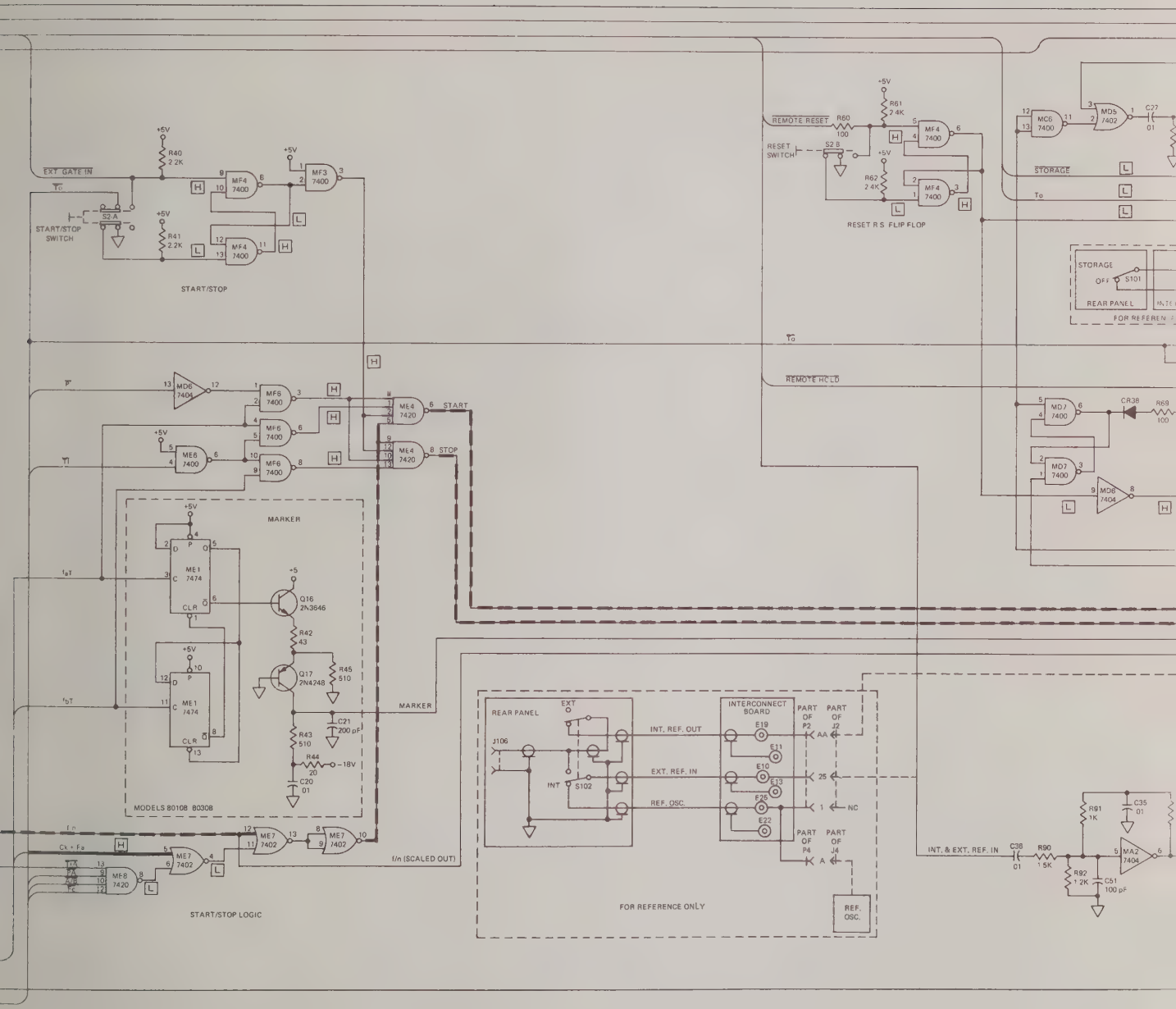
Figure 5.27 - Signal Flow for Period Average Mode 5-25

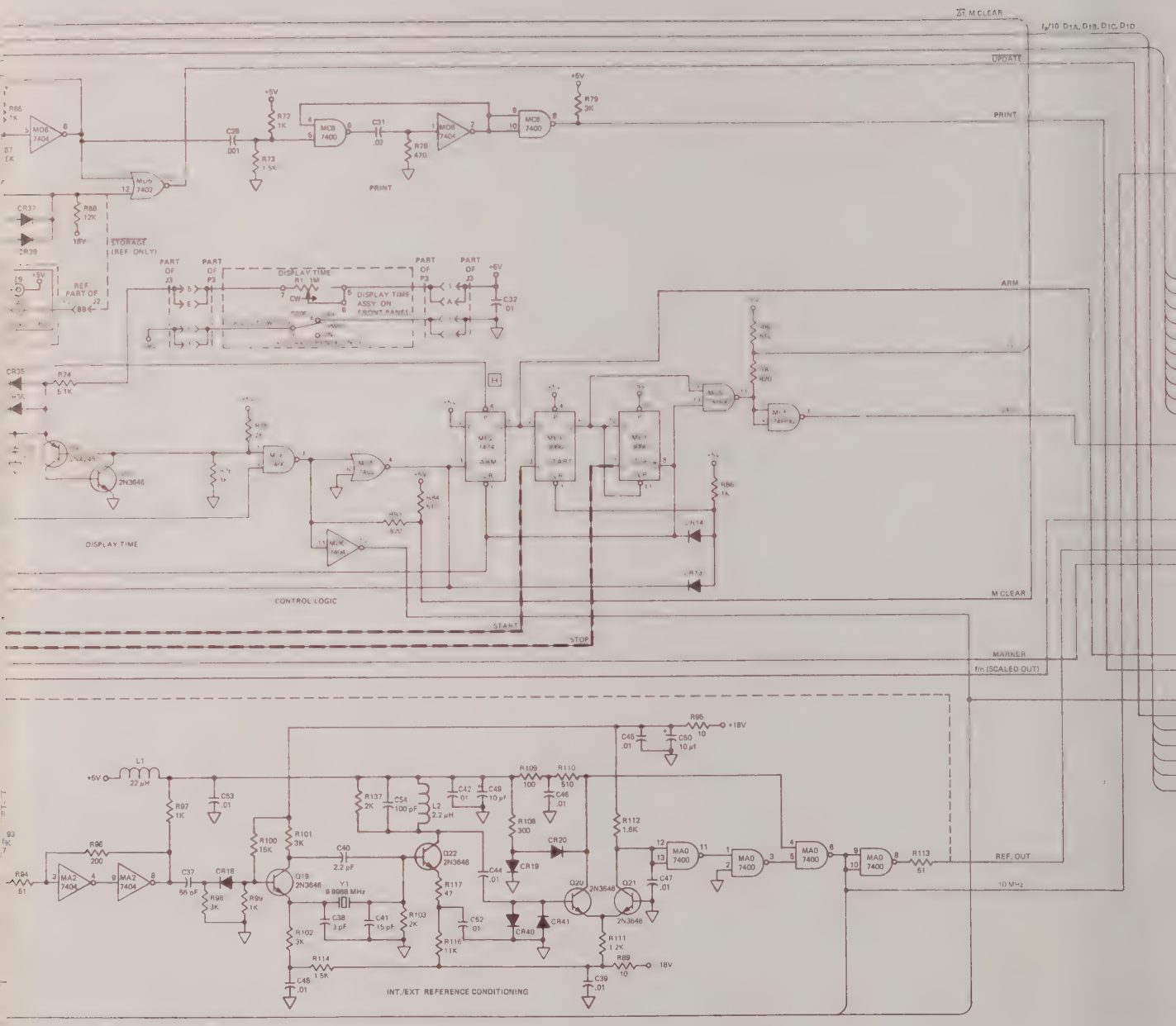

PART OF
INT & EXT REF IN
GROUND
+18V
EXT GATE IN
REMOTE
GROUND
+5V
-18V
REMOTE RESET
REMOTE HOLD
10 MHz
1 MHz
MODELS 80108 80308 SYNCHRONIZER
To SYN
2N4258
NOTE UNLESS OTHERWISE SPECIFIED
ALL DIODES ARE 018
J2 CONNECTS TO INTERCONNECT BOARD

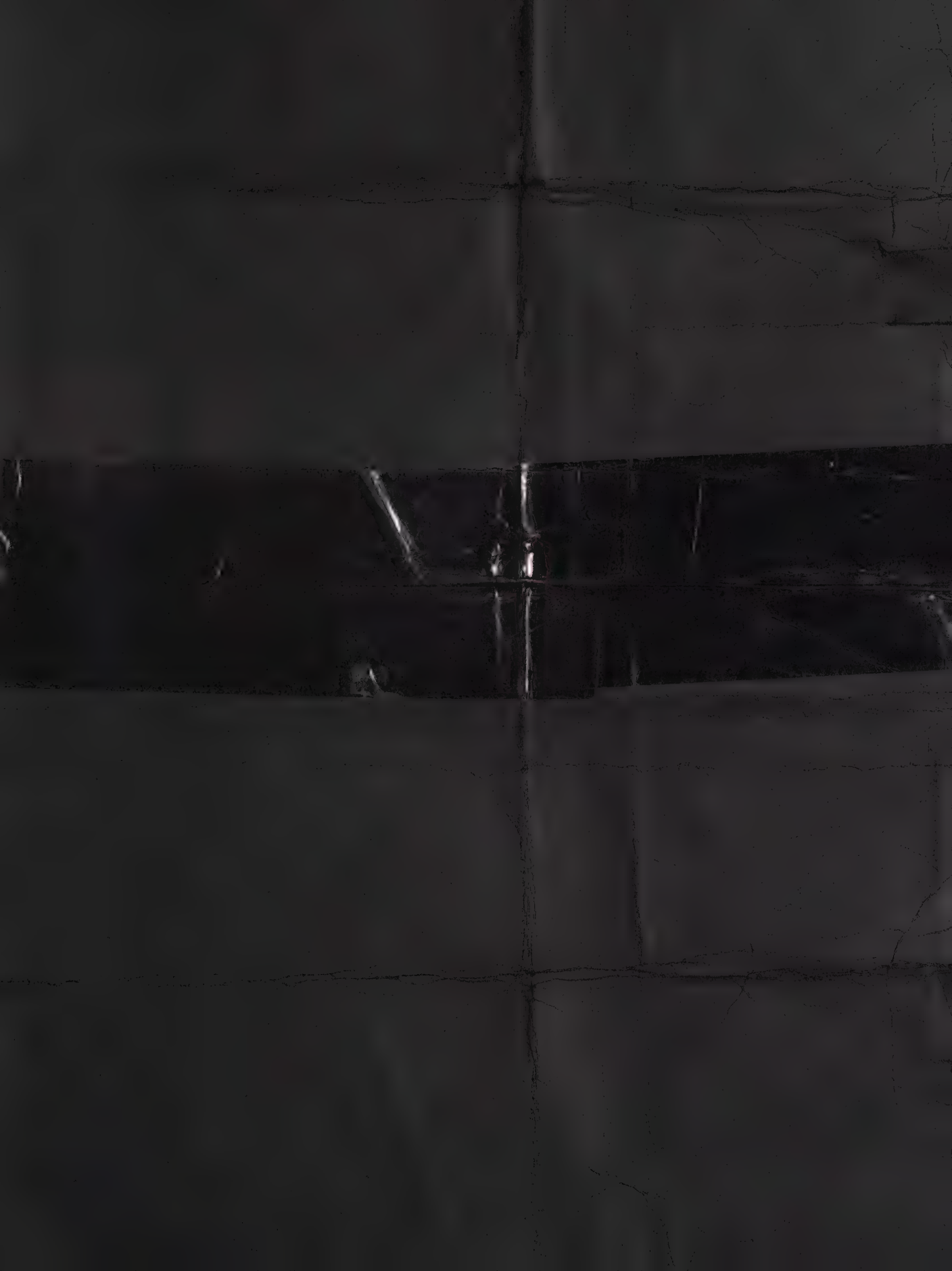

NOTES:
H ECL High 4.2V
L ECL Low 3.6V
H TTL High ≥ 2.0V
L TTL Low ≤ .8V
AC
DC
FAST COUNTING DECADE
TIME BASE STEERING LOGIC
M CLEAR
÷ 4

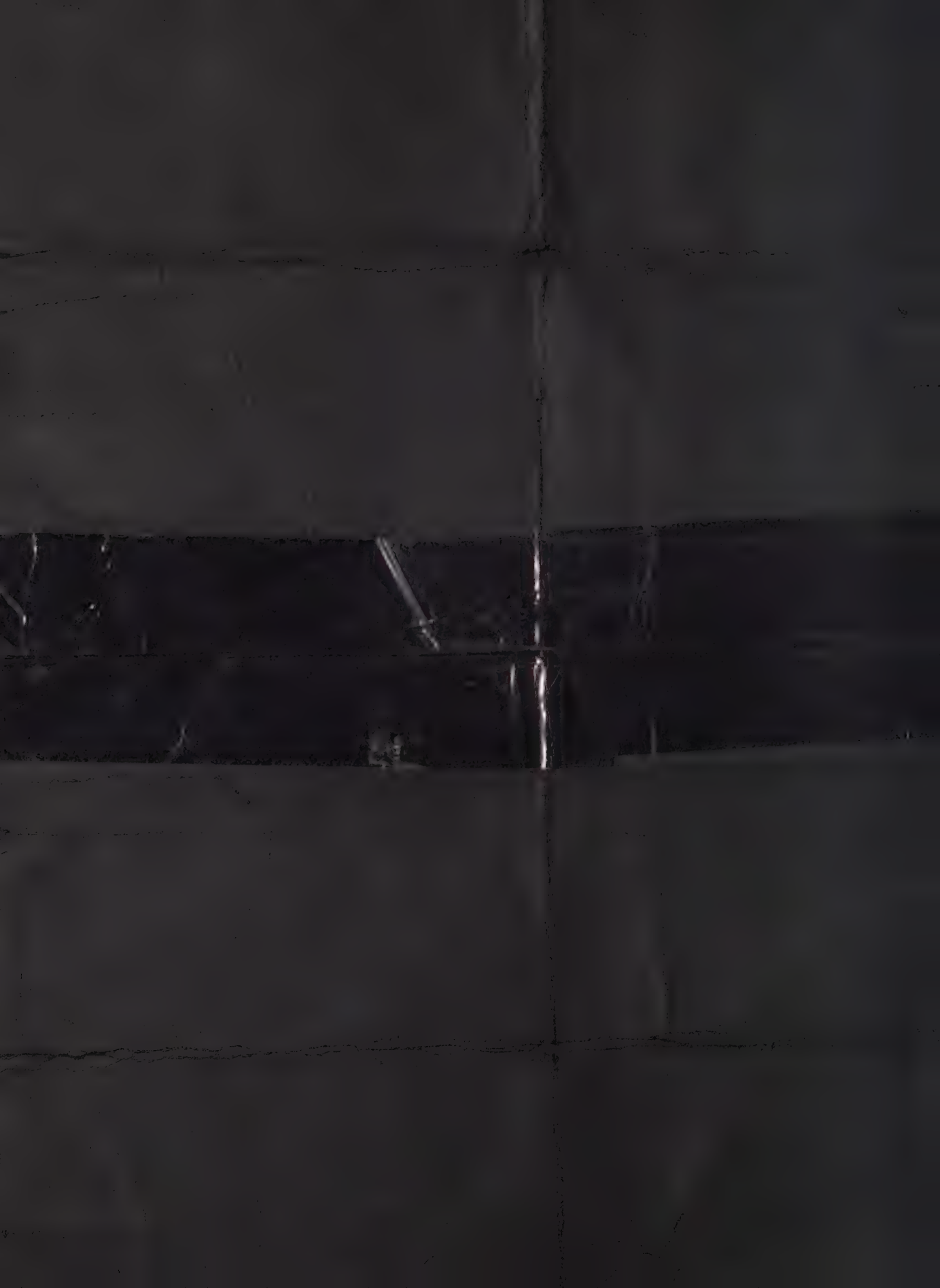


5-26 Figure 5.28 - Signal Flow for Frequency A Mode


EXT GATE IN
START/STOP SWITCH
START/STOP
REMOTE RESET
RESET SWITCH
RESET R S FLIP FLOP
STORAGE
REAR PANEL
REMOTE HOLD
START
STOP
MARKER
MODELS 8010B 8030B
START/STOP LOGIC
f/n (SCALED OUT)
REAR PANEL
INTERCONNECT BOARD
INT. REF. OUT
EXT. REF. IN
REF. OSC.
FOR REFERENCE ONLY
INT. & EXT. REF. IN


M CLEAR
UPDATE
PRINT
ARM
M CLEAR
MARKER
f/n (SCALED OUT)
START
STOP
CONTROL LOGIC
DISPLAY TIME
INT./EXT REFERENCE CONDITIONING
REF. OUT
10 MHz
+5V
+18V
18V
PART OF J3
PART OF P3
DISPLAY TIME ASSY ON FRONT PANEL
STORAGE (REF ONLY)
2N3646
9.9988 MHz





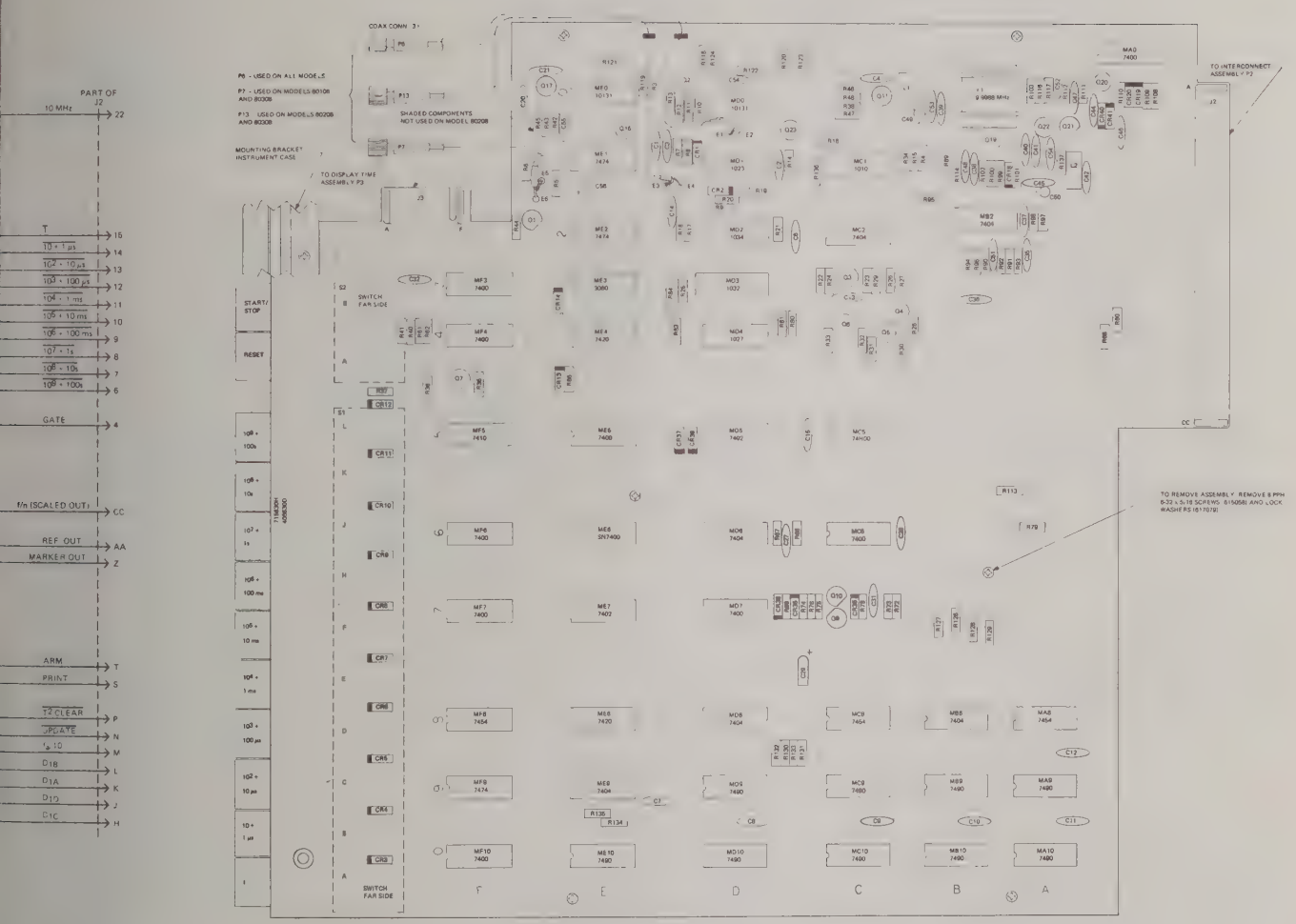
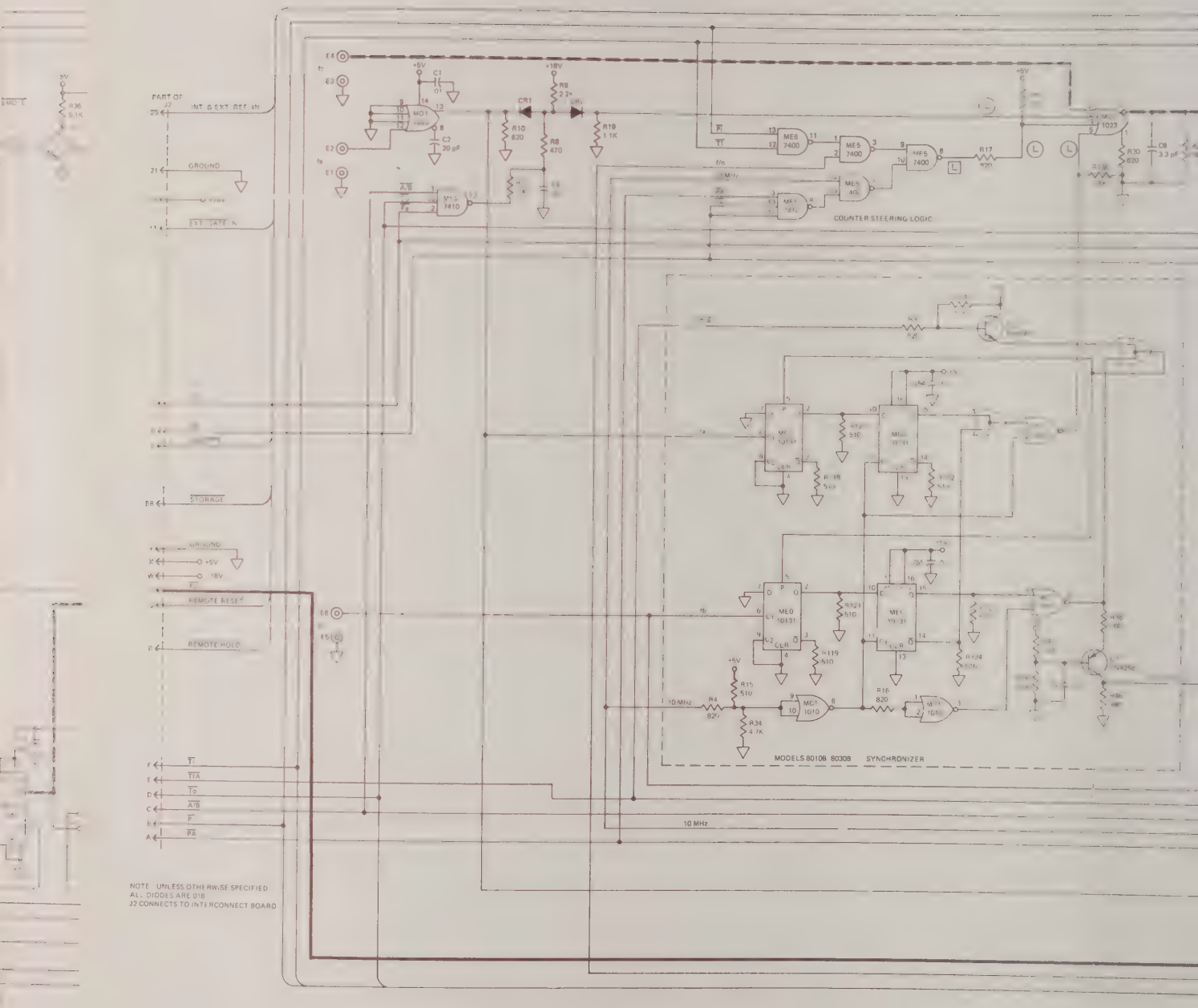
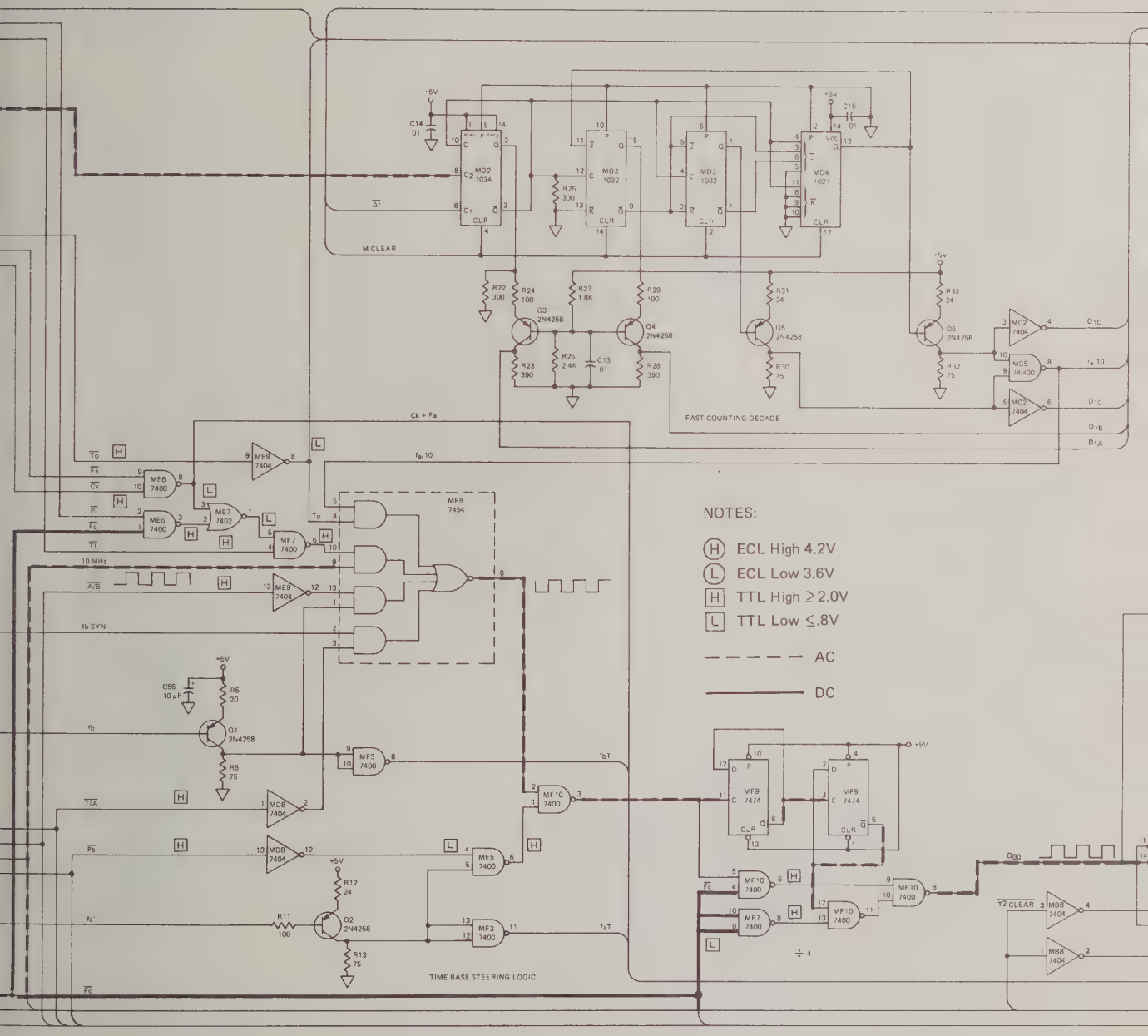
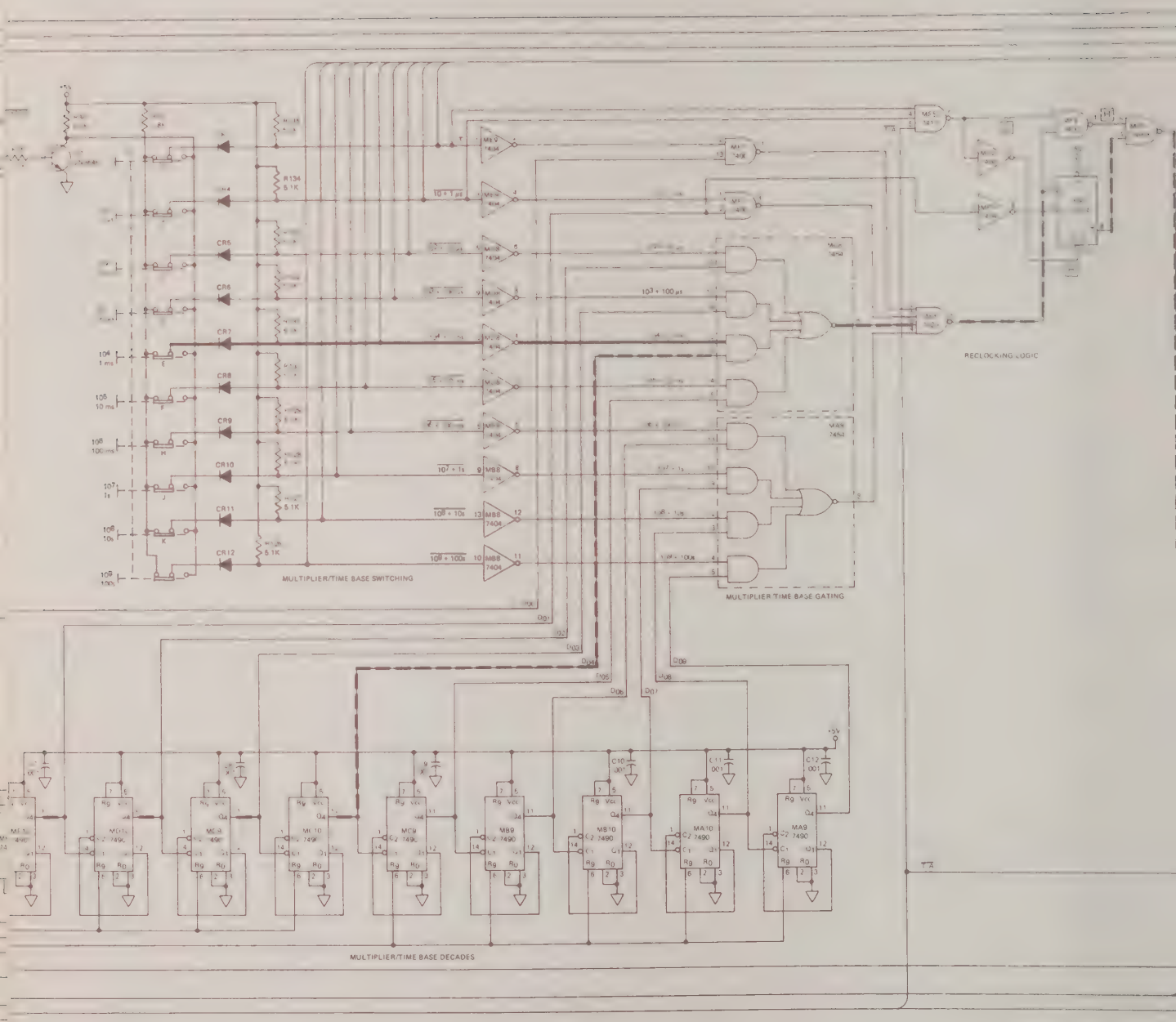


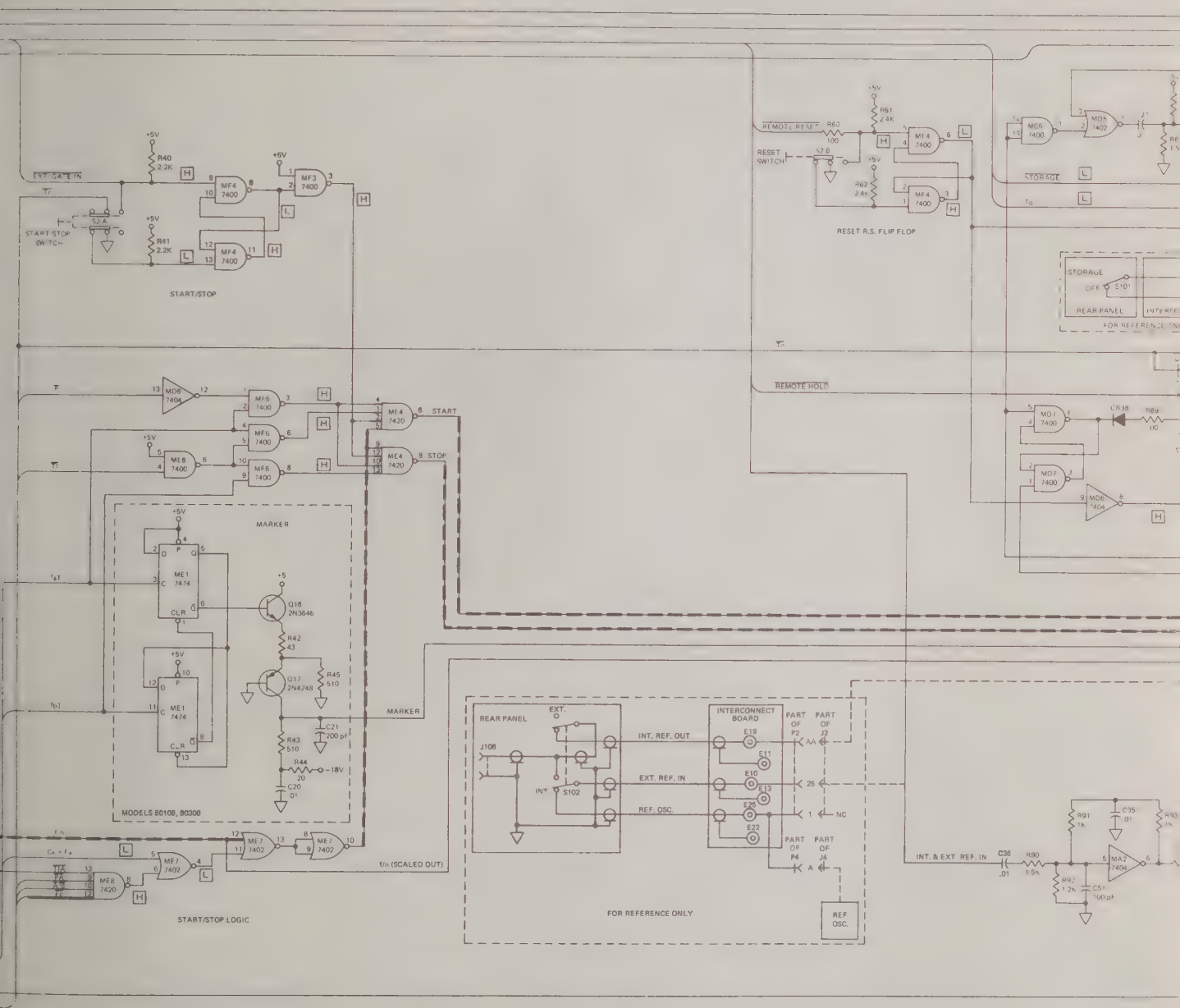
Figure 5.28 - Signal Flow for Frequency A Mode 5-27

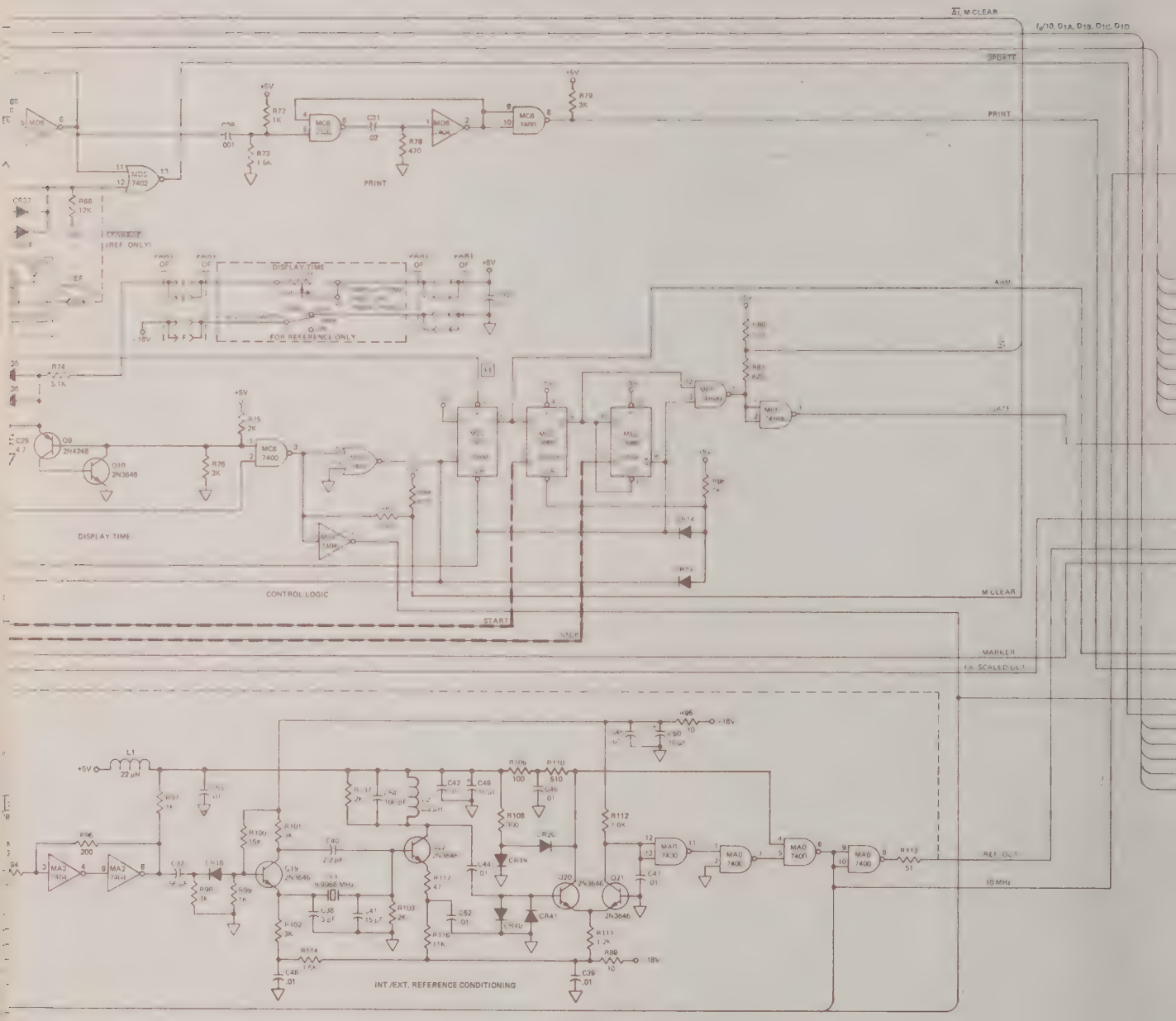

PART OF J2
INT. & EXT. REF. IN
GROUND
EST. RATE A
STORAGE
REMOTE RESET
REMOTE HOLD
10 MHz
COUNTER STEERING LOGIC
MODELS 80108 80308 SYNCHRONIZER
NOTE UNLESS OTHERWISE SPECIFIED
ALL DIODES ARE 018
J2 CONNECTS TO INTERCONNECT BOARD

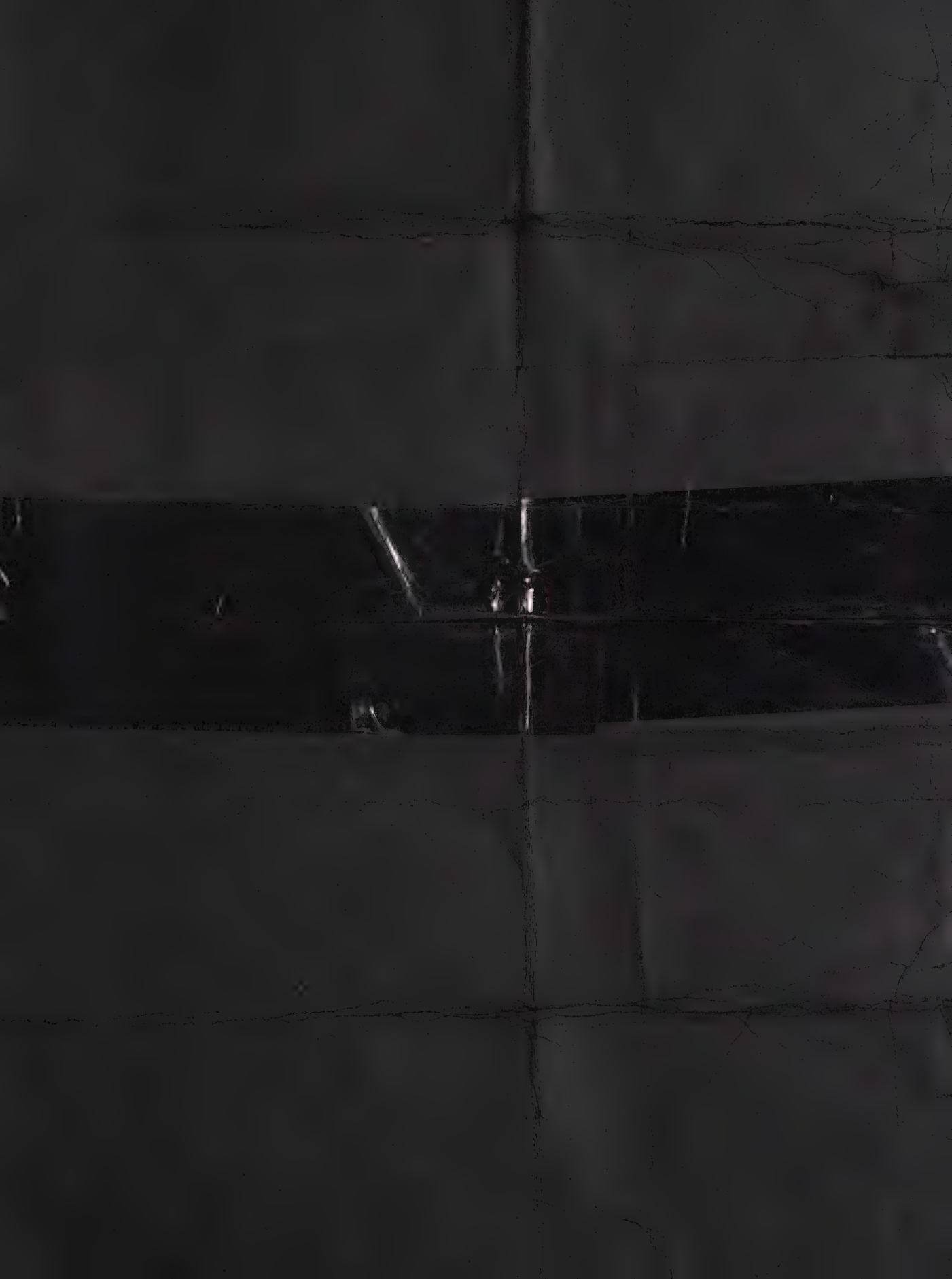

NOTES:
H ECL High 4.2V
L ECL Low 3.6V
H TTL High ≥ 2.0V
L TTL Low ≤.8V
AC
DC
M CLEAR
FAST COUNTING DECADE
TIME BASE STEERING LOGIC
÷ 4
10 MHz
+5V

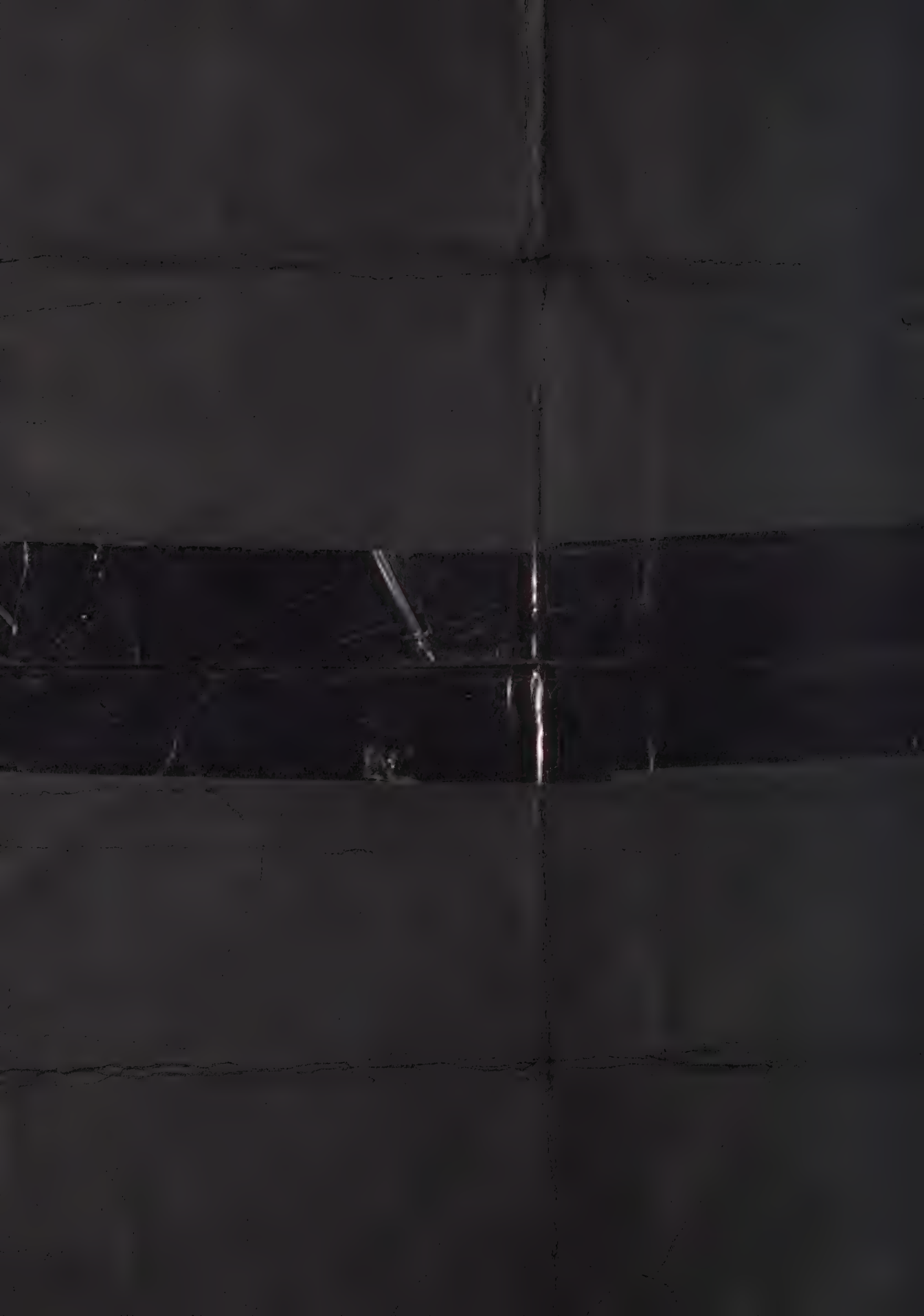


5-28 Figure 5.29 - Signal Flow for Frequency C Mode


START/STOP
START/STOP LOGIC
RESET R.S. FLIP FLOP
MARKER
MODELS 8010B, 8030B
REAR PANEL
INTERCONNECT BOARD
INT. REF. OUT
EXT. REF. IN
REF. OSC.
FOR REFERENCE ONLY
REF OSC.
INT. & EXT. REF. IN
f/n (SCALED OUT)
REMOTE RESET
REMOTE HOLD
STORAGE
START
STOP
MARKER


ΔT MCLEAR
f0/10, D1A, D1B, D1C, D1D
UPDATE
PRINT
+5V
R79 3K
R72 1K
R73 1.6K
C38 .001
C21 .02
R78 470
MC8 7400
MD6 7402
R68 12K
CURRENT (REF ONLY)
DISPLAY TIME
FOR REFERENCE ONLY
-18V
R74 5.1K
R75 2K
R76 3K
Q9 2N4248
Q10 2N3646
CONTROL LOGIC
START
STOP
MCLEAR
MARKER
fo SCALED OUT
L1 22 µH
+9V
-18V
R96 200
R97 1K
R98 1K
R99 1K
R100 15K
R101 1K
R102 3K
R103 2K
R104 100
R105 510
R106 100
R107 2K
R108 100
R109 6K
R110 6K
R111 1.2K
R112 6K
R113 51
R114 1.2K
R116 11K
R117 47
C40 2.2 pF
C41 15 pF
C42 .01
C44 .01
C46 .01
C47 .01
C48 .01
C49 .01
C50 10
C52 .01
C39 .01
L58 5 pF
Y1 4.9968 MHz
CR18
CR19
CR40
CR41
Q19 2N1646
Q20 2N3646
Q21 2N3646
MA0 7430
MA0 7404
MA0 7400
MA2 7404
REF OUT
10 MHz
INT /EXT. REFERENCE CONDITIONING





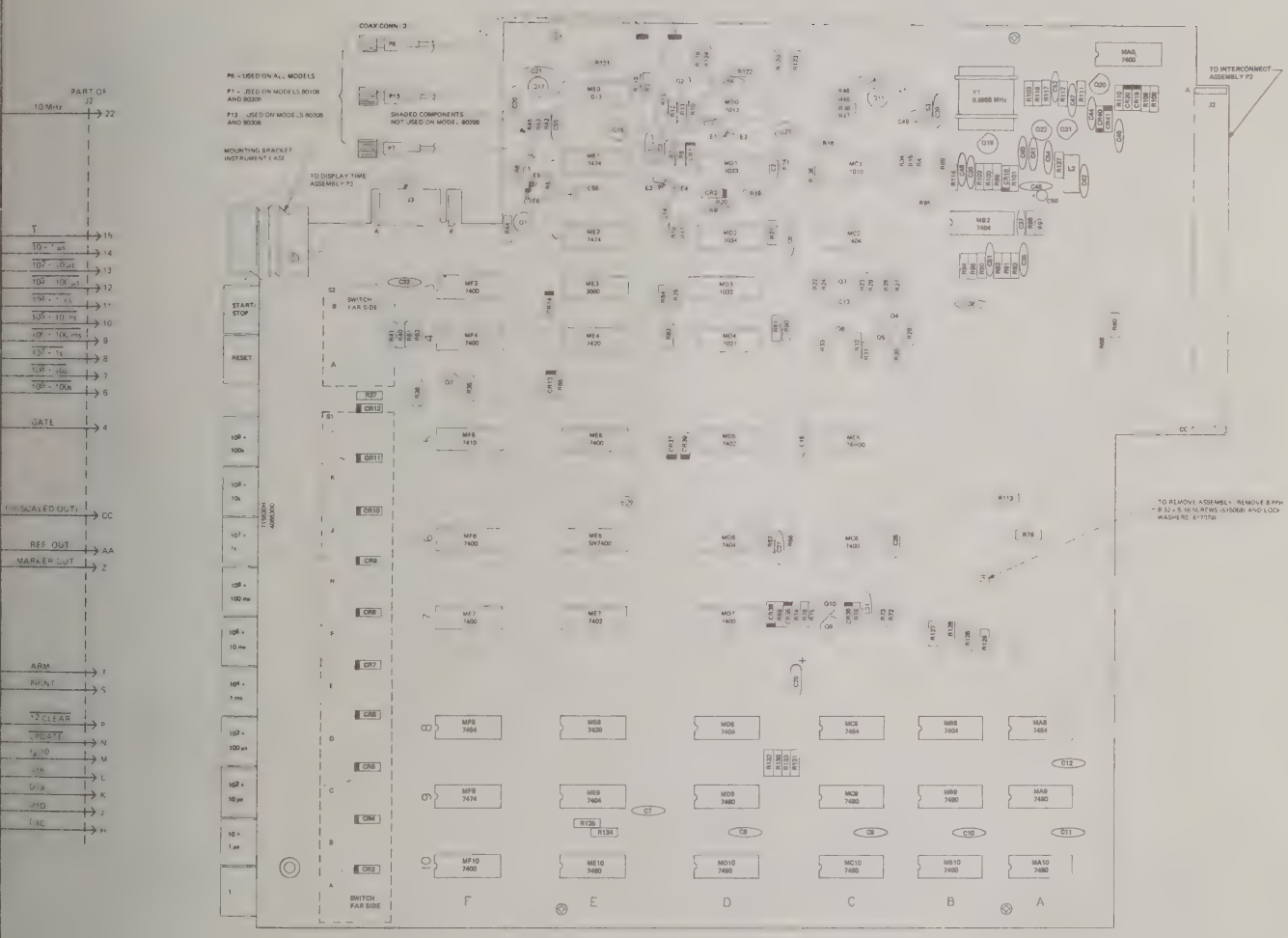
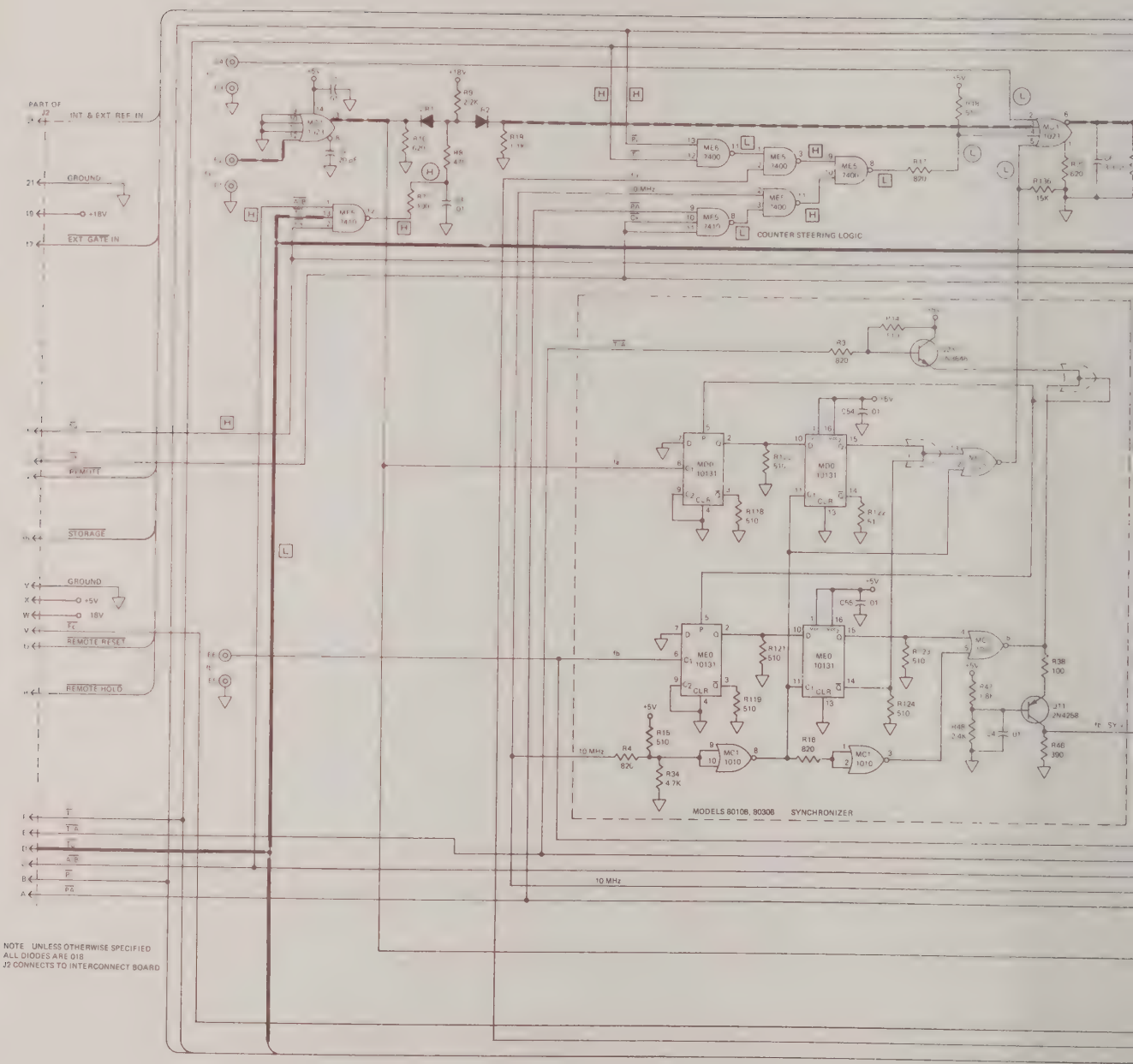
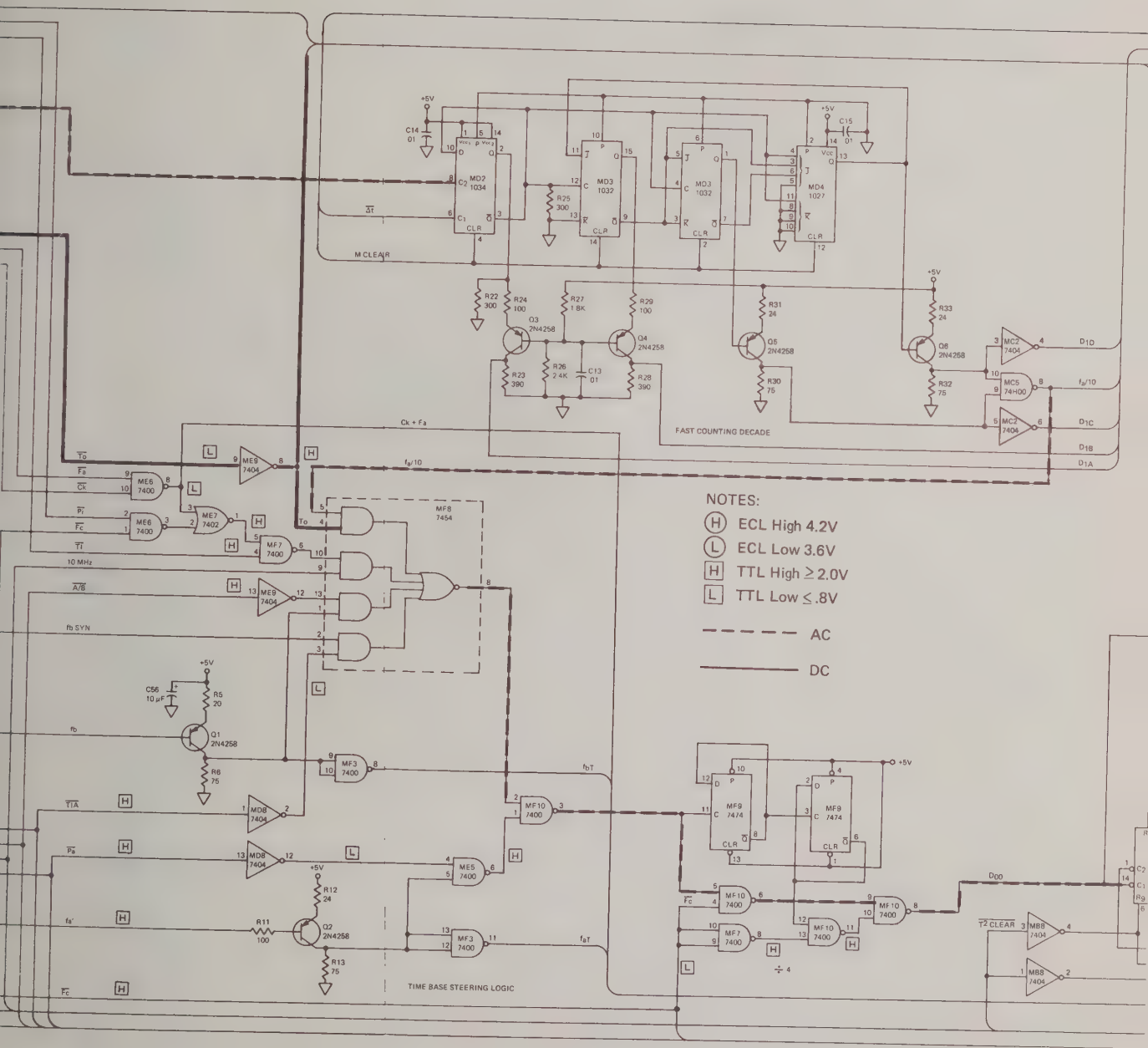
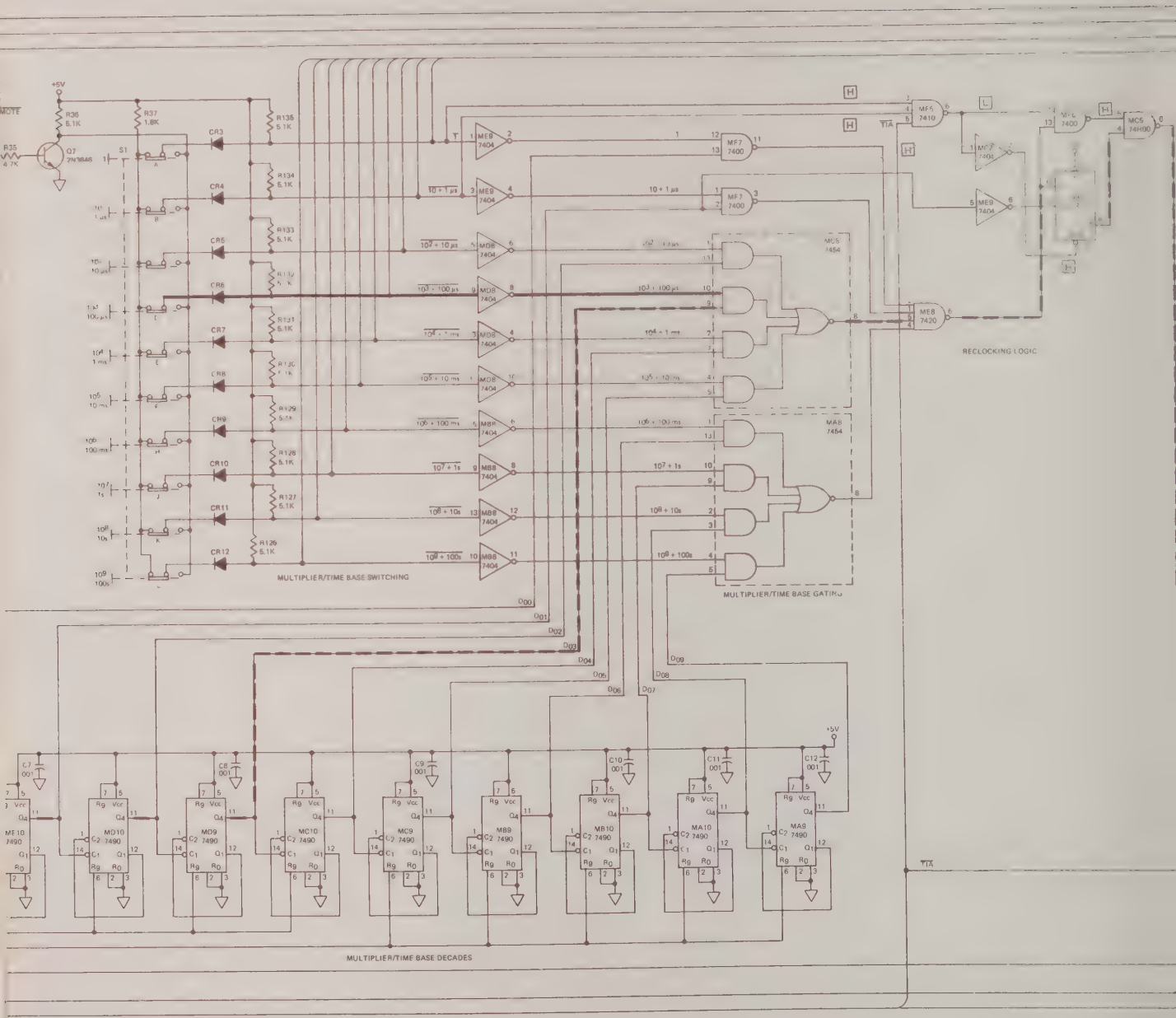


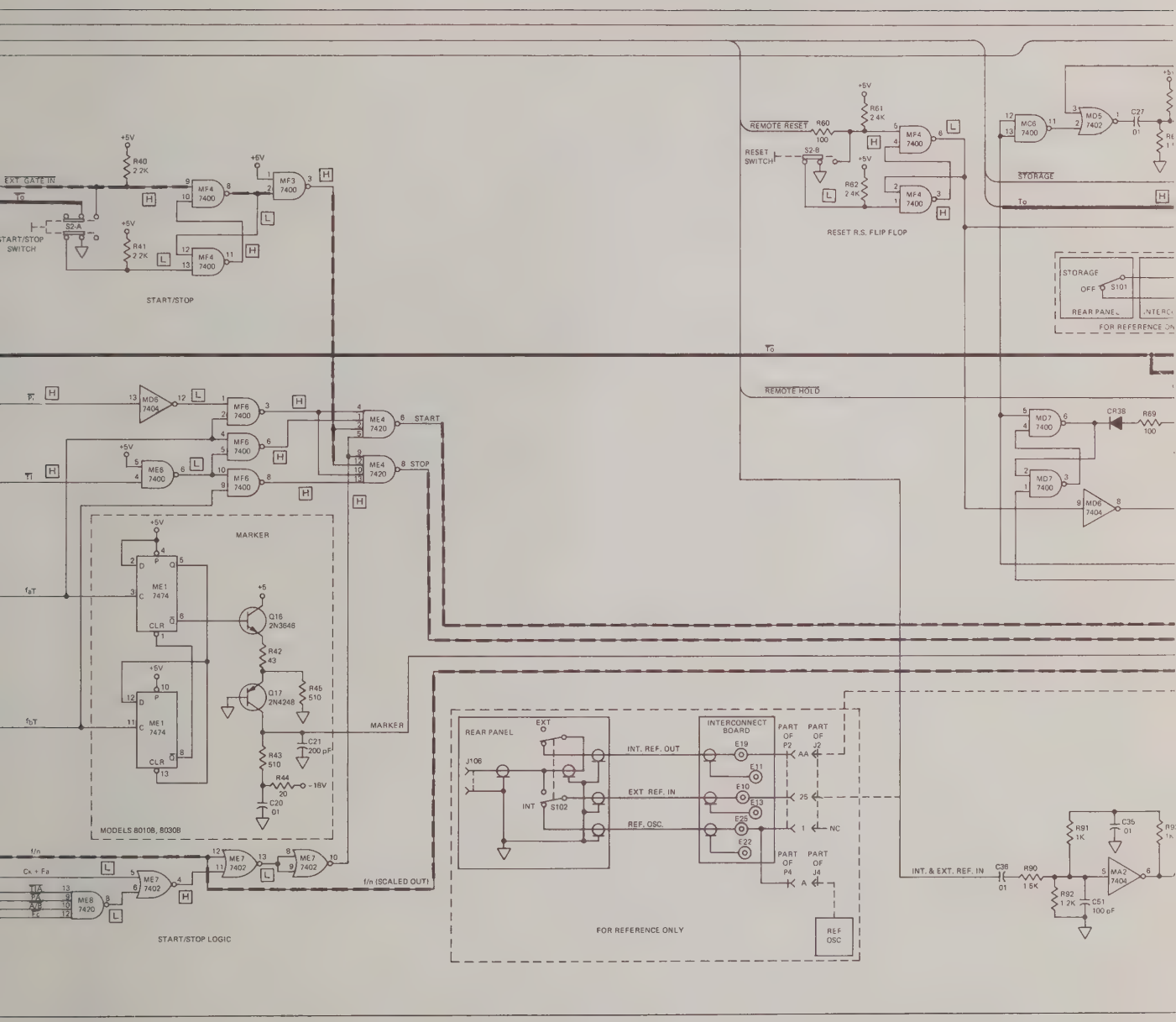
Figure 5.29 - Signal Flow for Frequency C Mode 5-29

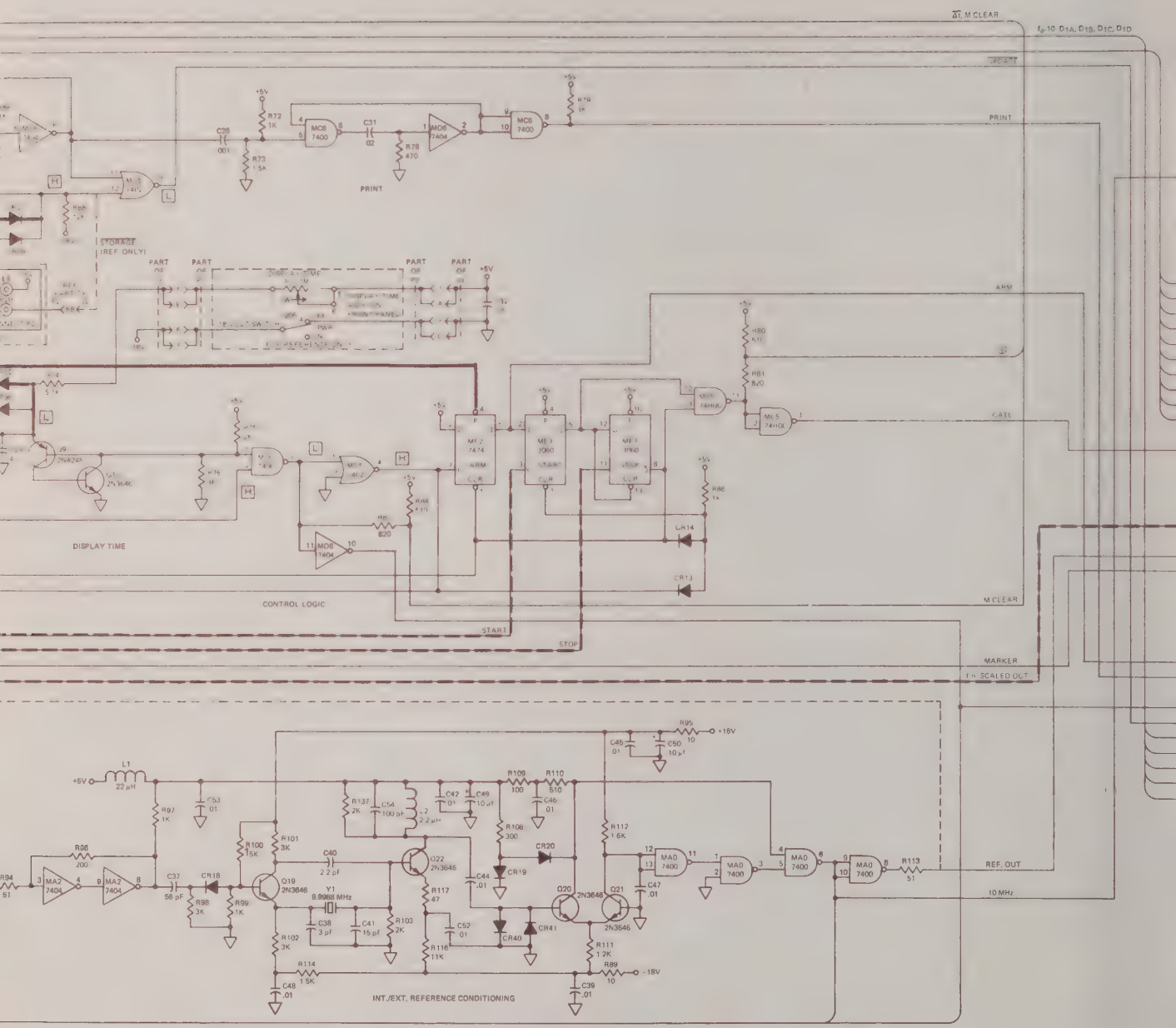

PART OF J2
INT & EXT REF IN
GROUND
+18V
EXT GATE IN
PERMIT
STORAGE
GROUND
+5V
18V
REMOTE RESET
REMOTE HOLD
10 MHz
COUNTER STEERING LOGIC
MODELS 80108, 80308 SYNCHRONIZER
NOTE: UNLESS OTHERWISE SPECIFIED
ALL DIODES ARE 018
J2 CONNECTS TO INTERCONNECT BOARD

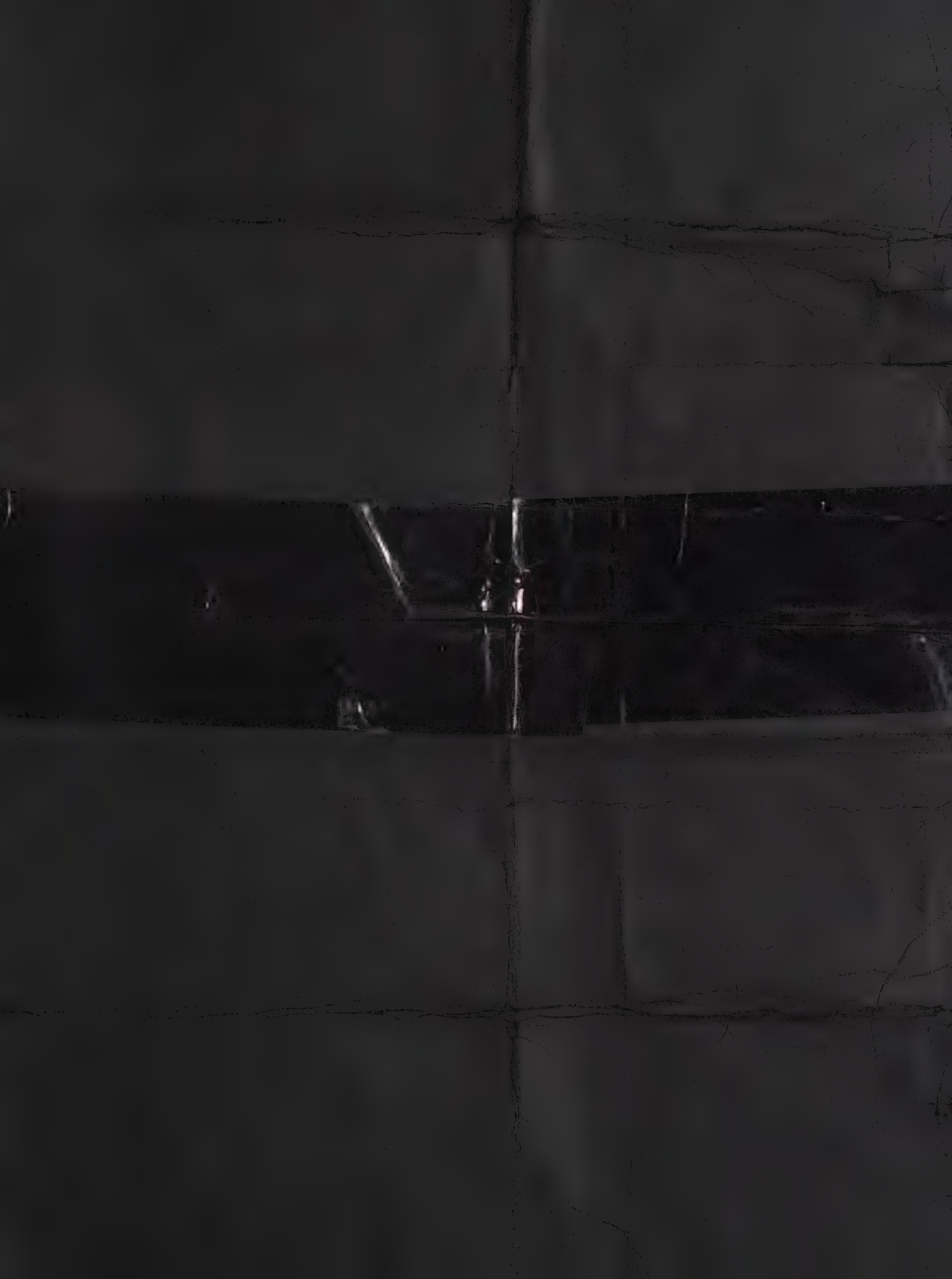

NOTES:
H ECL High 4.2V
L ECL Low 3.6V
H TTL High ≥ 2.0V
L TTL Low ≤ .8V
AC
DC
M CLEAR
FAST COUNTING DECADE
TIME BASE STEERING LOGIC
÷ 4
Ck + Fa
fb SYN
10 MHz
+5V

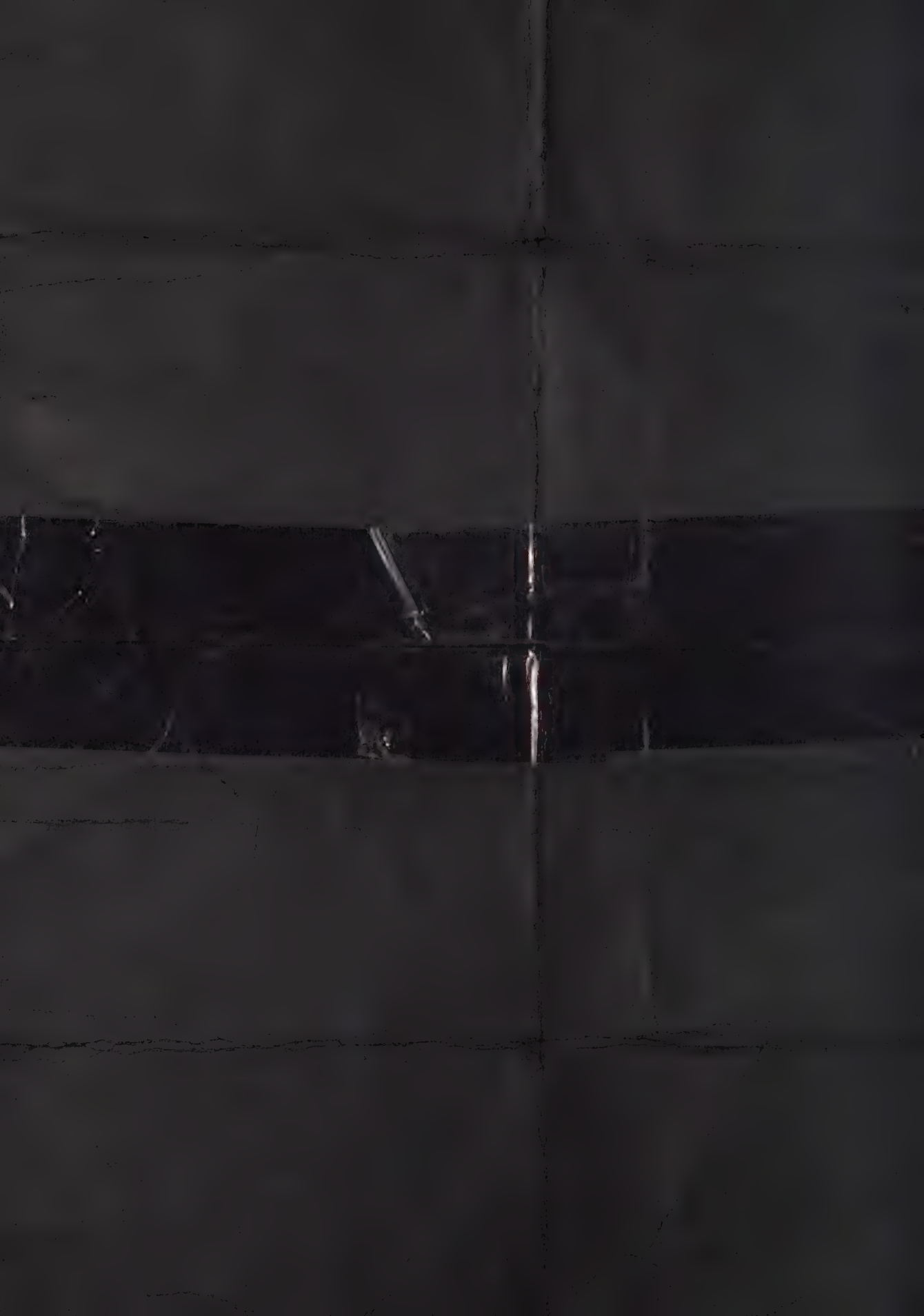


5-30 Figure 5.30 - Signal Flow for Totalize Mode


EXT. GATE IN
START/STOP SWITCH
START/STOP
RESET SWITCH
REMOTE RESET
RESET R.S. FLIP FLOP
STORAGE
REMOTE HOLD
START
STOP
MARKER
MODELS 8010B, 8030B
START/STOP LOGIC
f/n (SCALED OUT)
REAR PANEL
INTERCONNECT BOARD
INT. REF. OUT
EXT. REF. IN
REF. OSC.
FOR REFERENCE ONLY
REF OSC
INT. & EXT. REF. IN


PRINT
STORAGE (REF ONLY)
DISPLAY TIME
CONTROL LOGIC
START
STOP
ARM
GATE
M CLEAR
MARKER
SCALED OUT
REF. OUT
10 MHz
INT./EXT. REFERENCE CONDITIONING





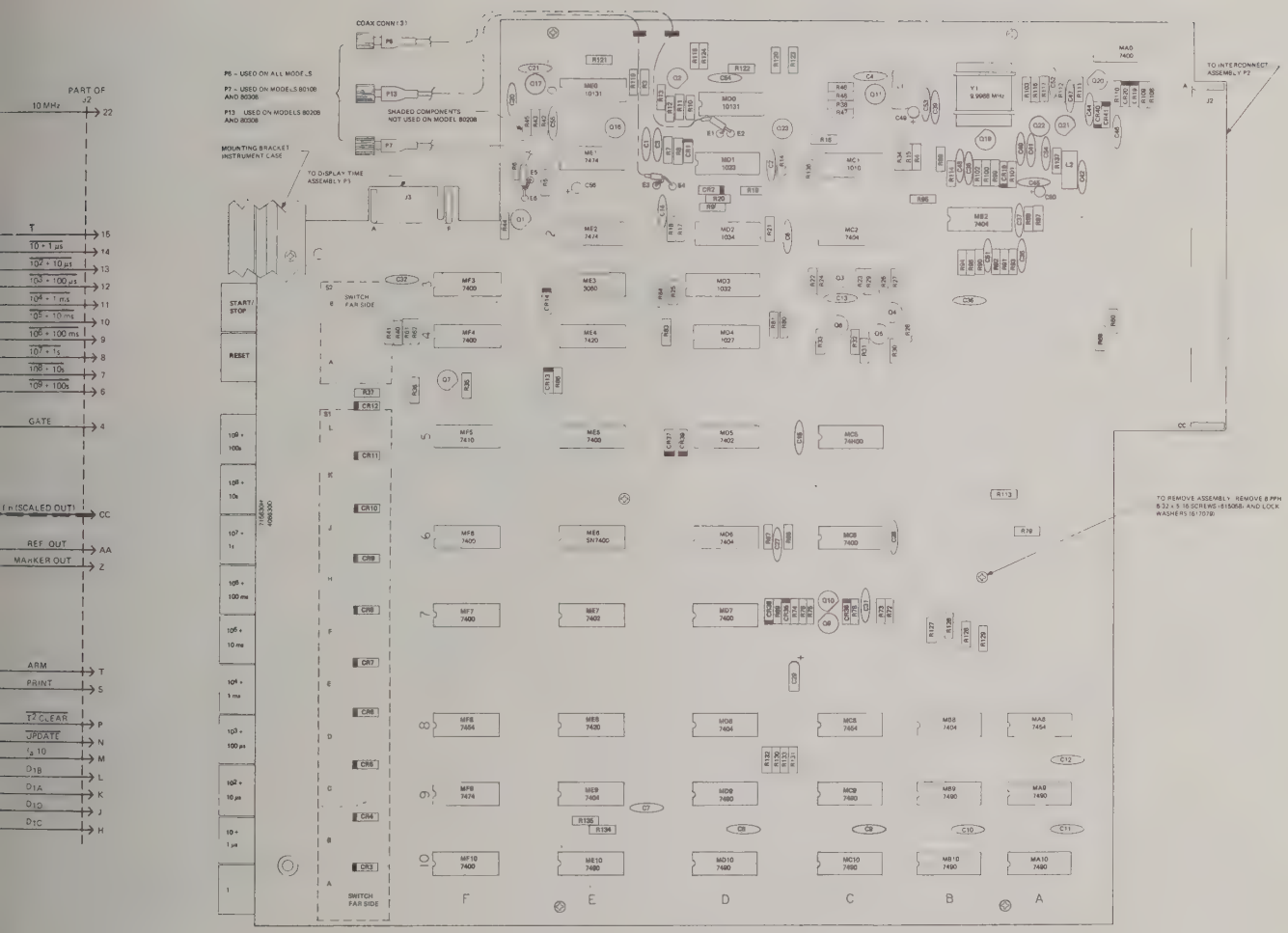
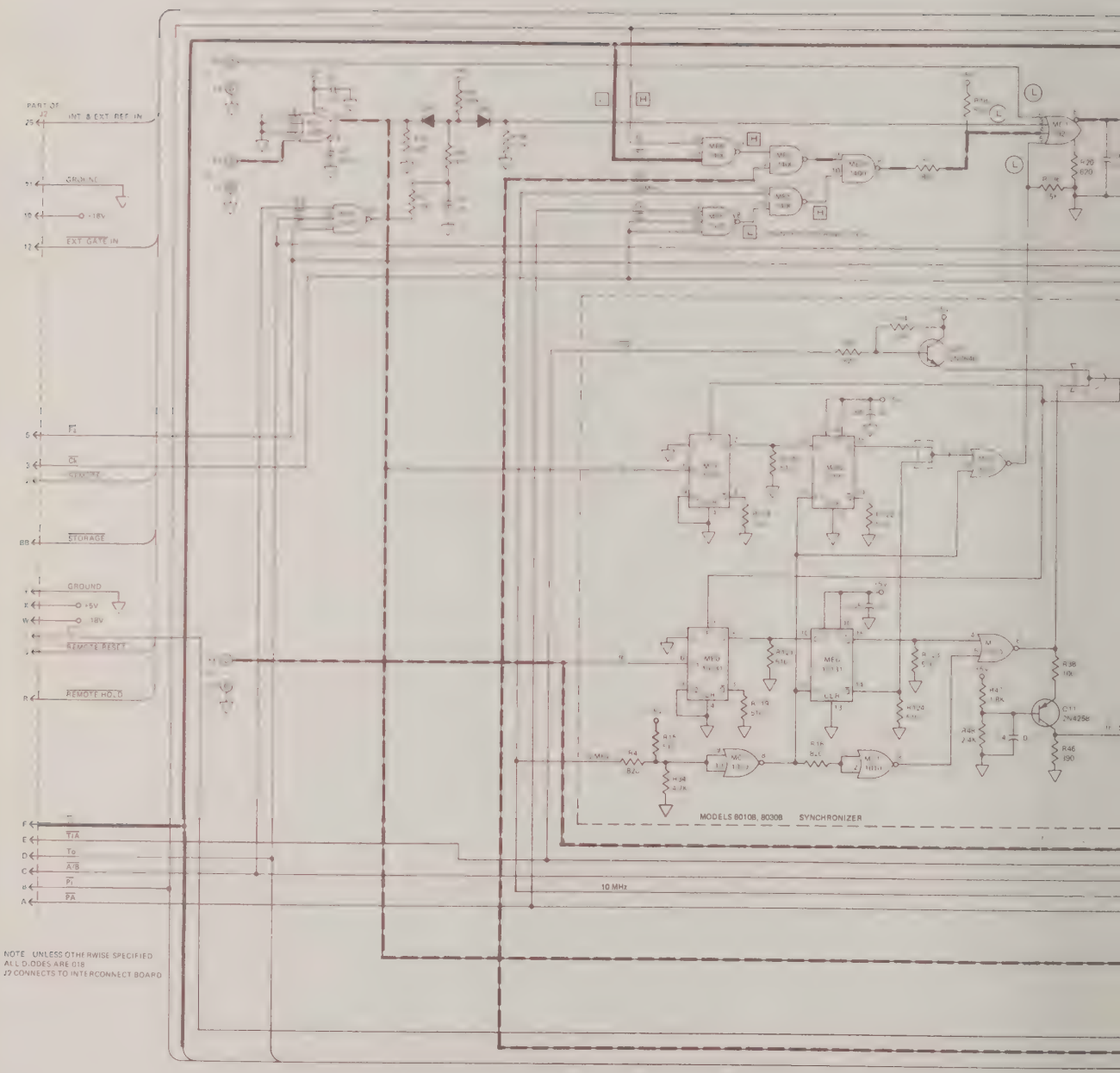
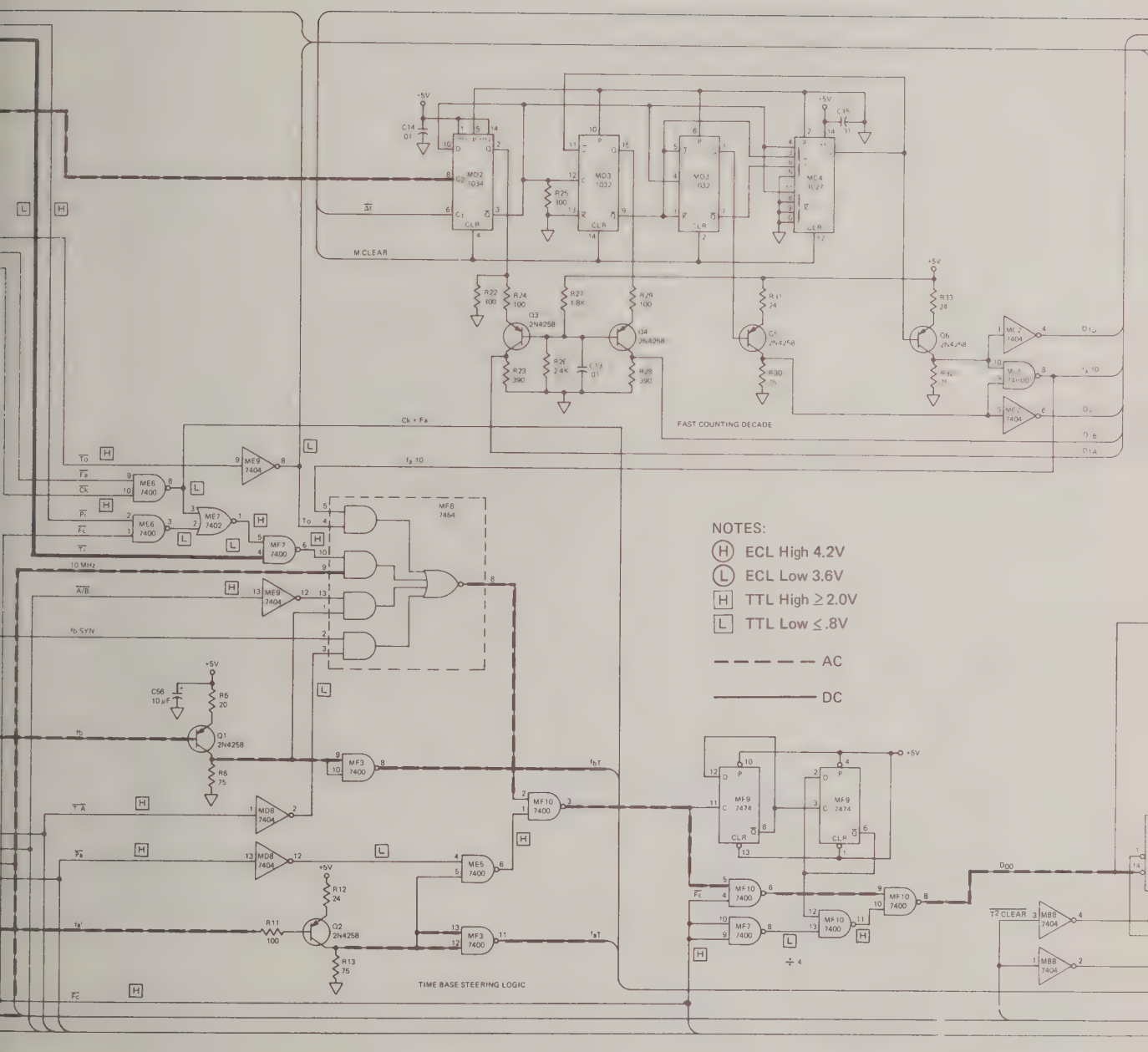
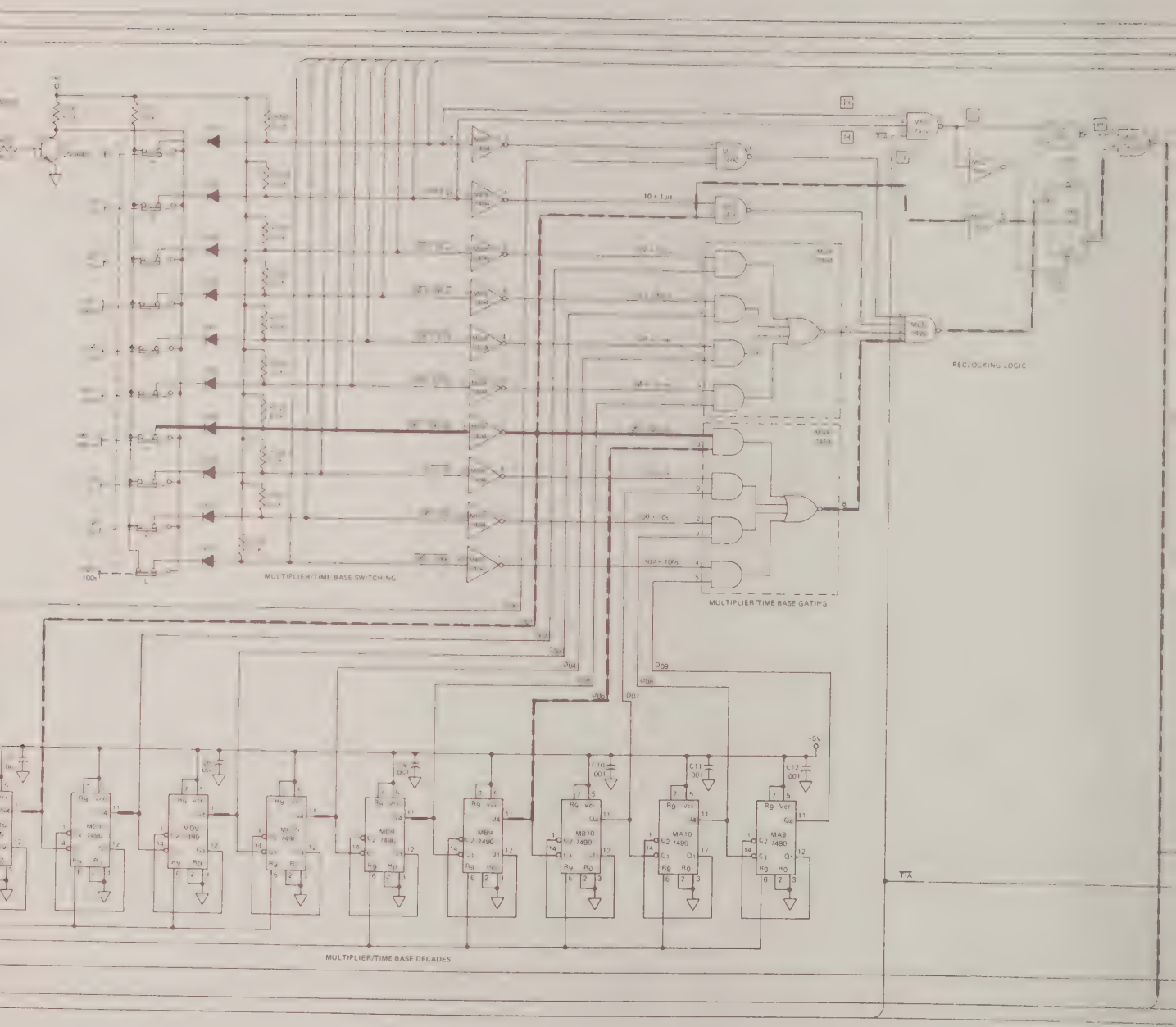


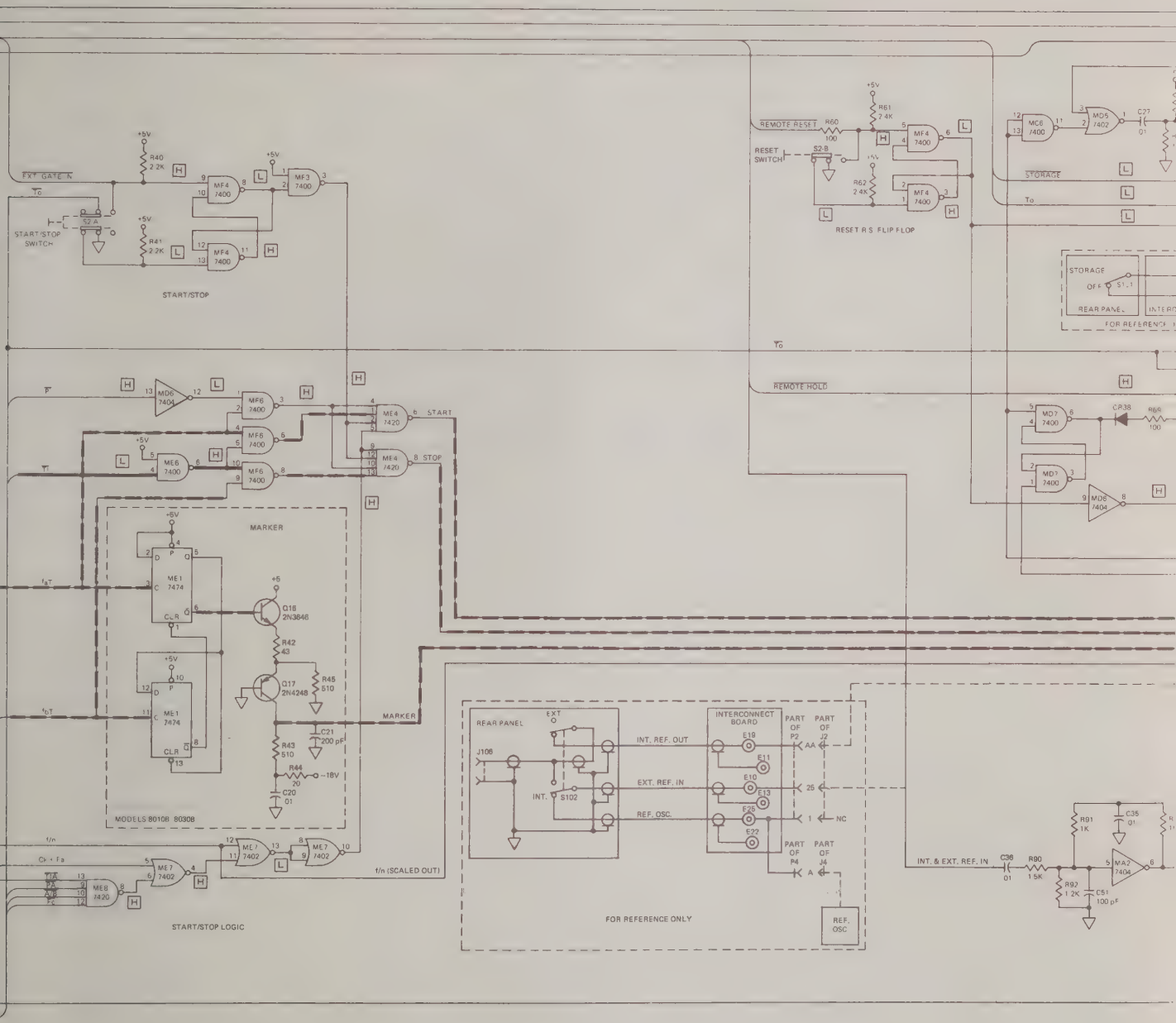
Figure 5.30 - Signal Flow for Totalize Mode 5-31

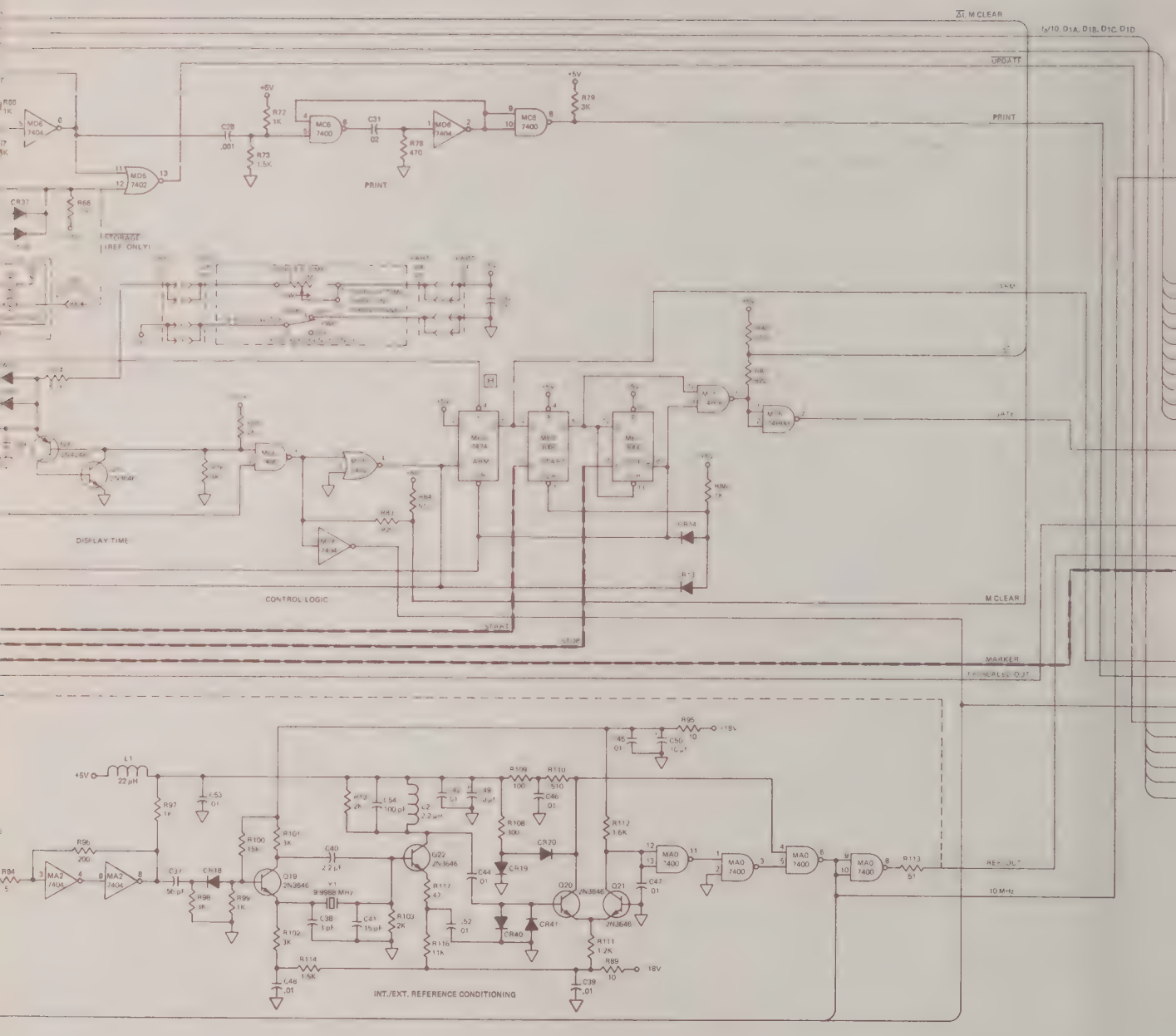

PART OF J2
25 INT. & EXT. REF. IN
11 GROUND
10 +18V
12 EXT. GATE IN
5
3
4
BB STORAGE
T GROUND
Z +5V
W 18V
REMOTE RESET
R REMOTE HOLD
F
E
D
C
B
A
NOTE UNLESS OTHERWISE SPECIFIED
ALL DIODES ARE 018
J2 CONNECTS TO INTERCONNECT BOARD
MODELS 80108, 80308 SYNCHRONIZER
10 MHz

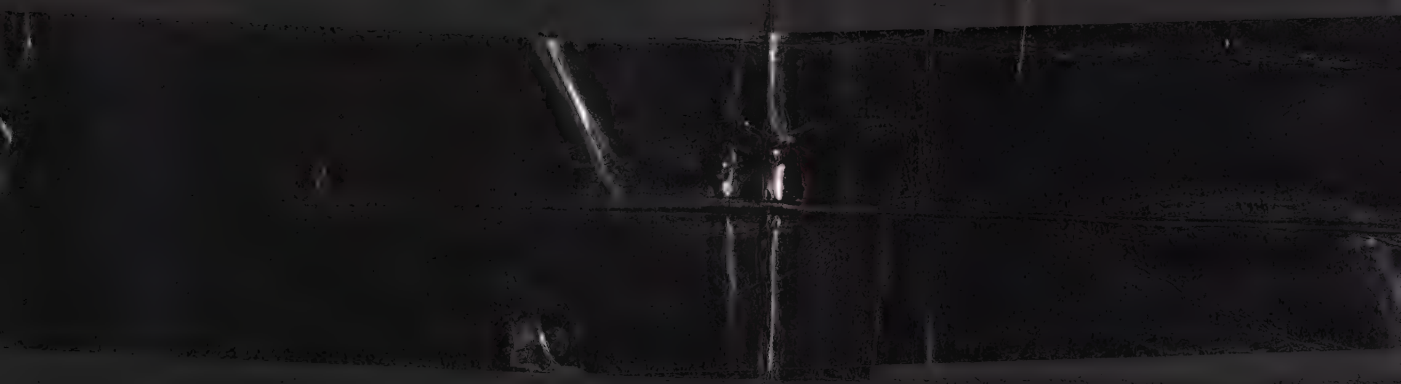

NOTES:
H ECL High 4.2V
L ECL Low 3.6V
H TTL High ≥ 2.0V
L TTL Low ≤ .8V
AC
DC
M CLEAR
FAST COUNTING DECADE
TIME BASE STEERING LOGIC
÷ 4
10 MHz
+5V

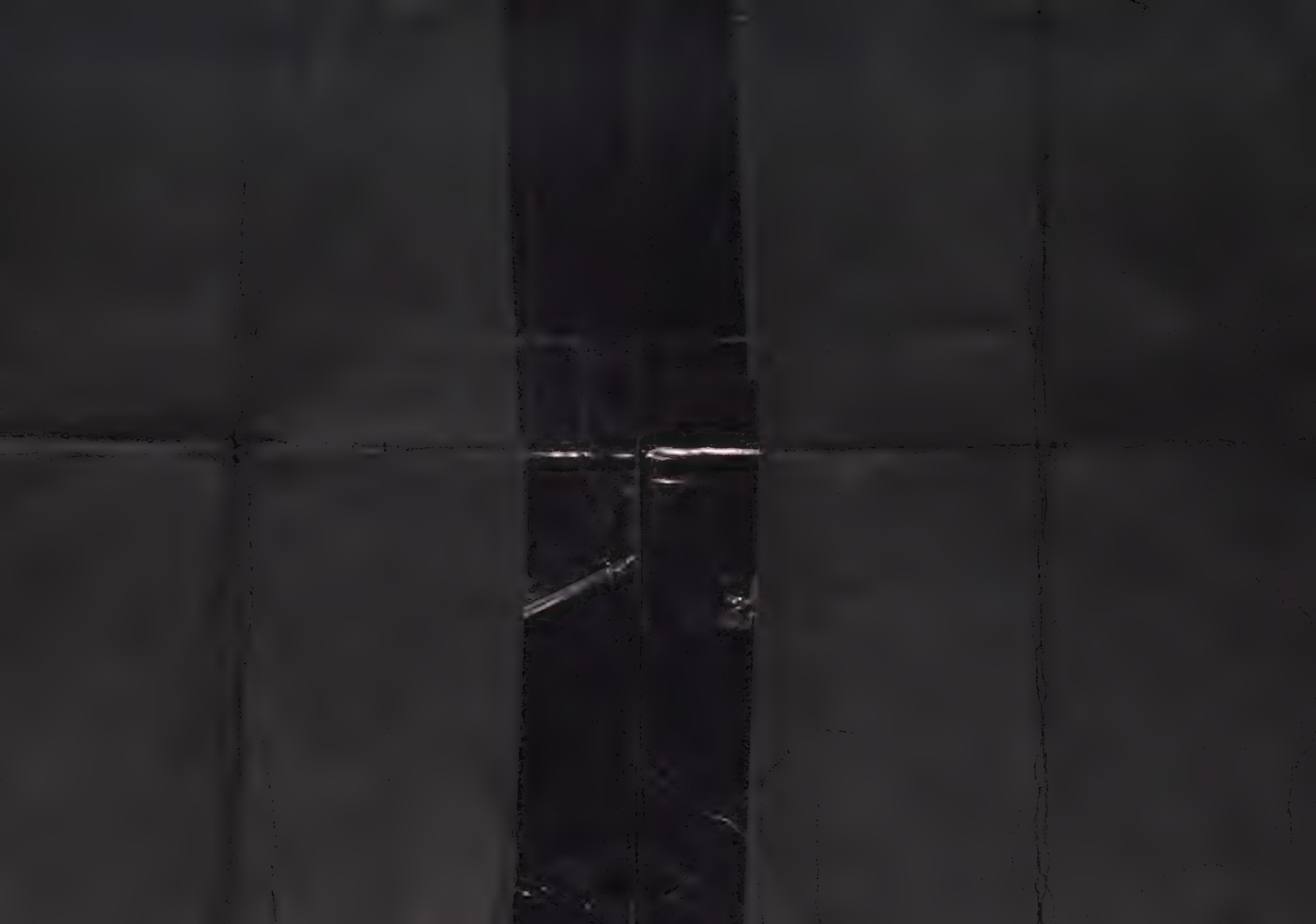


5-32 Figure 5.31 - Signal Flow for Time Interval Mode


START/STOP
START/STOP LOGIC
RESET R S FLIP FLOP
MARKER
MODELS 8010B 8030B
f/n (SCALED OUT)
REMOTE HOLD
REMOTE RESET
RESET SWITCH
START/STOP SWITCH
EXT GATE IN
STORAGE
REAR PANEL
INTERCONNECT BOARD
INT. REF. OUT
EXT. REF. IN
REF. OSC.
INT. & EXT. REF. IN
FOR REFERENCE ONLY
START
STOP
MARKER
f/n (SCALED OUT)


M CLEAR
UPDATE
PRINT
STORAGE (REF ONLY)
DISPLAY TIME
CONTROL LOGIC
MARKER
10 MHz
INT./EXT. REFERENCE CONDITIONING





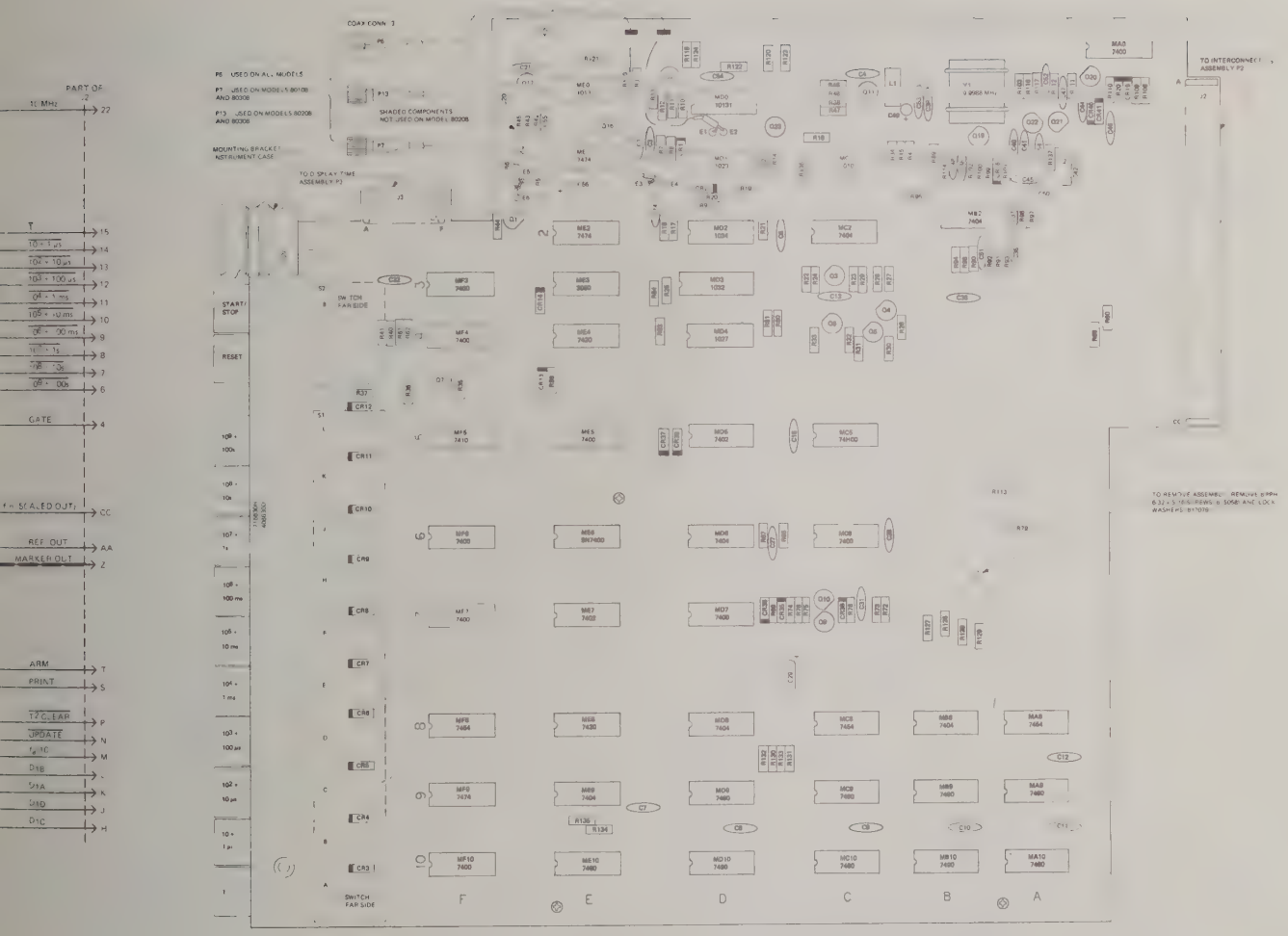
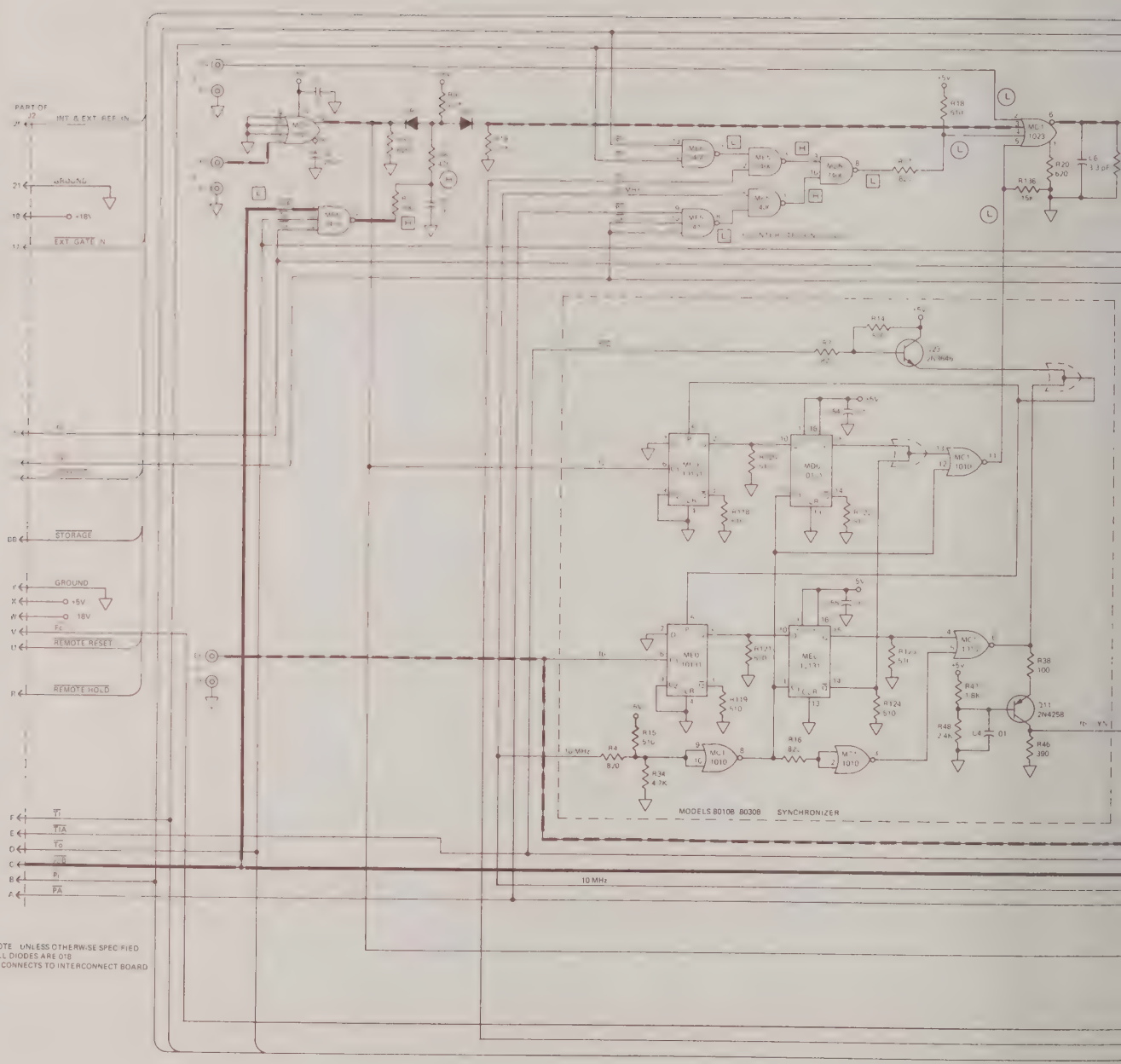
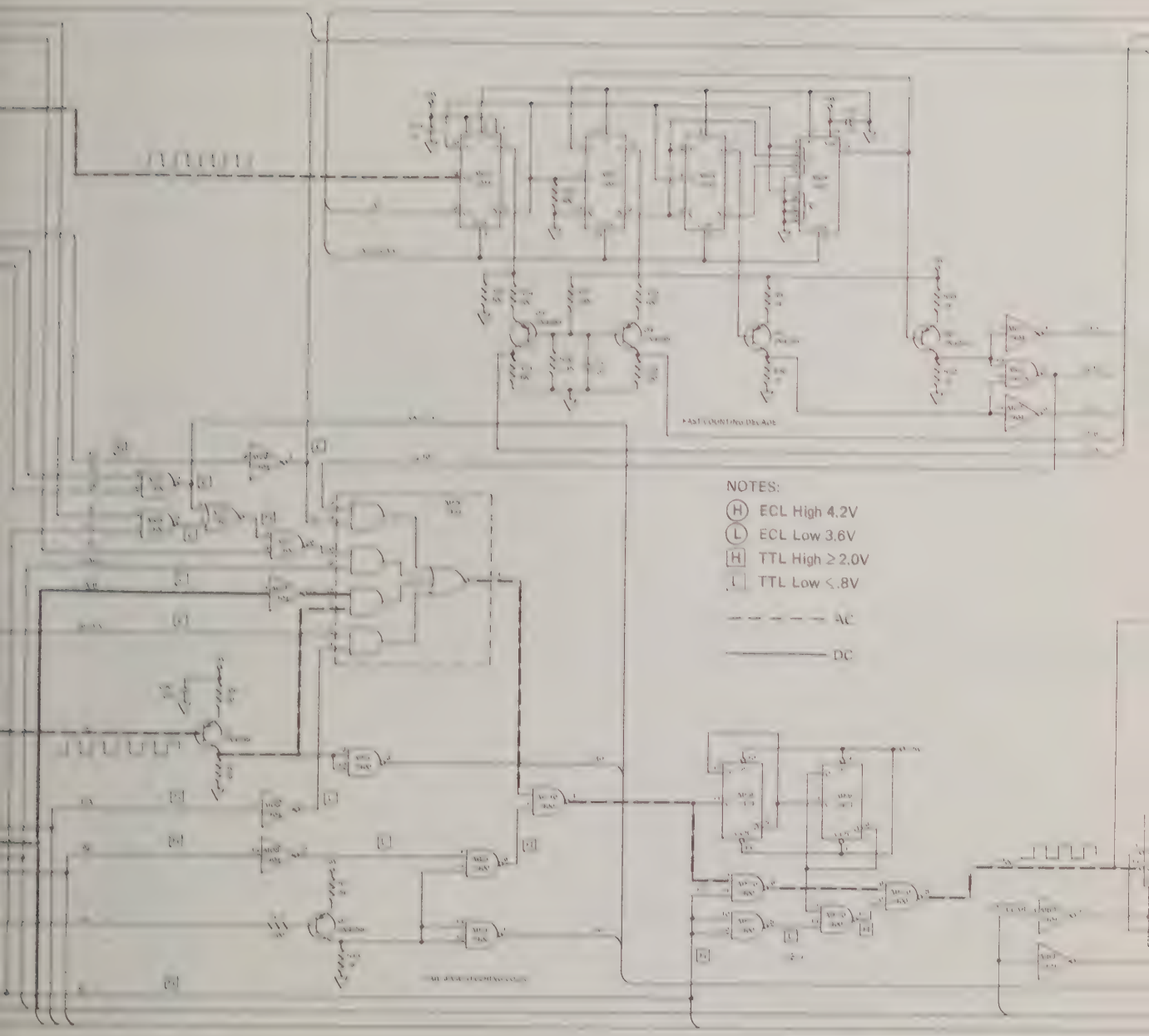
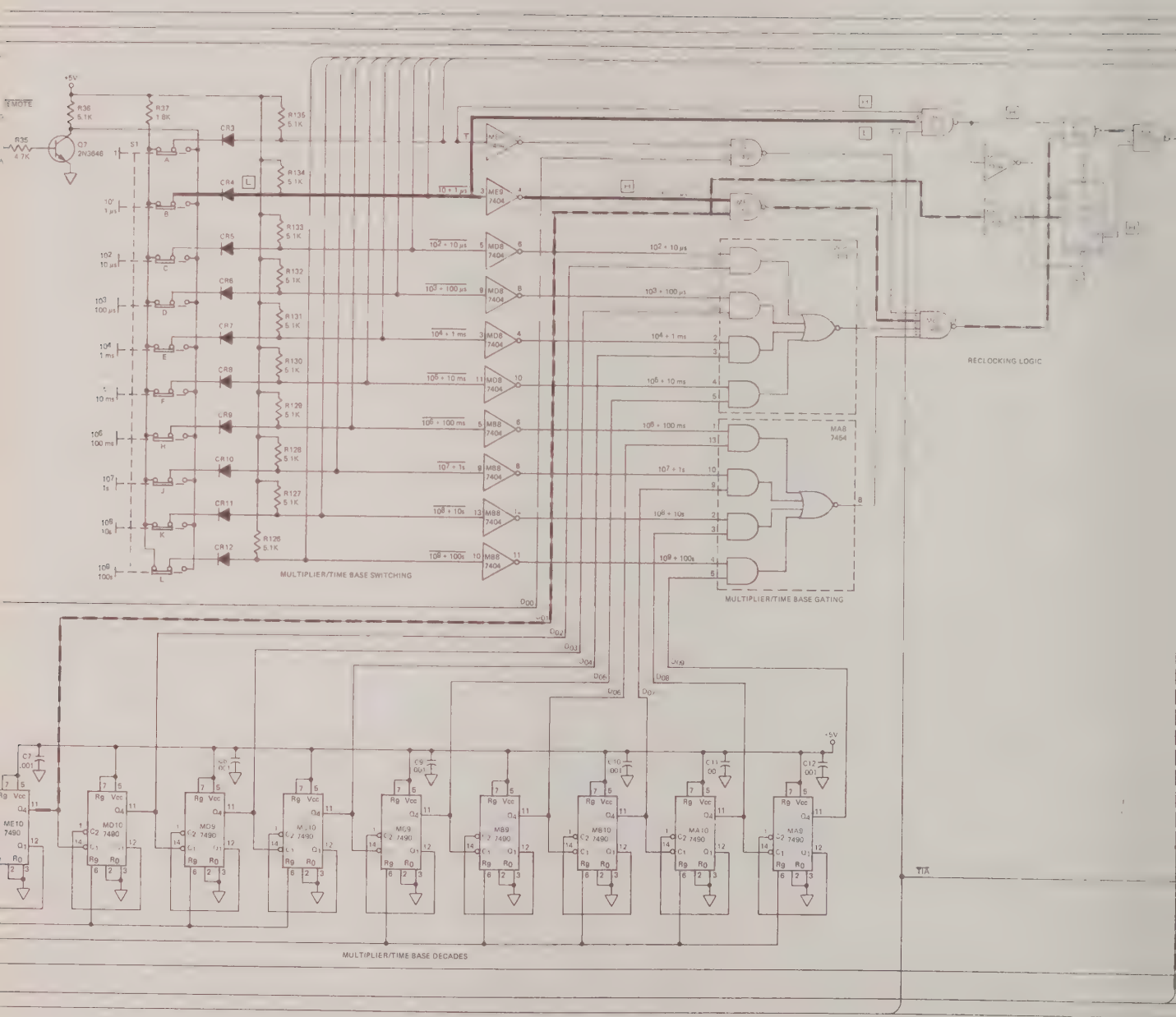


Figure 5.31 - Signal Flow for Time Interval Mode

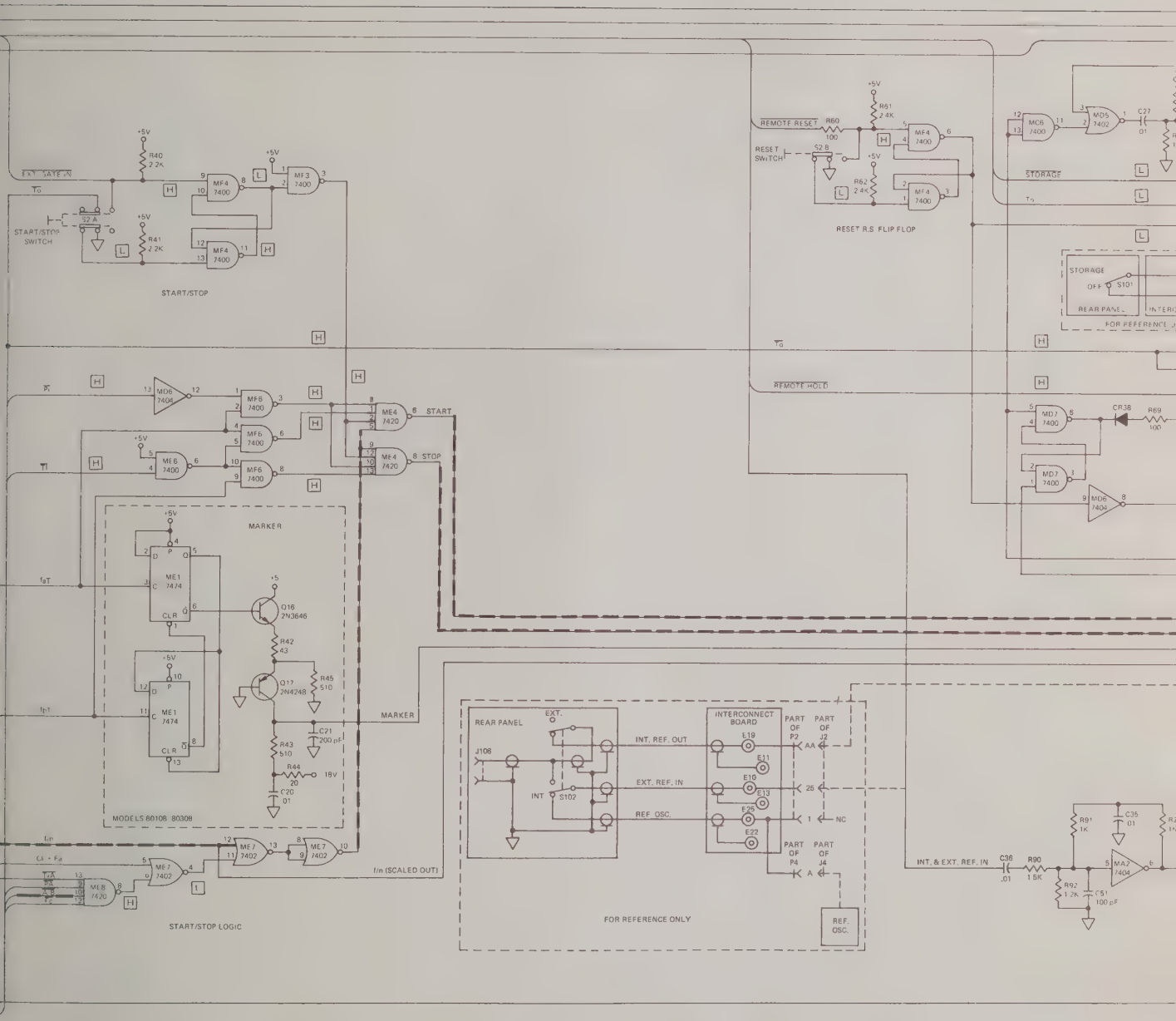


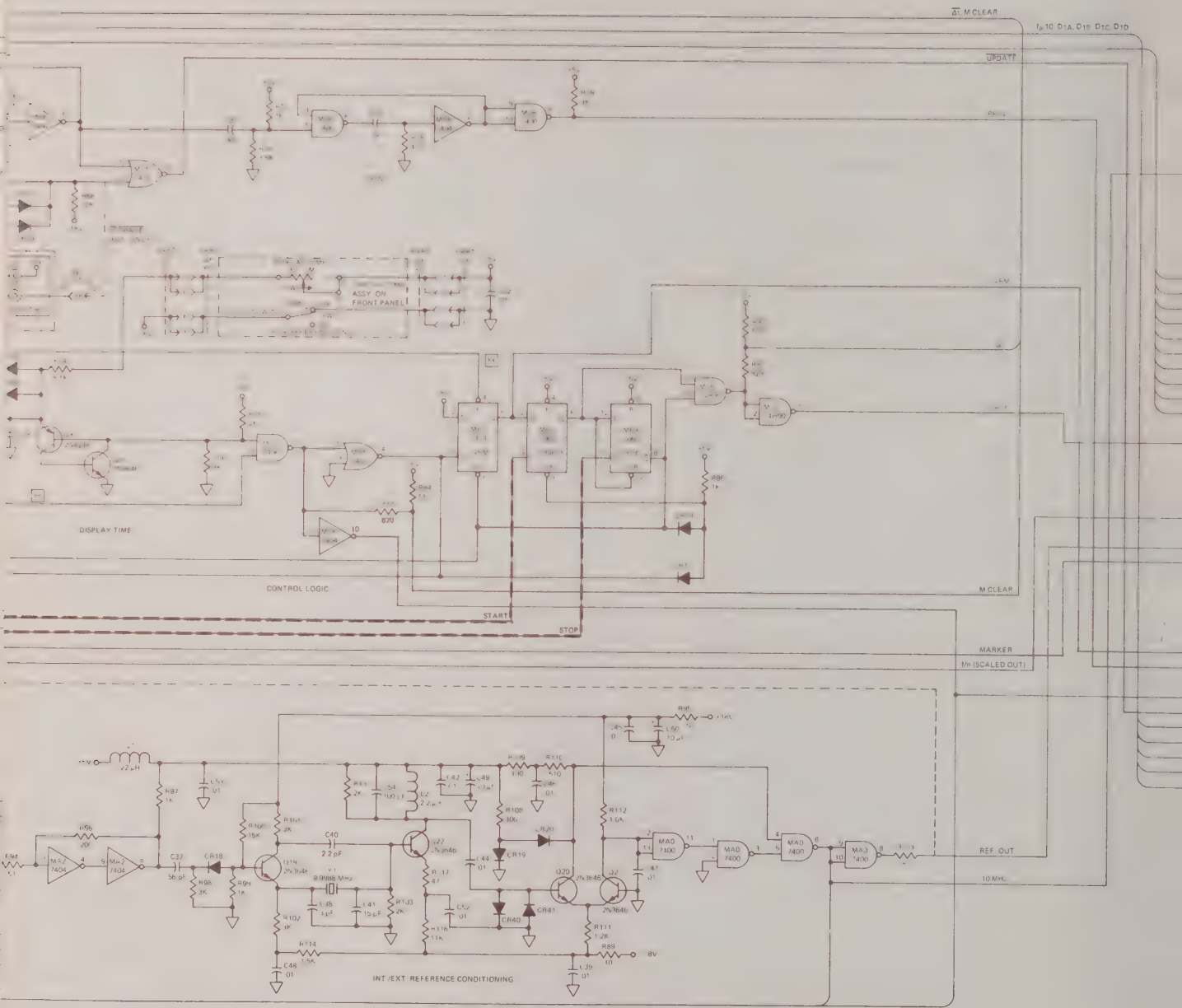
NOTE UNLESS OTHERWISE SPECIFIED
ALL DIODES ARE 018
J2 CONNECTS TO INTERCONNECT BOARD

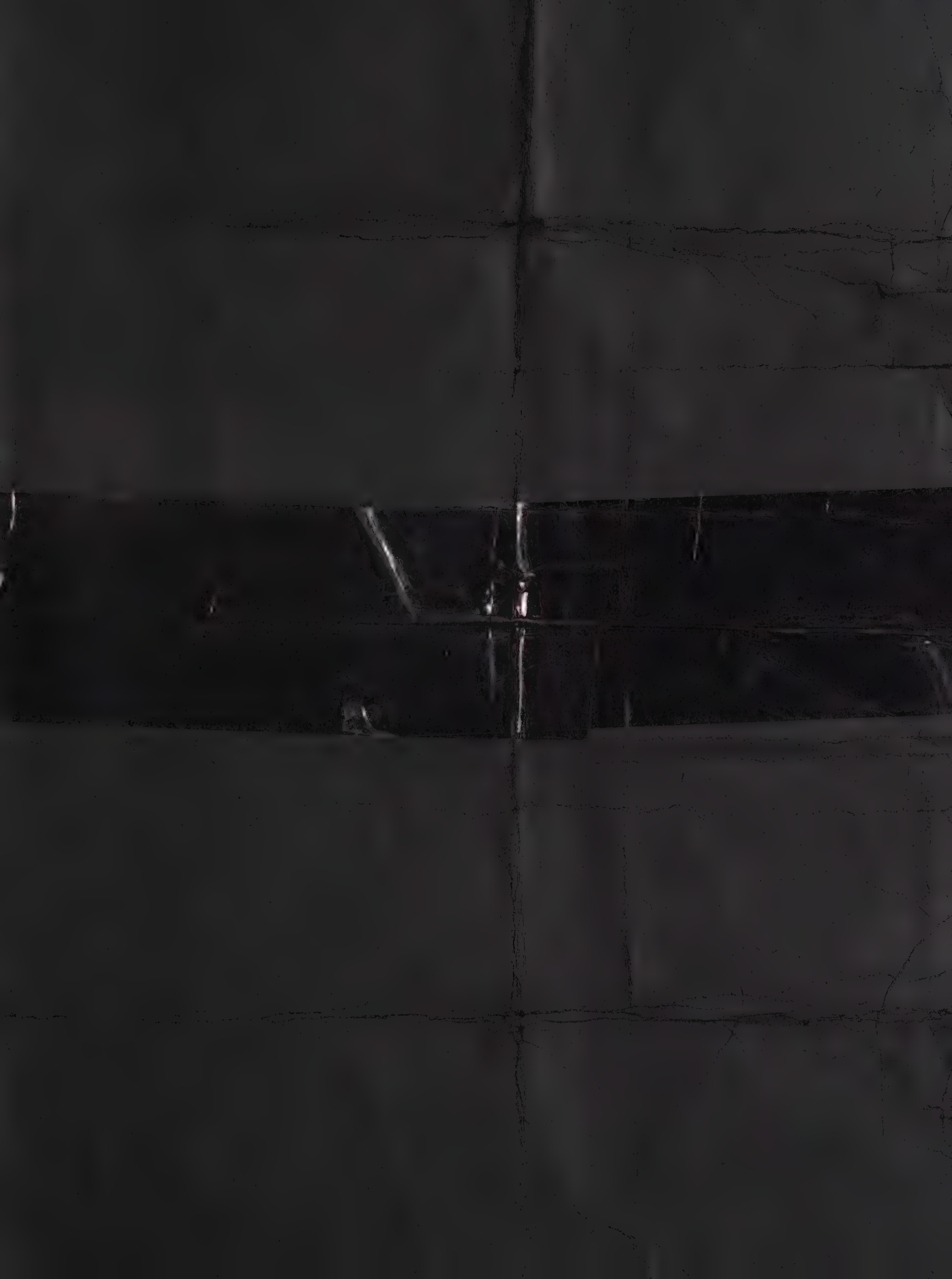

NOTES:
H ECL High 4.2V
L ECL Low 3.6V
H TTL High ≥ 2.0V
L TTL Low ≤ .8V
AC
DC

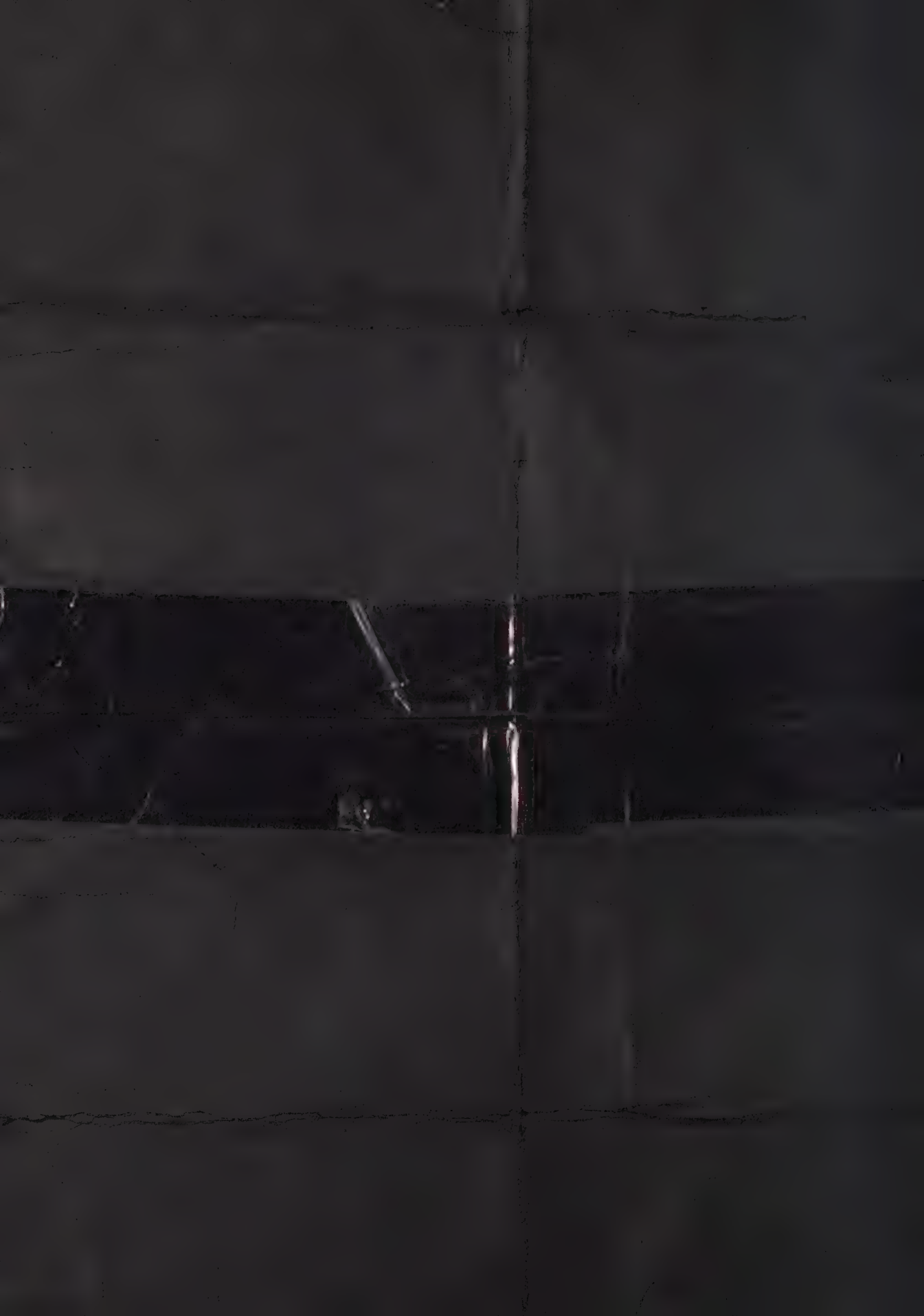


5-34 Figure 5.32 - Signal Flow for A/B Ratio Mode


START/STOP
START/STOP LOGIC
RESET R.S. FLIP FLOP
MARKER
MODELS 80108, 80308
FOR REFERENCE ONLY
REAR PANEL
INTERCONNECT BOARD
INT. REF. OUT
EXT. REF. IN
REF. OSC.
INT. & EXT. REF. IN
REMOTE RESET
REMOTE HOLD
STORAGE
START
STOP
MARKER
1/n (SCALED OUT)


M CLEAR
UPDATE
ASSY ON FRONT PANEL
DISPLAY TIME
CONTROL LOGIC
START
STOP
M CLEAR
MARKER
f/n (SCALED OUT)
REF OUT
10 MHz
INT /EXT REFERENCE CONDITIONING





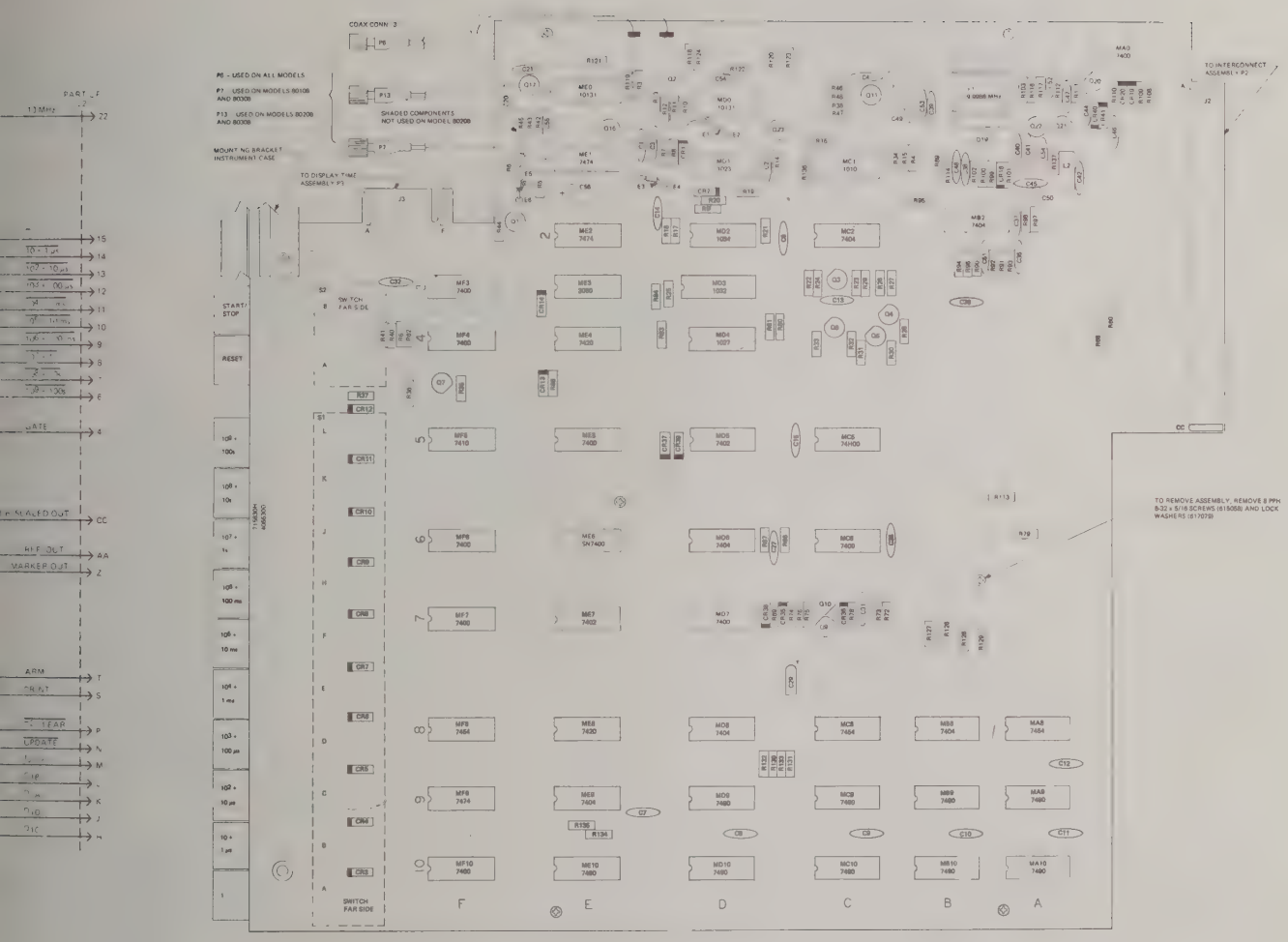
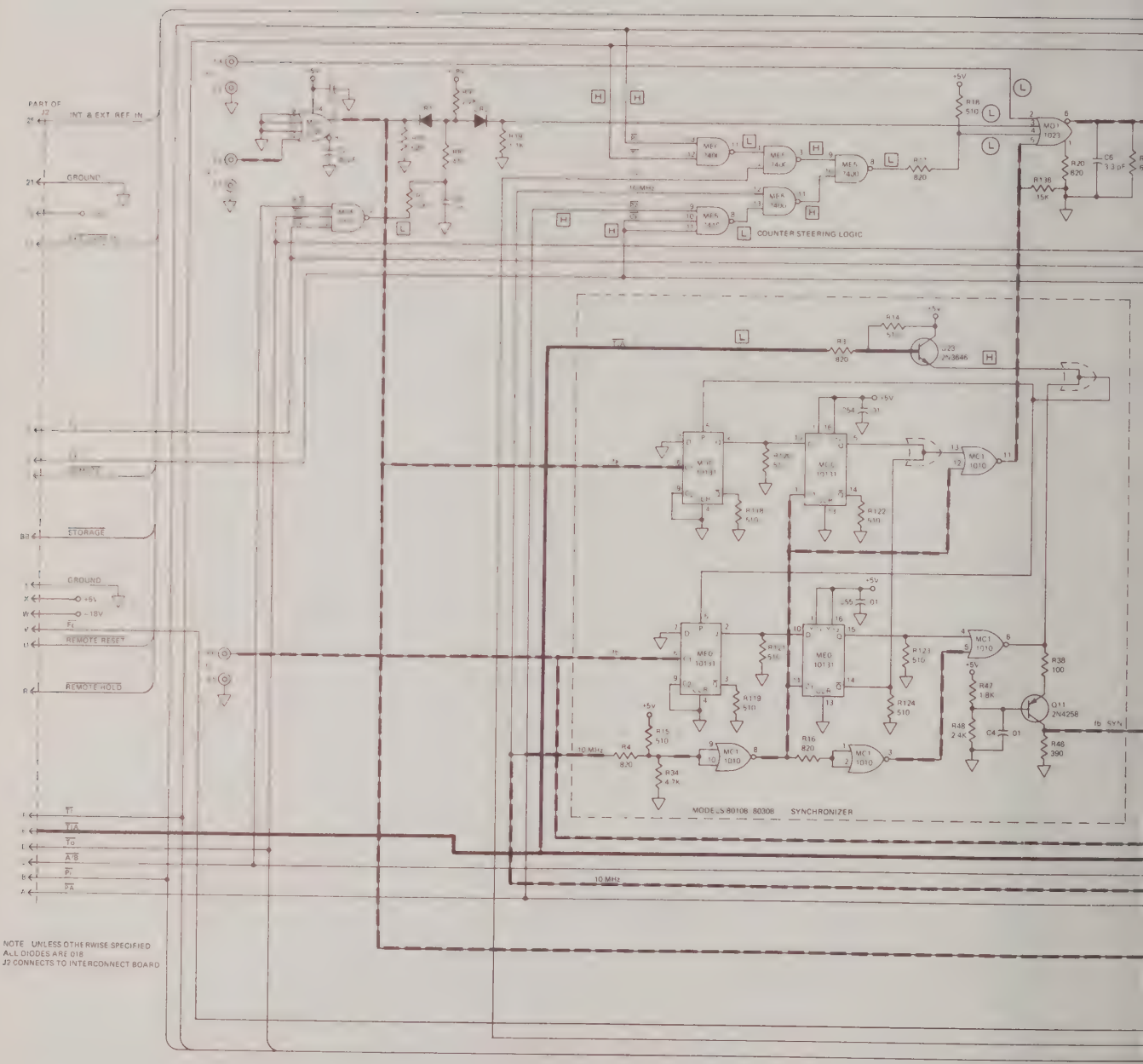
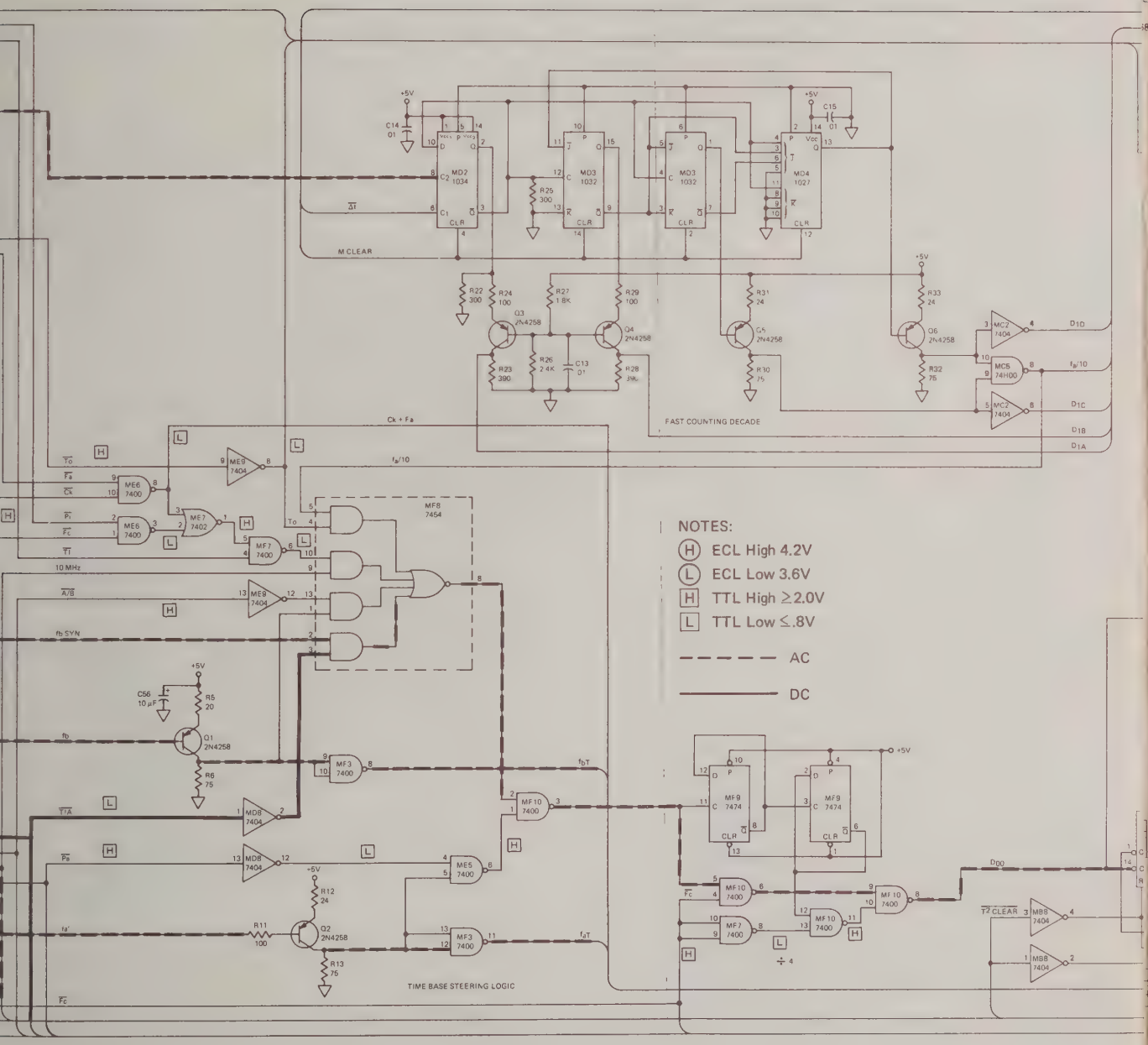
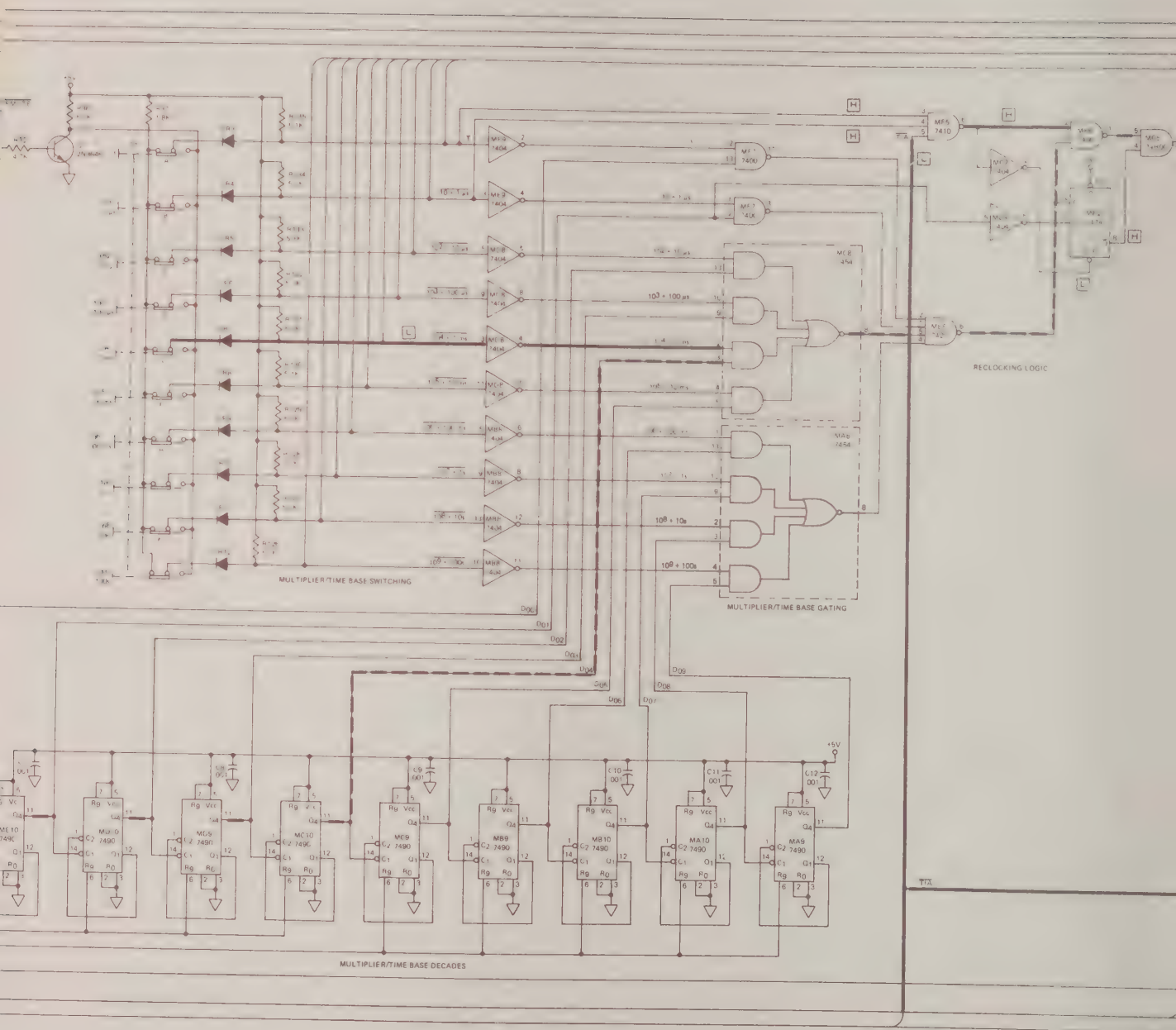


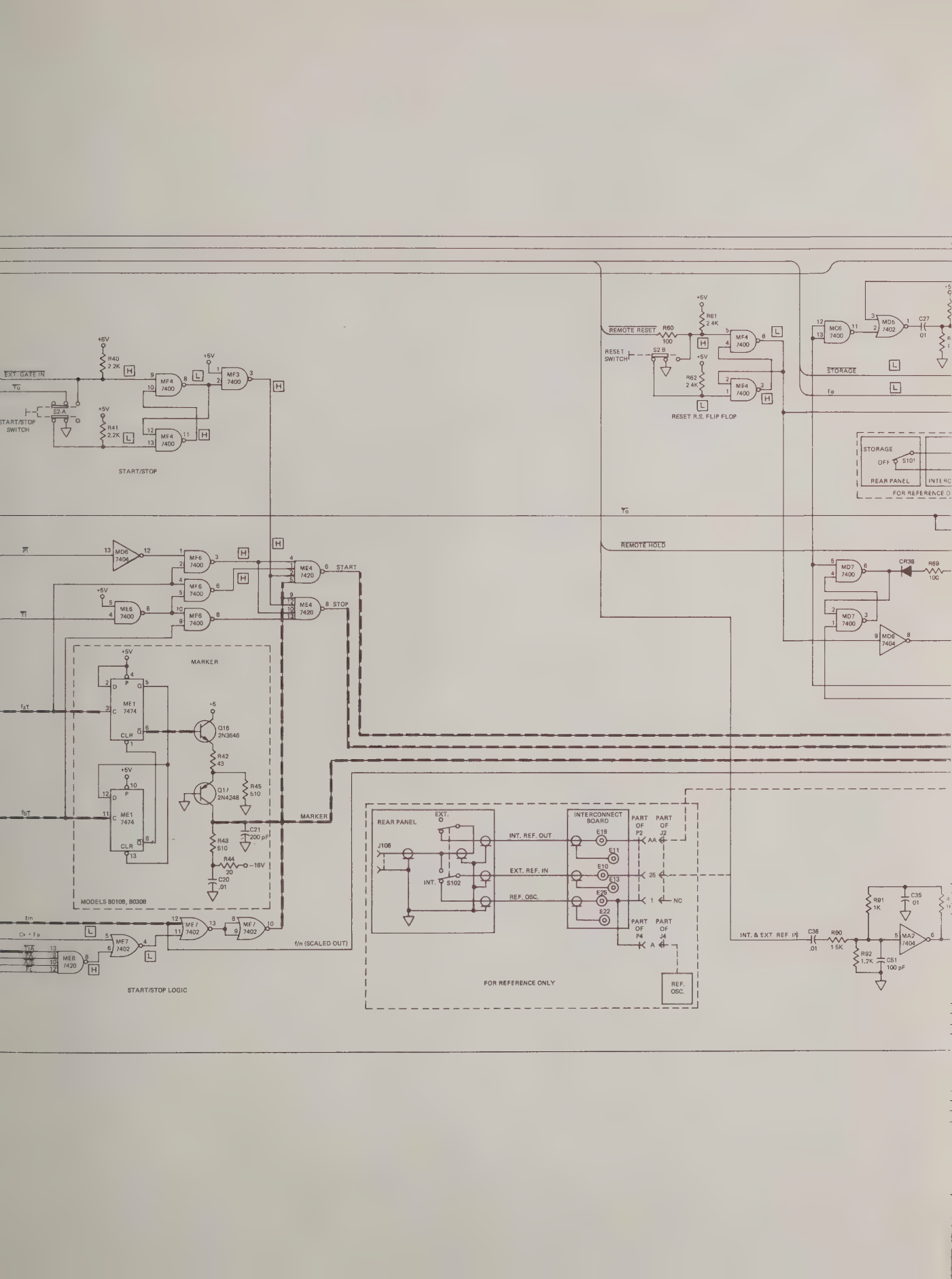
Figure 5.32 - Signal Flow for A/B Ratio Mode 5-35

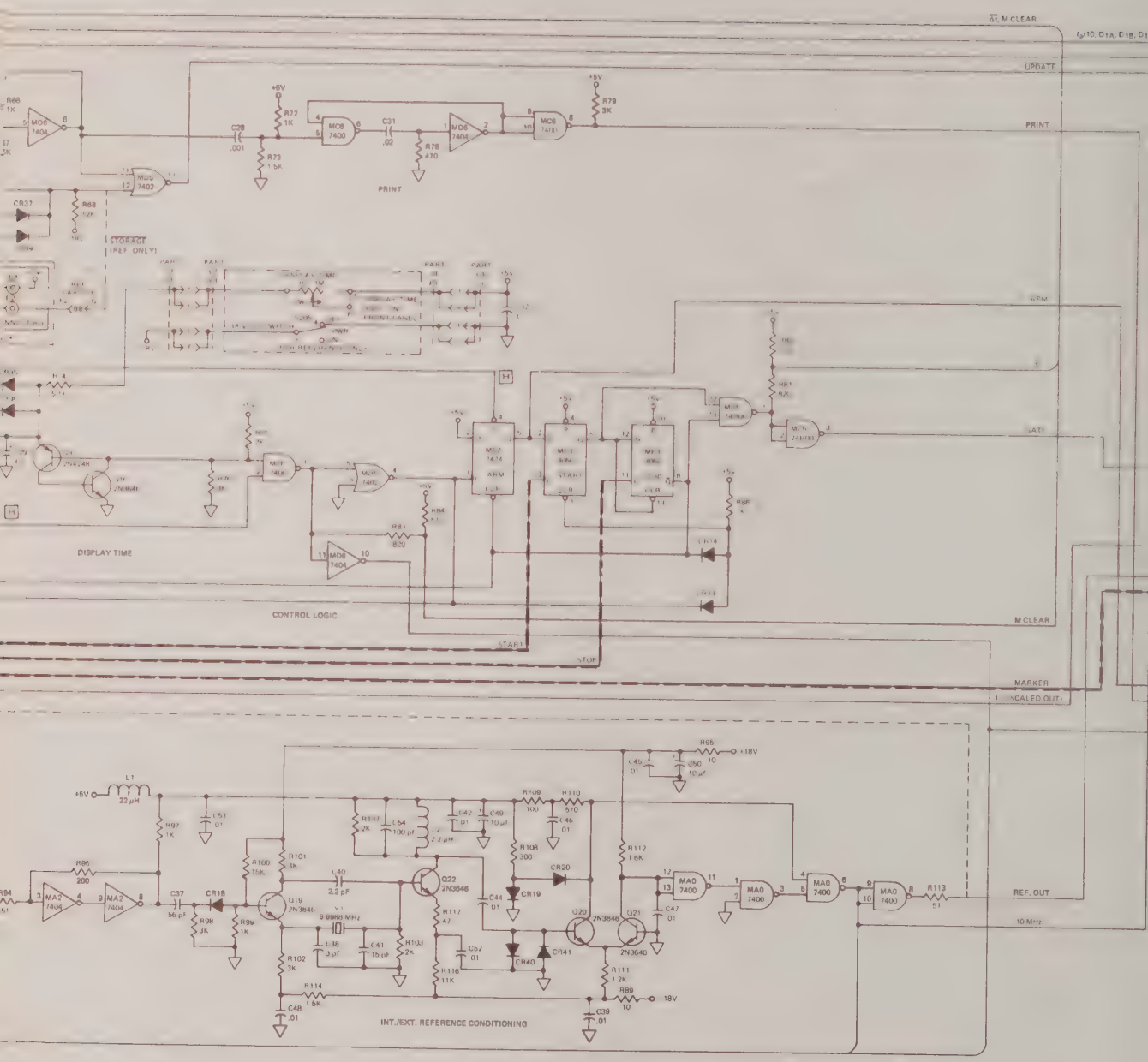

PART OF J2
INT. & EXT. REF. IN
GROUND
STORAGE
GROUND
+5V
-18V
REMOTE RESET
REMOTE HOLD
10 MHz
COUNTER STEERING LOGIC
MODELS 8010B 8030B SYNCHRONIZER
NOTE: UNLESS OTHERWISE SPECIFIED
ALL DIODES ARE 018
J2 CONNECTS TO INTERCONNECT BOARD

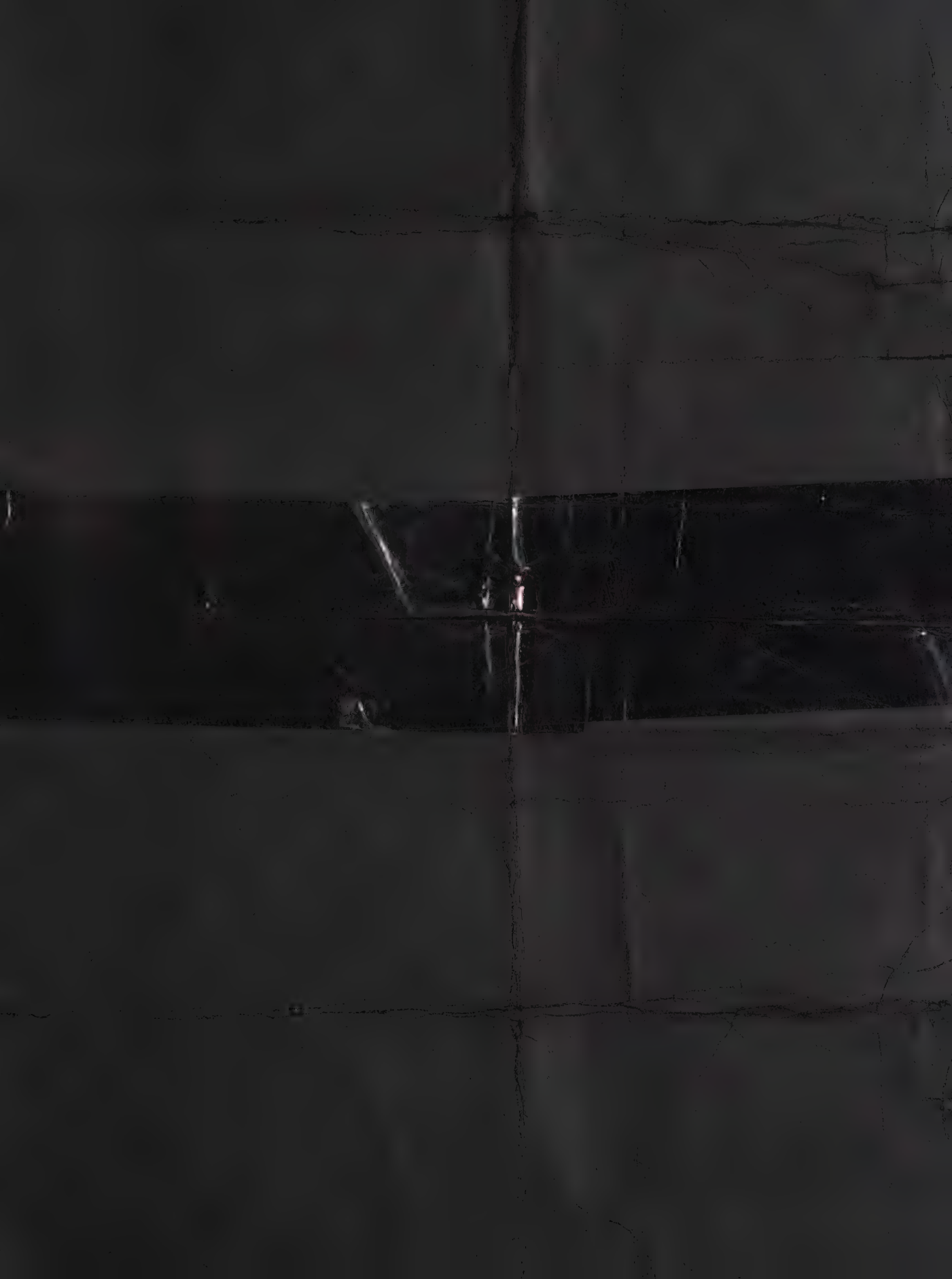

NOTES:
H ECL High 4.2V
L ECL Low 3.6V
H TTL High ≥2.0V
L TTL Low ≤.8V
AC
DC
M CLEAR
FAST COUNTING DECADE
TIME BASE STEERING LOGIC
÷ 4
10 MHz

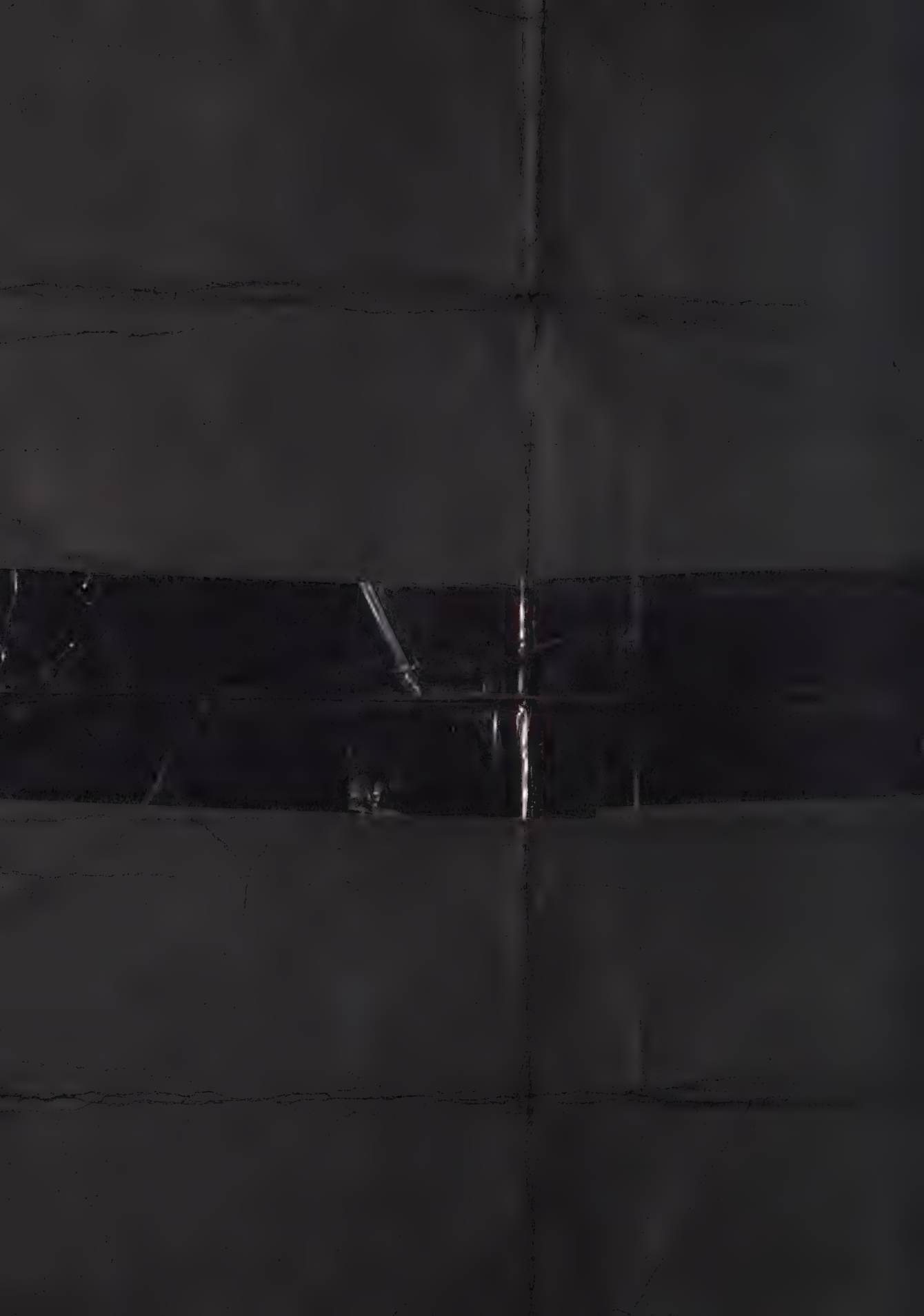


5-36 Figure 5.33 - Signal Flow for Time Interval Average Mode


START/STOP
START/STOP LOGIC
RESET R.S. FLIP FLOP
REMOTE RESET
REMOTE HOLD
STORAGE
MARKER
MODELS 80108, 80308
REAR PANEL
INTERCONNECT BOARD
INT. REF. OUT
EXT. REF. IN
REF. OSC.
FOR REFERENCE ONLY
INT. & EXT. REF. IN
f/n (SCALED OUT)


MCLEAR
UPDATE
PRINT
STORAGE
(REF. ONLY)
DISPLAY TIME
CONTROL LOGIC
START
MARKER
(SCALED OUT)
INT./EXT. REFERENCE CONDITIONING
REF. OUT
10 MHz





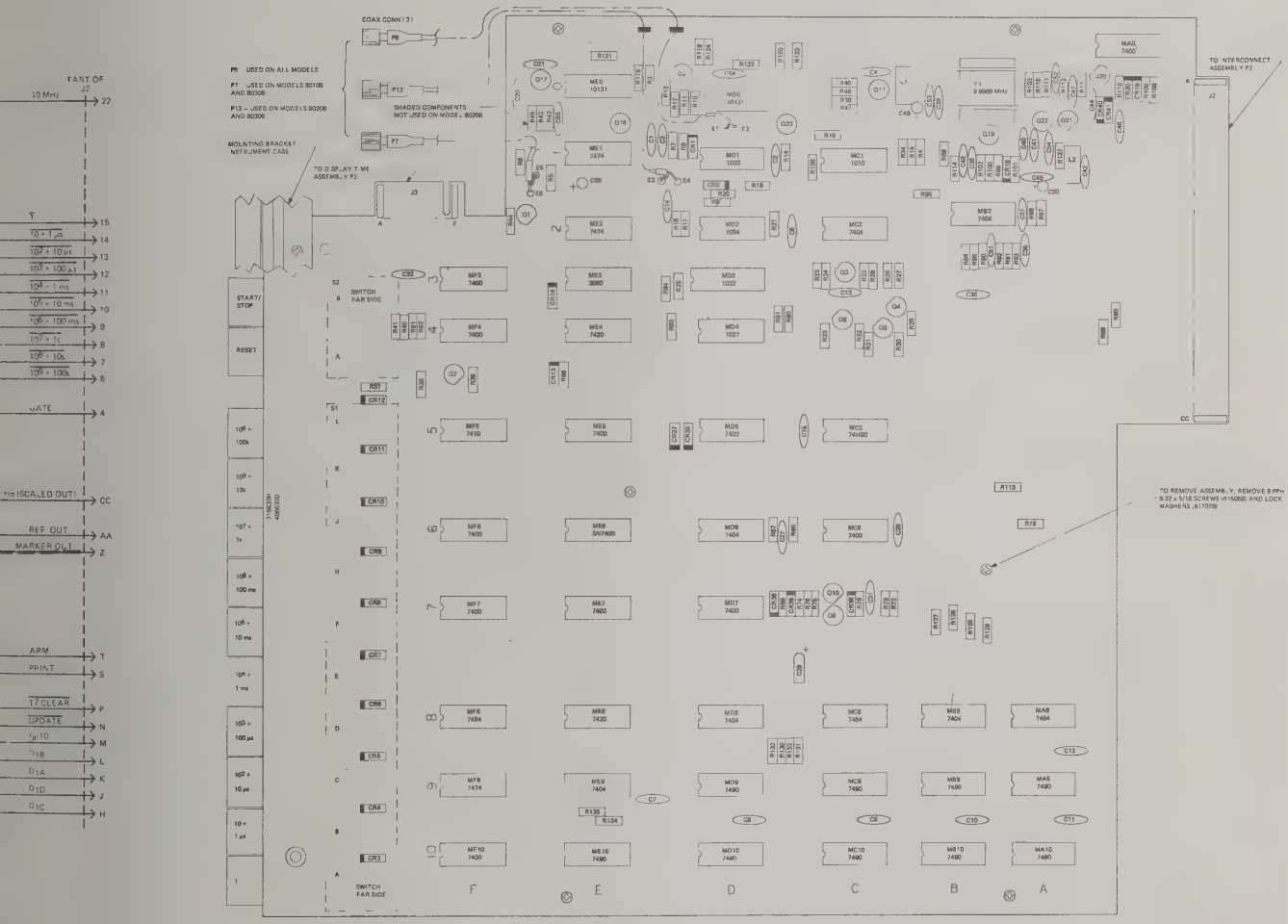


Figure 5.33 - Signal Flow for Time Interval Average Mode 5-37

SECTION 6 SCHEMATICS

Figure	Title	Page
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6.6	Schematic, Readout Board	6-9
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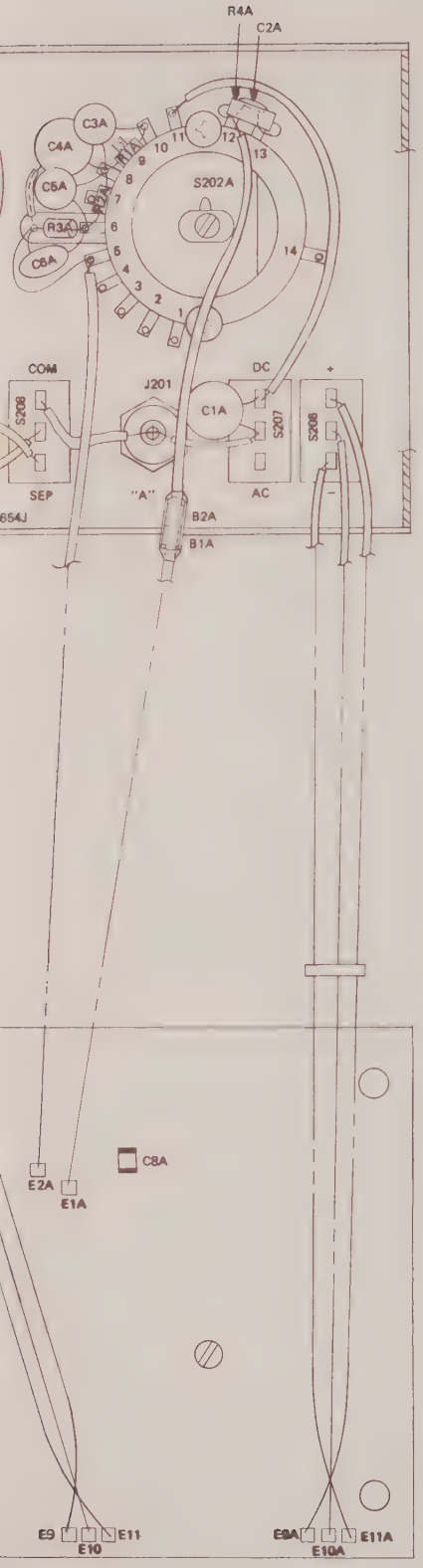
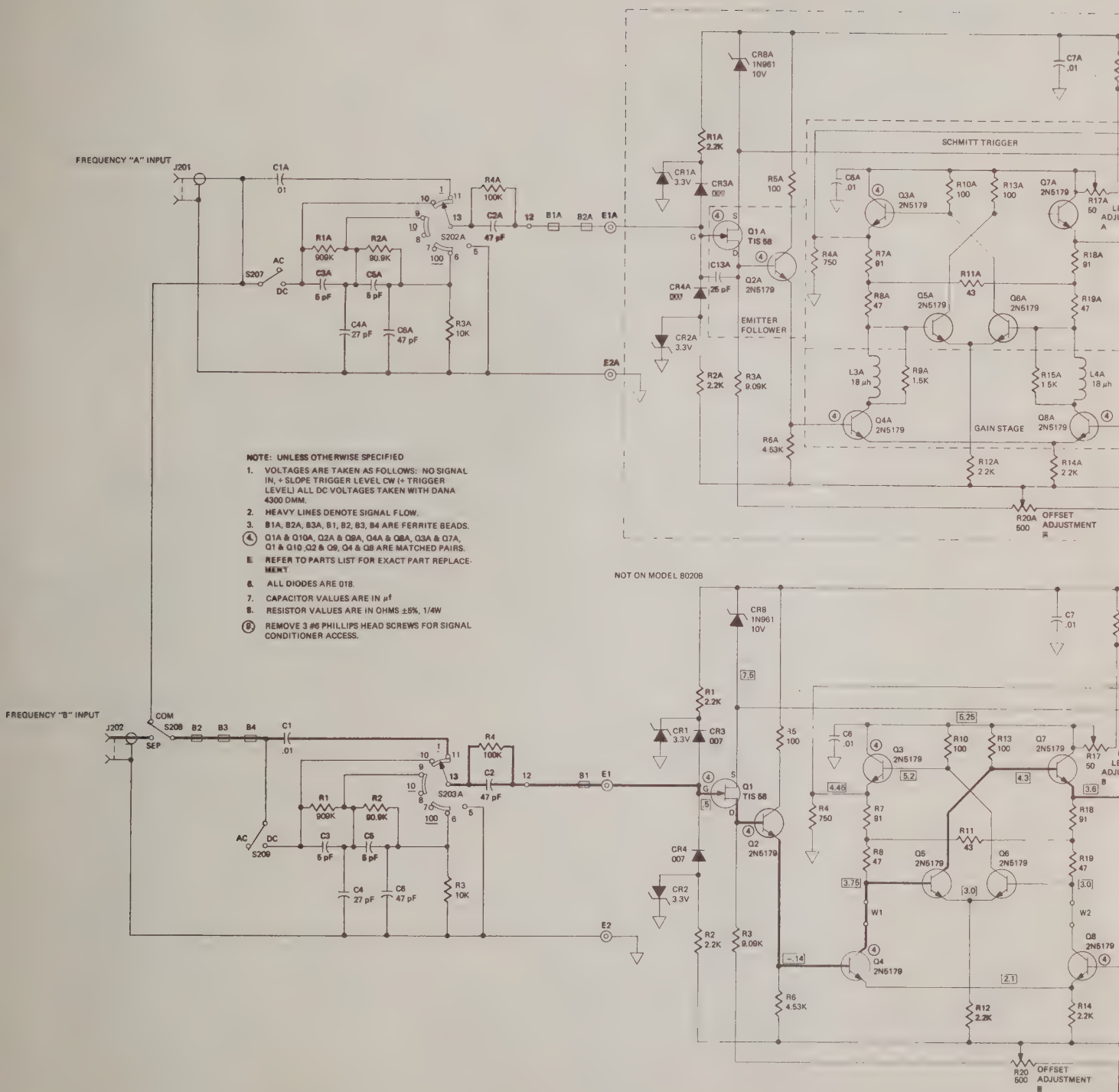
6.9	Schematic, Rear Panel	6-13
6.10	Layout, Rear Panel (Used with Options 200 & 300) (406732)	6-14


R4A
C2A
C3A
C4A
C5A
R3A
C6A
S202A
COM
DC
J201
C1A
S207
S206
S208
SEP
"A"
AC
B2A
B1A
C8A
E2A
E1A
E9
E10
E11
E9A
E10A
E11A


FREQUENCY "A" INPUT
J201
C1A .01
R1A 909K
R2A 90.9K
C3A 5 pF
C5A 5 pF
C4A 27 pF
C6A 47 pF
R3A 10K
S207 AC DC
S202A
R4A 100K
C2A 47 pF
B1A B2A E1A
E2A
CR8A 1N961 10V
C7A .01
R1A 2.2K
CR1A 3.3V
CR3A 007
R5A 100
Q1A TIS 58
C13A 25 pF
CR4A 007
Q2A 2N5179
CR2A 3.3V
R2A 2.2K
R3A 9.09K
R4A 750
SCHMITT TRIGGER
C6A .01
Q3A 2N5179
R10A 100
R13A 100
Q7A 2N5179
R17A 50
R7A 91
R11A 43
R8A 47
Q5A 2N5179
Q6A 2N5179
R18A 91
R19A 47
EMITTER FOLLOWER
L3A 18 µh
R9A 1.5K
R15A 1.5K
L4A 18 µh
Q4A 2N5179
GAIN STAGE
Q8A 2N5179
R6A 4.53K
R12A 2.2K
R14A 2.2K
R20A 500
OFFSET ADJUSTMENT
NOTE: UNLESS OTHERWISE SPECIFIED
1. VOLTAGES ARE TAKEN AS FOLLOWS: NO SIGNAL IN, + SLOPE TRIGGER LEVEL CW (+ TRIGGER LEVEL) ALL DC VOLTAGES TAKEN WITH DANA 4300 DMM.
2. HEAVY LINES DENOTE SIGNAL FLOW.
3. B1A, B2A, B3A, B1, B2, B3, B4 ARE FERRITE BEADS.
4. Q1A & Q10A, Q2A & Q9A, Q4A & Q8A, Q3A & Q7A, Q1 & Q10, Q2 & Q9, Q4 & Q8 ARE MATCHED PAIRS.
5. REFER TO PARTS LIST FOR EXACT PART REPLACEMENT.
6. ALL DIODES ARE 018.
7. CAPACITOR VALUES ARE IN µf
8. RESISTOR VALUES ARE IN OHMS ±5%, 1/4W
9. REMOVE 3 #6 PHILLIPS HEAD SCREWS FOR SIGNAL CONDITIONER ACCESS.
NOT ON MODEL 8020B
FREQUENCY "B" INPUT
J202
COM
SEP
S208
B2 B3 B4
C1 .01
S203A
R4 100K
C2 47 pF
B1 E1
E2
S209 AC DC
R1 909K
R2 90.9K
C3 5 pF
C5 5 pF
C4 27 pF
C8 47 pF
R3 10K
CR8 1N961 10V
C7 .01
R1 2.2K
CR1 3.3V
CR3 007
Q1 TIS 58
CR4 007
Q2 2N5179
CR2 3.3V
R2 2.2K
R3 9.09K
C6 .01
Q3 2N5179
R10 100
R13 100
Q7 2N5179
R17 50
R4 750
R7 91
R11 43
R8 47
Q5 2N5179
Q6 2N5179
R18 91
R19 47
W1
W2
Q4 2N5179
Q8 2N5179
R6 4.53K
R12 2.2K
R14 2.2K
R20 500
OFFSET ADJUSTMENT

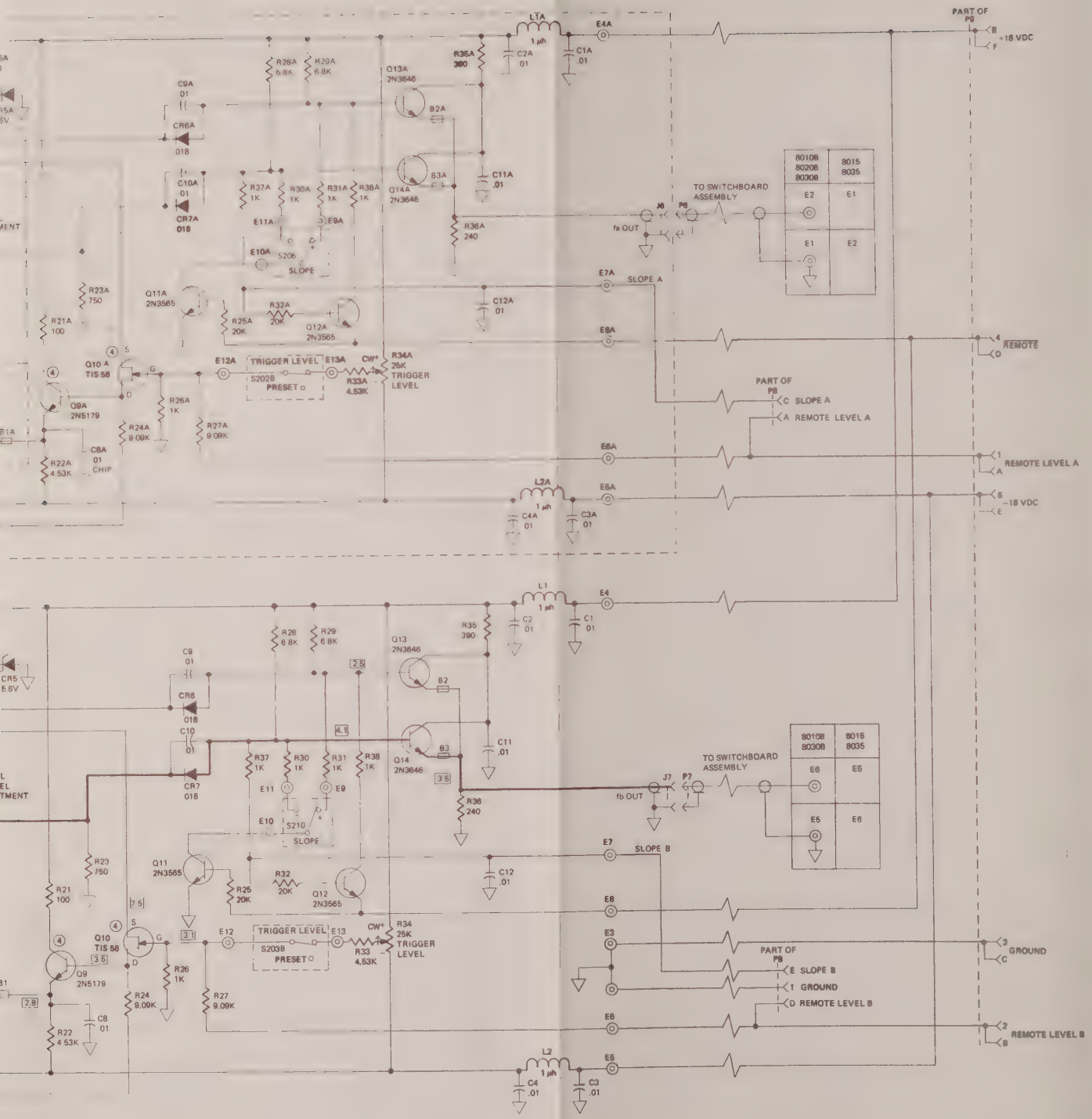
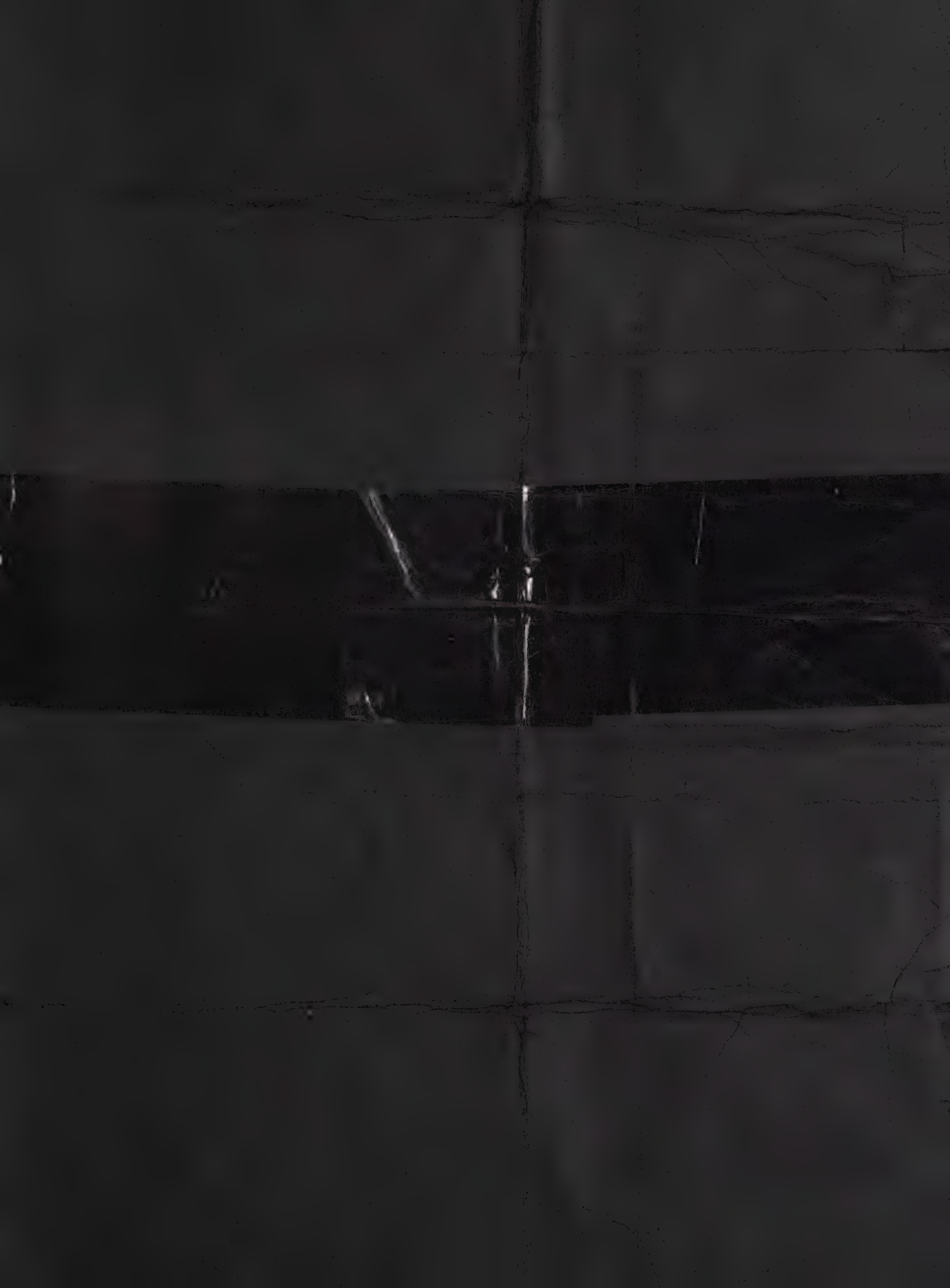
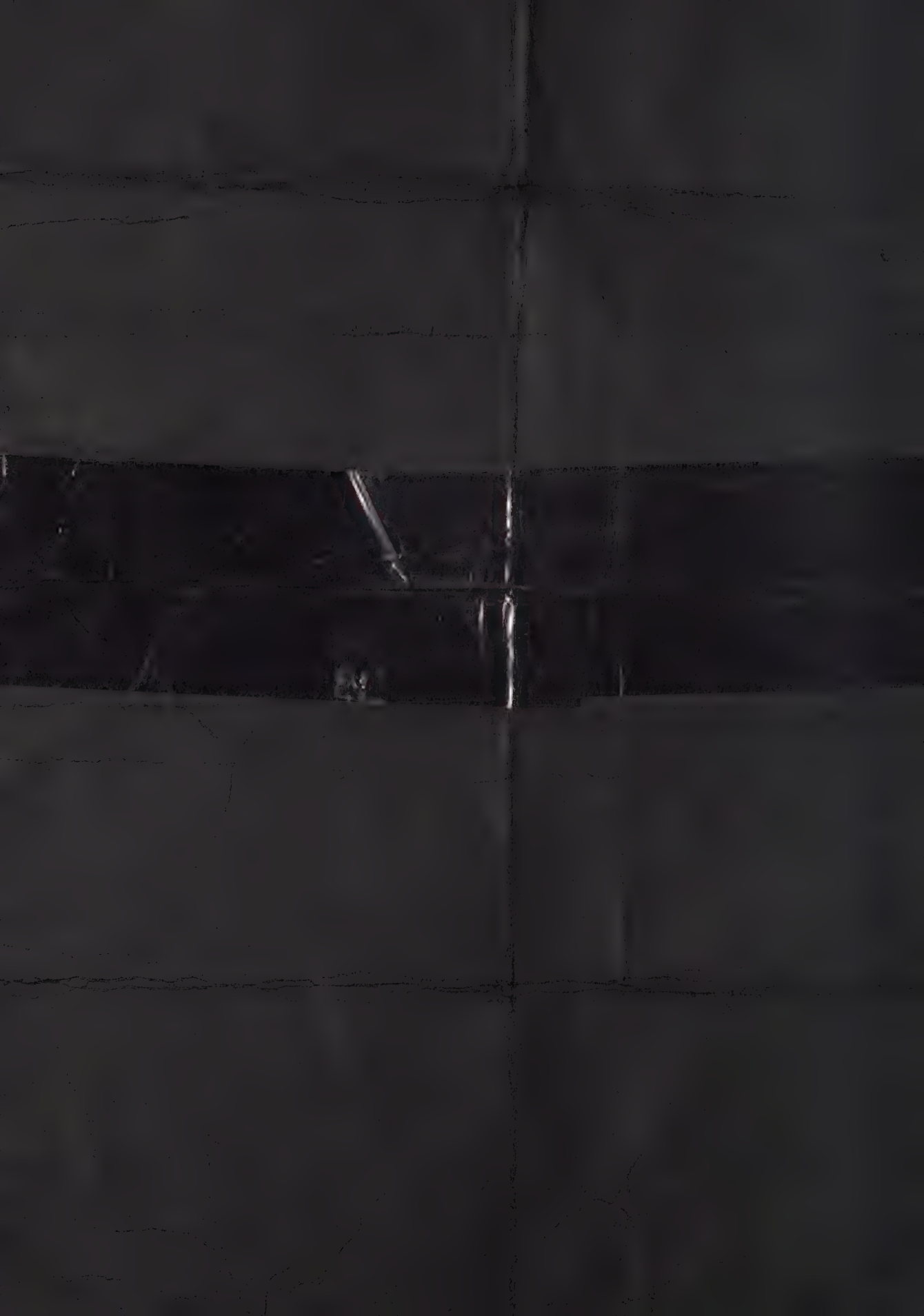
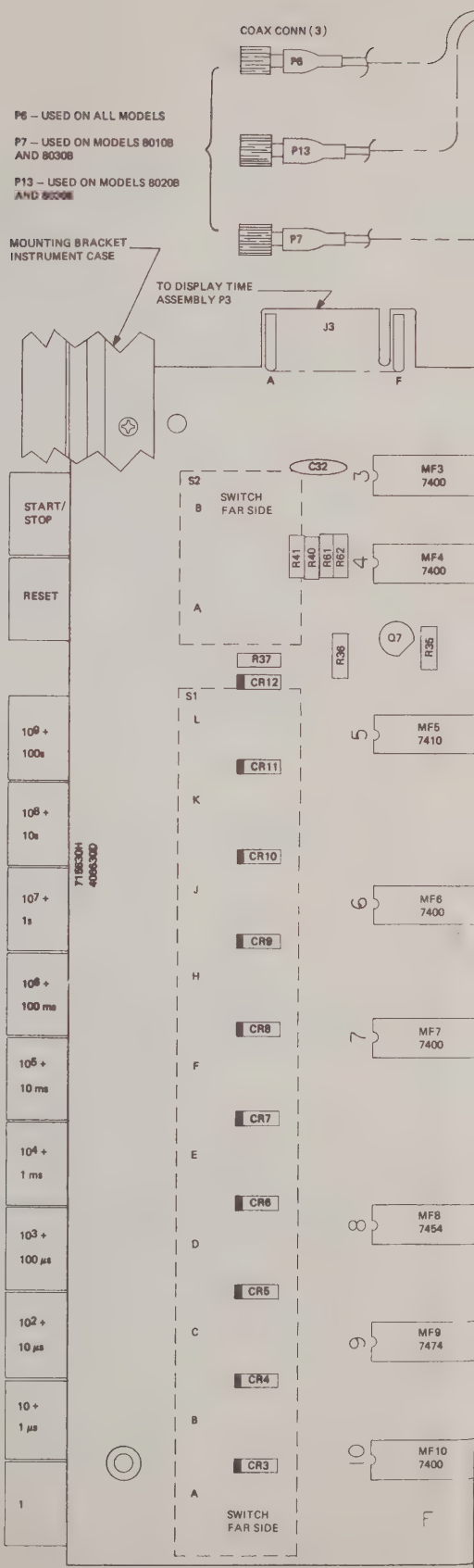


Figure 6.2 - Schematic, Signal Conditioning – Dual






COAX CONN (3)
P6
P13
P7
P6 – USED ON ALL MODELS
P7 – USED ON MODELS 80108 AND 80308
P13 – USED ON MODELS 80208 AND 80308
MOUNTING BRACKET INSTRUMENT CASE
TO DISPLAY TIME ASSEMBLY P3
J3
A
F
C32
S2
B
SWITCH FAR SIDE
A
START/ STOP
RESET
R41
R40
R61
R62
Q7
R36
R35
R37
CR12
S1
L
K
J
H
F
E
D
C
B
A
CR11
CR10
CR9
CR8
CR7
CR6
CR5
CR4
CR3
SWITCH FAR SIDE
10^9 + 100s
10^8 + 10s
10^7 + 1s
10^6 + 100 ms
10^5 + 10 ms
10^4 + 1 ms
10^3 + 100 µs
10^2 + 10 µs
10 + 1 µs
1
7186304
4086300
3
MF3 7400
4
MF4 7400
5
MF5 7410
6
MF6 7400
7
MF7 7400
8
MF8 7454
9
MF9 7474
10
MF10 7400
F

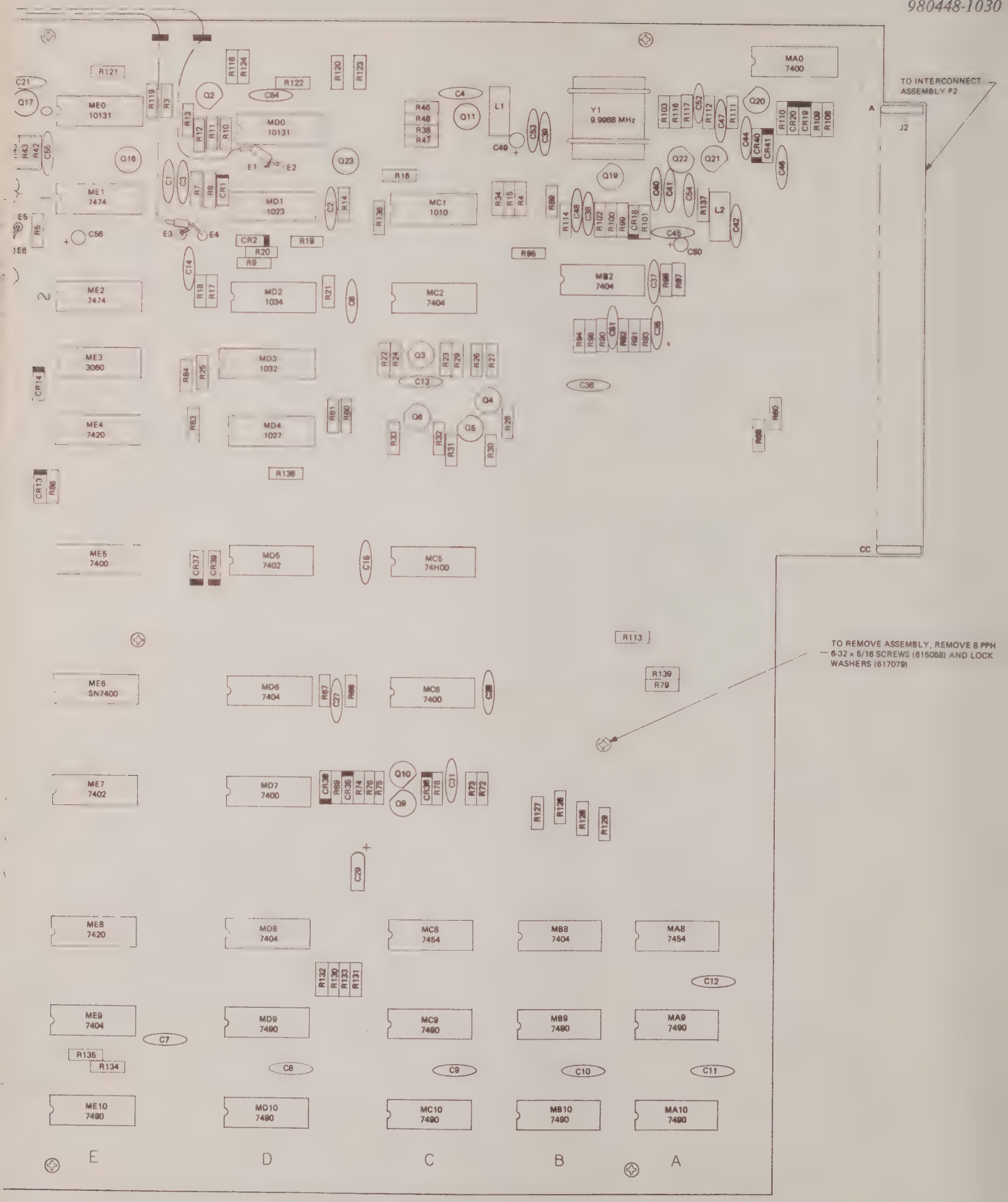
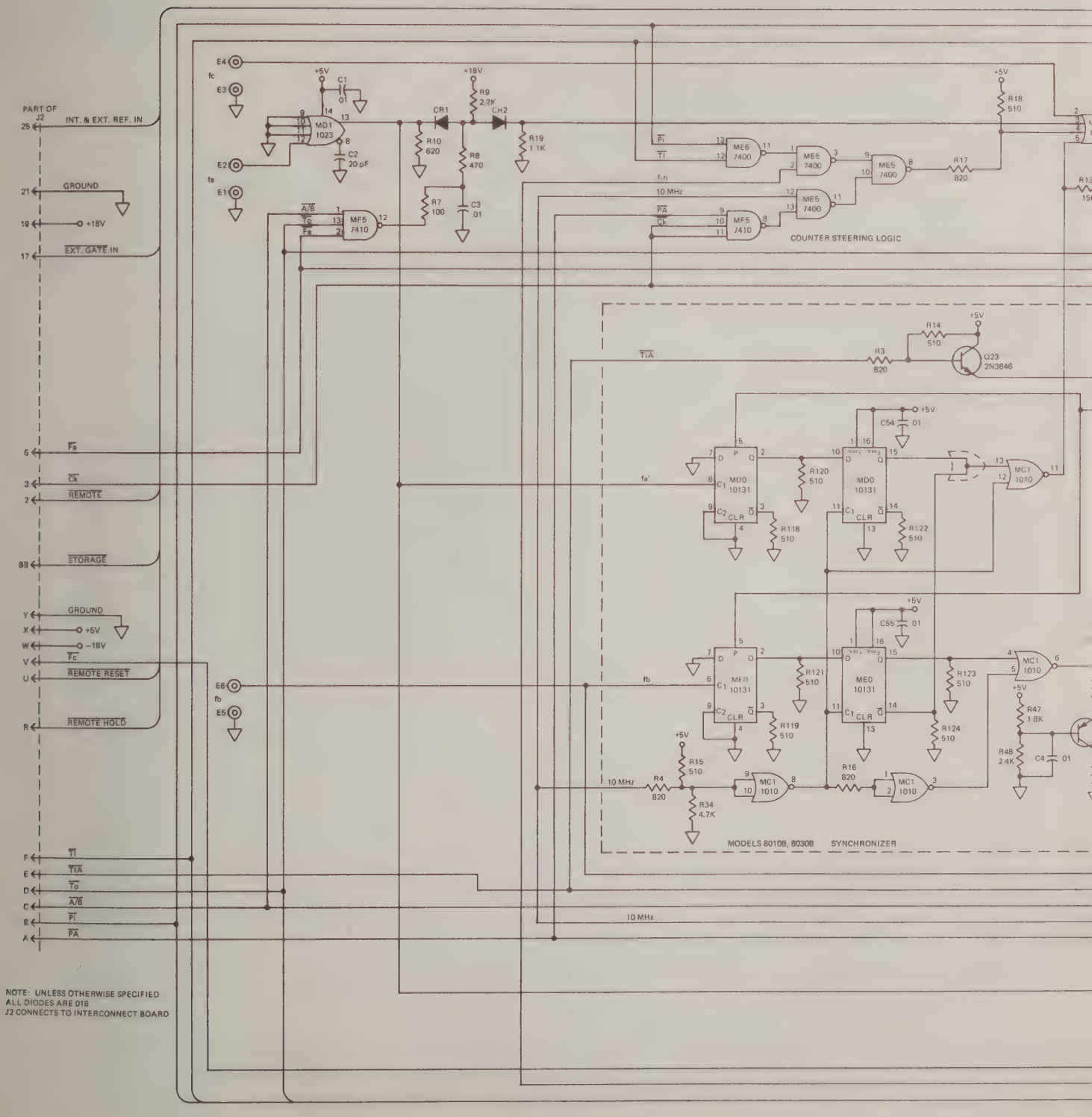


Figure 6.3 - Layout, Switch Board TIA


PART OF J2
25 INT. & EXT. REF. IN
21 GROUND
19 +18V
17 EXT. GATE IN
6 Fa
3 Ck
2 REMOTE
BB STORAGE
Y GROUND
X +5V
W −18V
V Fc
U REMOTE RESET
R REMOTE HOLD
F TI
E TIA
D To
C A/B
B PI
A PA
E4
E3
E2
E1
E6
E5
fc
fb
fa
+5V
+18V
C1 01
C2 20 pF
MD1 1023
CR1
CR2
R9 2.2K
R10 620
R8 470
R19 1.1K
R7 100
C3 .01
MF5 7410
ME6 7400
ME5 7400
R18 510
R17 820
10 MHz
COUNTER STEERING LOGIC
R14 510
R3 820
Q23 2N3646
C54 01
C55 01
MD0 10131
R120 510
R118 510
R122 510
R121 510
R119 510
R123 510
R124 510
MC1 1010
R15 510
R4 820
R34 4.7K
R16 820
R47 1.8K
R48 2.4K
C4 01
MODELS 8010B, 8030B SYNCHRONIZER
NOTE: UNLESS OTHERWISE SPECIFIED
ALL DIODES ARE 018
J2 CONNECTS TO INTERCONNECT BOARD

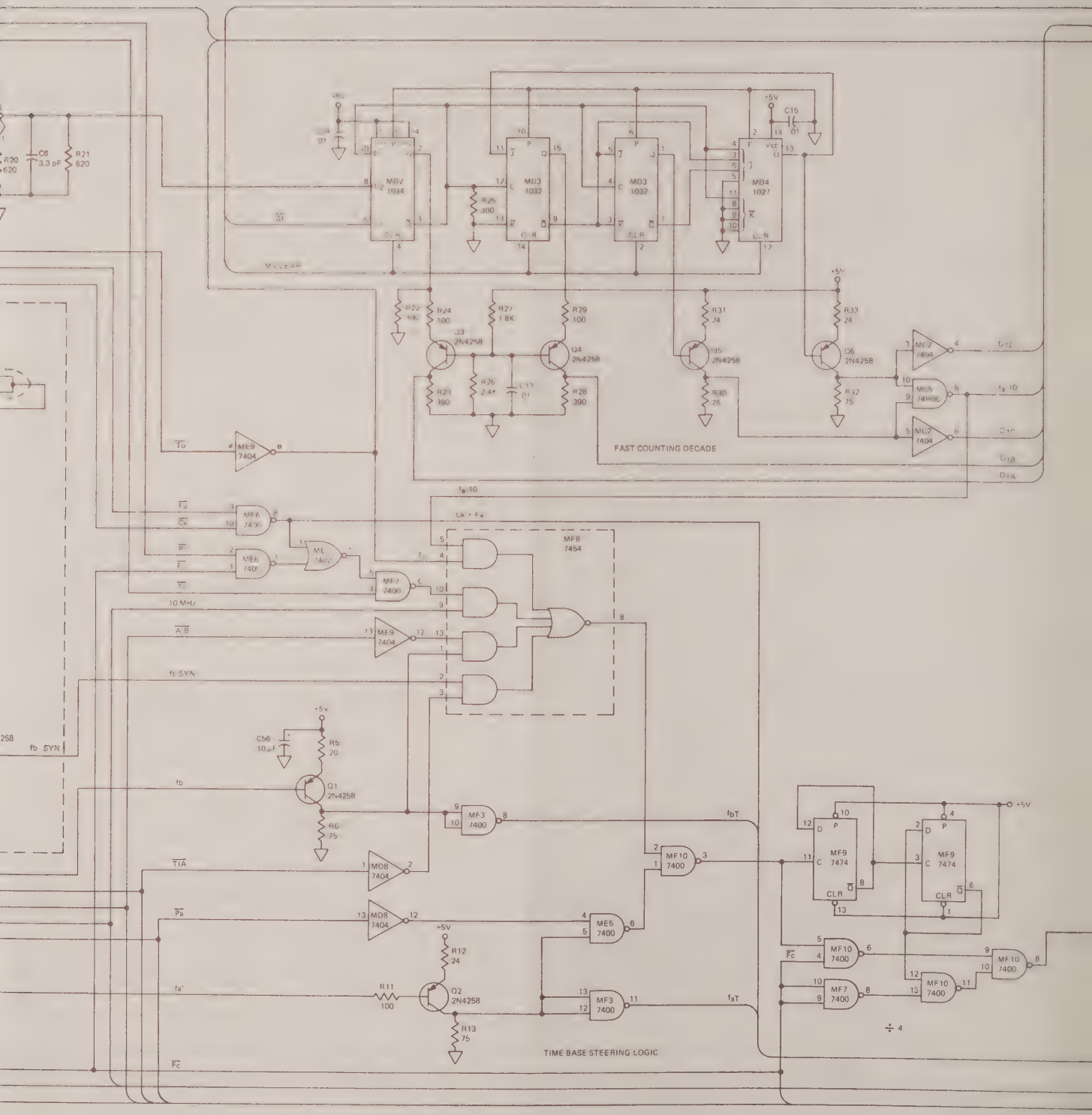
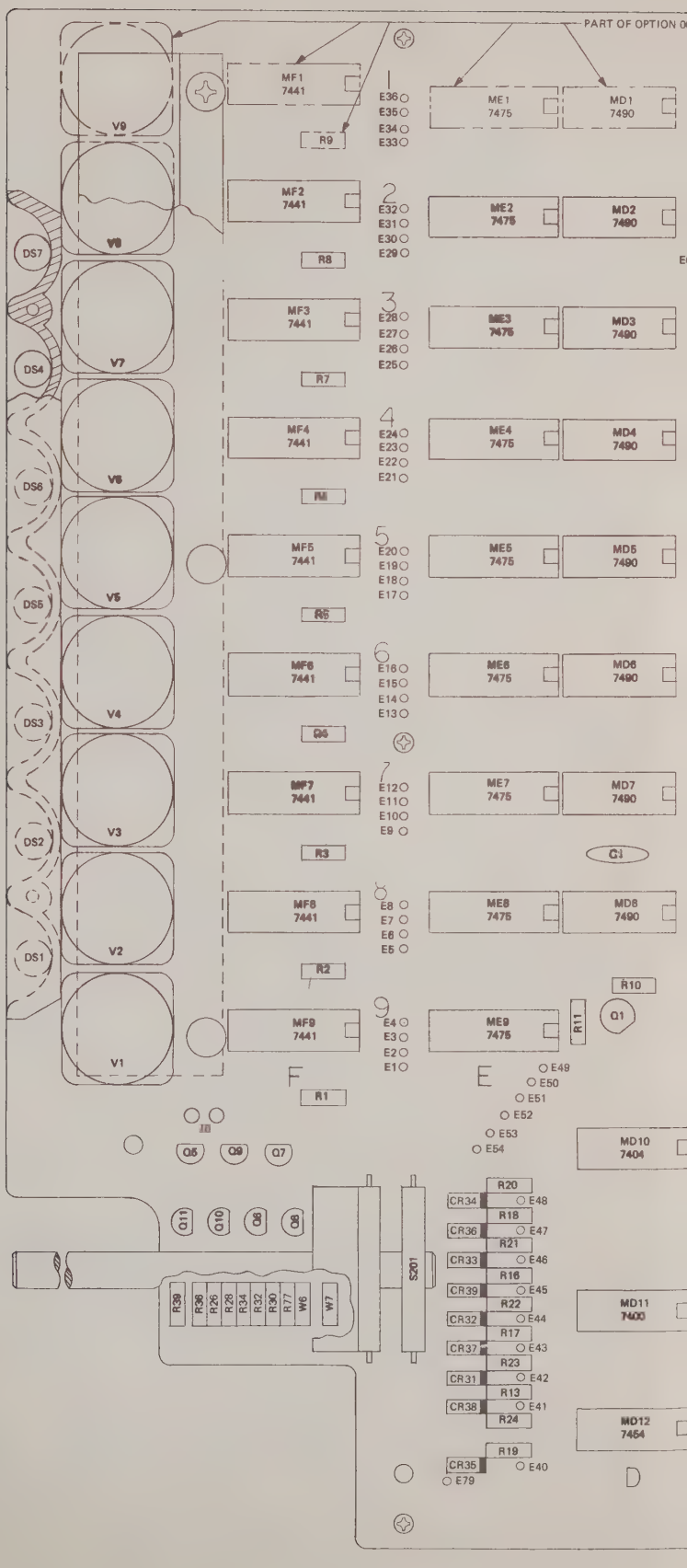


Figure 6.4 - Schematic, Switch Board TIA


PART OF OPTION 0
MF1 7441
MF2 7441
MF3 7441
MF4 7441
MF5 7441
MF6 7441
MF7 7441
MF8 7441
MF9 7441
ME1 7475
ME2 7475
ME3 7475
ME4 7475
ME5 7475
ME6 7475
ME7 7475
ME8 7475
ME9 7475
MD1 7490
MD2 7490
MD3 7490
MD4 7490
MD5 7490
MD6 7490
MD7 7490
MD8 7490
MD10 7404
MD11 7400
MD12 7454
V1
V2
V3
V4
V5
V6
V7
V8
V9
DS1
DS2
DS3
DS4
DS5
DS6
DS7
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
Q1
Q5
Q6
Q7
Q8
Q9
Q10
Q11
C1
S201
R20
R18
R21
R16
R22
R17
R23
R13
R24
R19
R26
R28
R34
R32
R30
R77
W6
W7
R36
R39
CR34
CR36
CR33
CR39
CR32
CR37
CR31
CR38
CR35
E79
E1
E2
E3
E4
E5
E6
E7
E8
E9
E10
E11
E12
E13
E14
E15
E16
E17
E18
E19
E20
E21
E22
E23
E24
E25
E26
E27
E28
E29
E30
E31
E32
E33
E34
E35
E36
E40
E41
E42
E43
E44
E45
E46
E47
E48
E49
E50
E51
E52
E53
E54
F
E
D

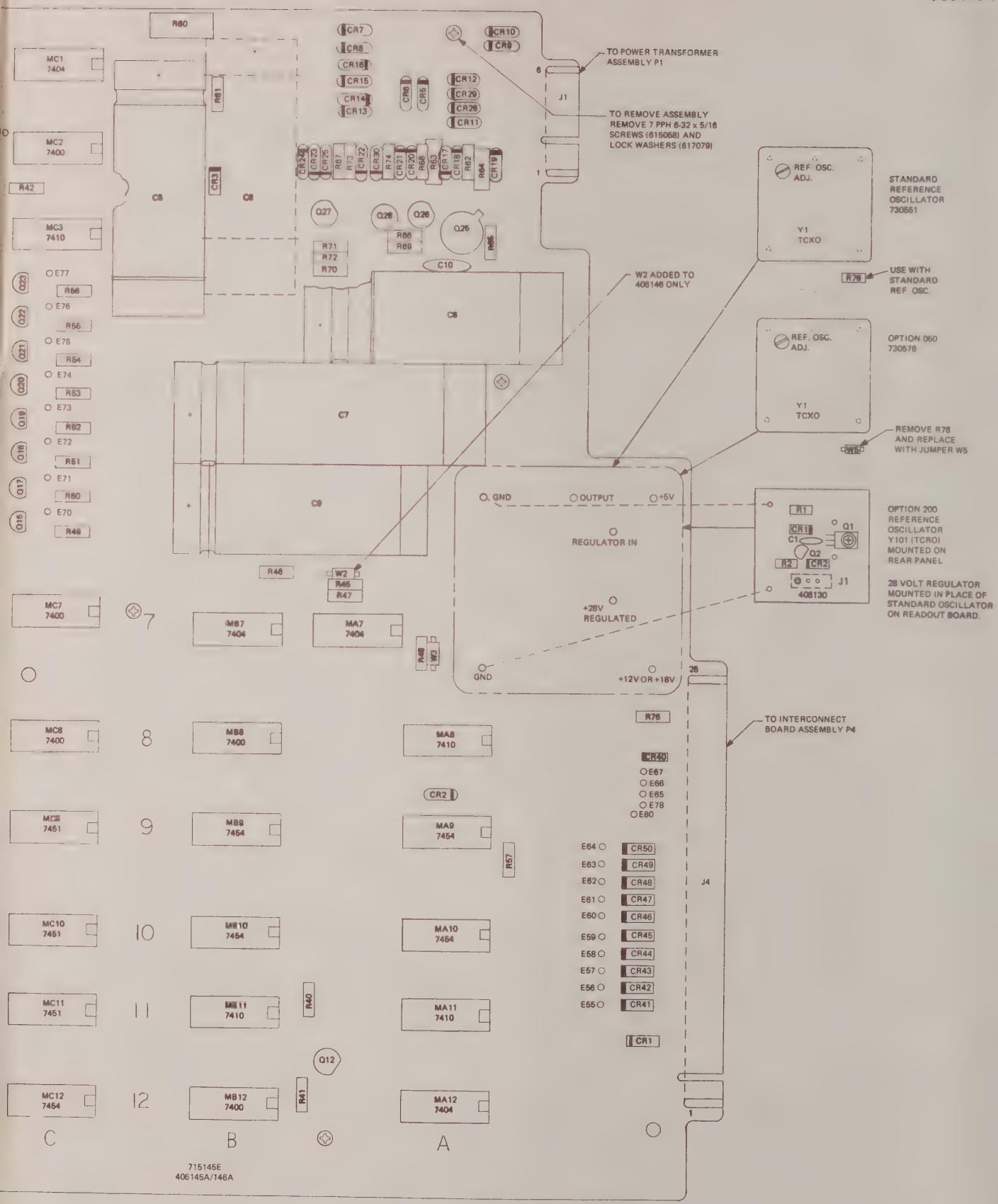
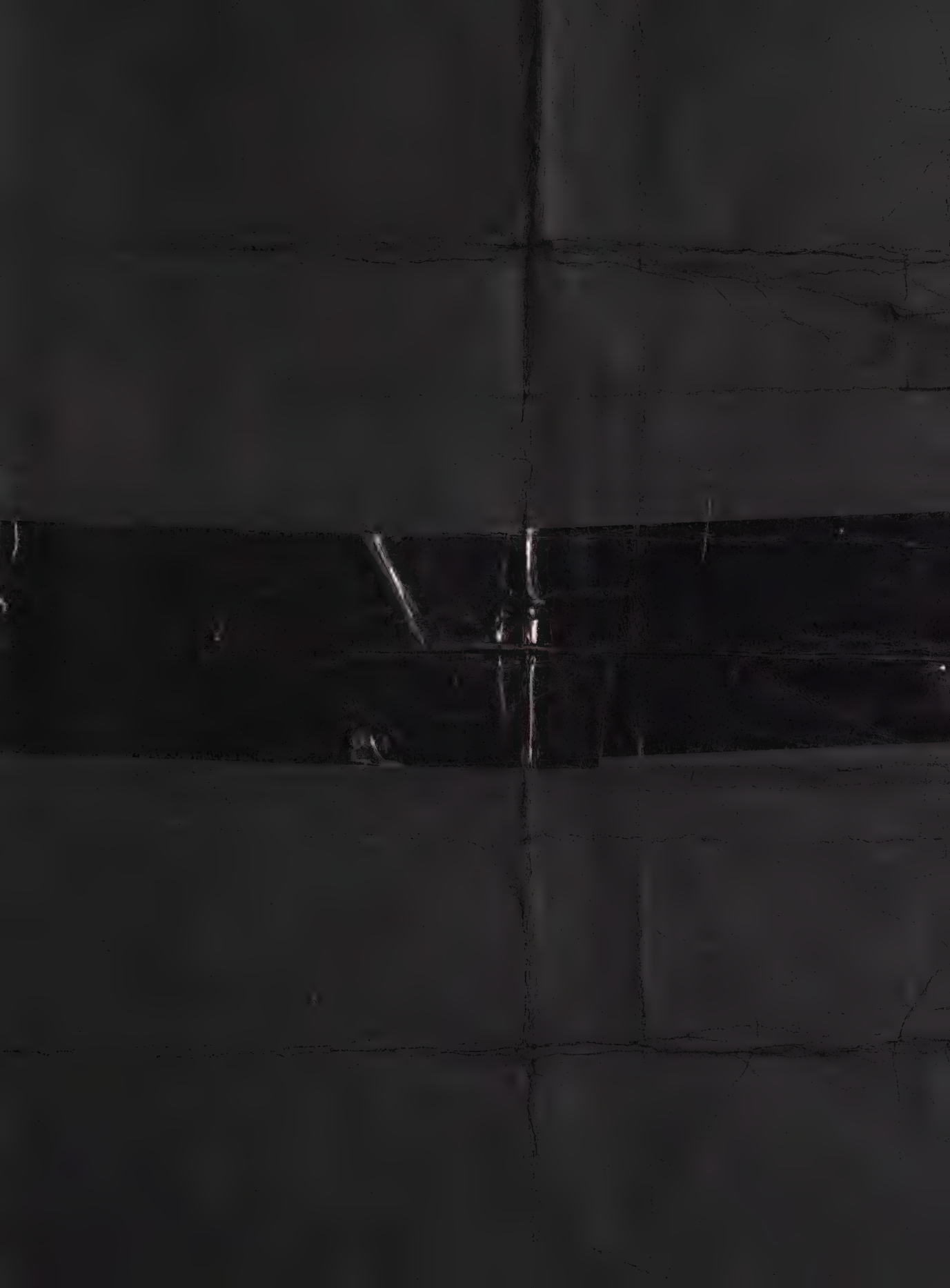
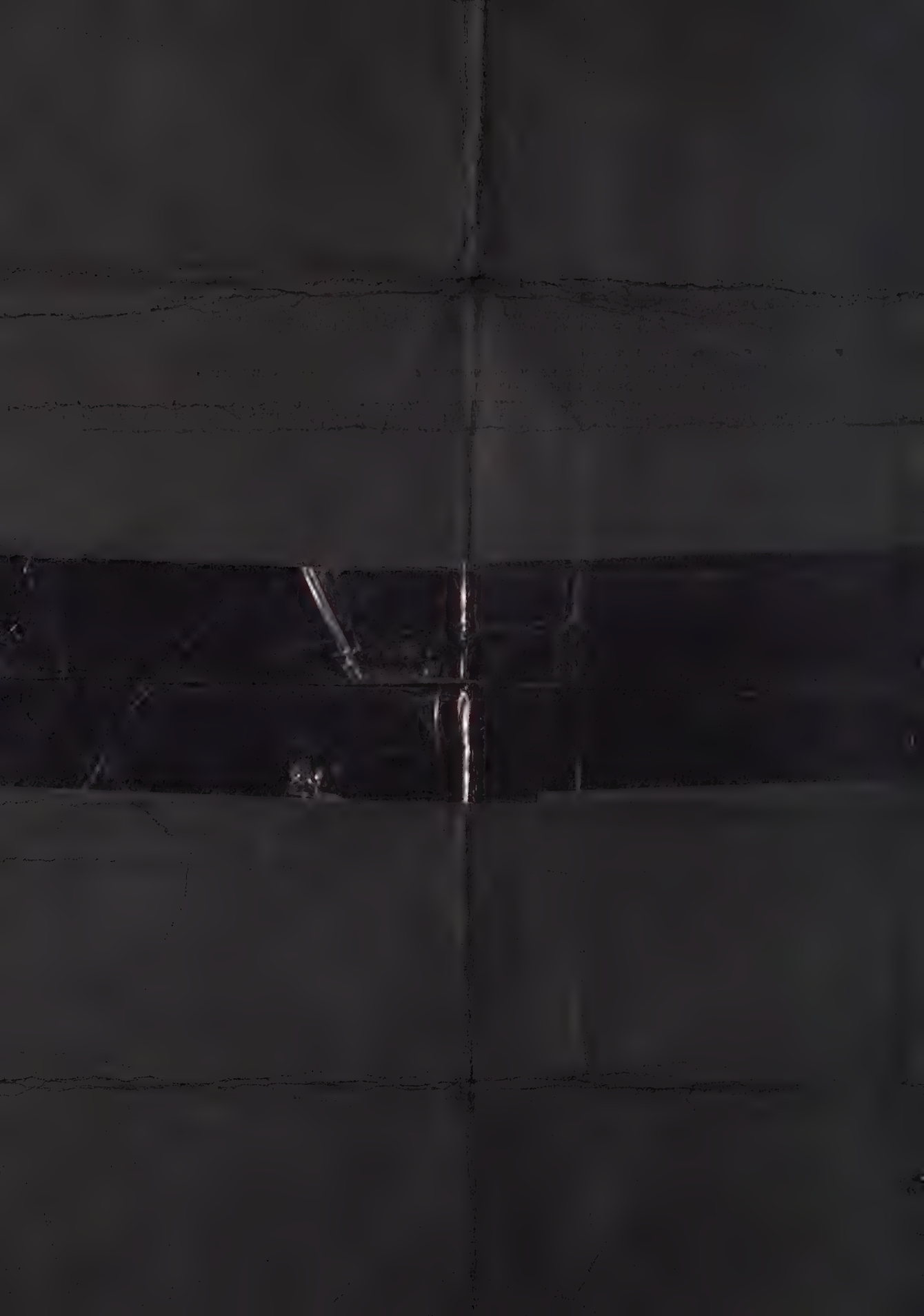
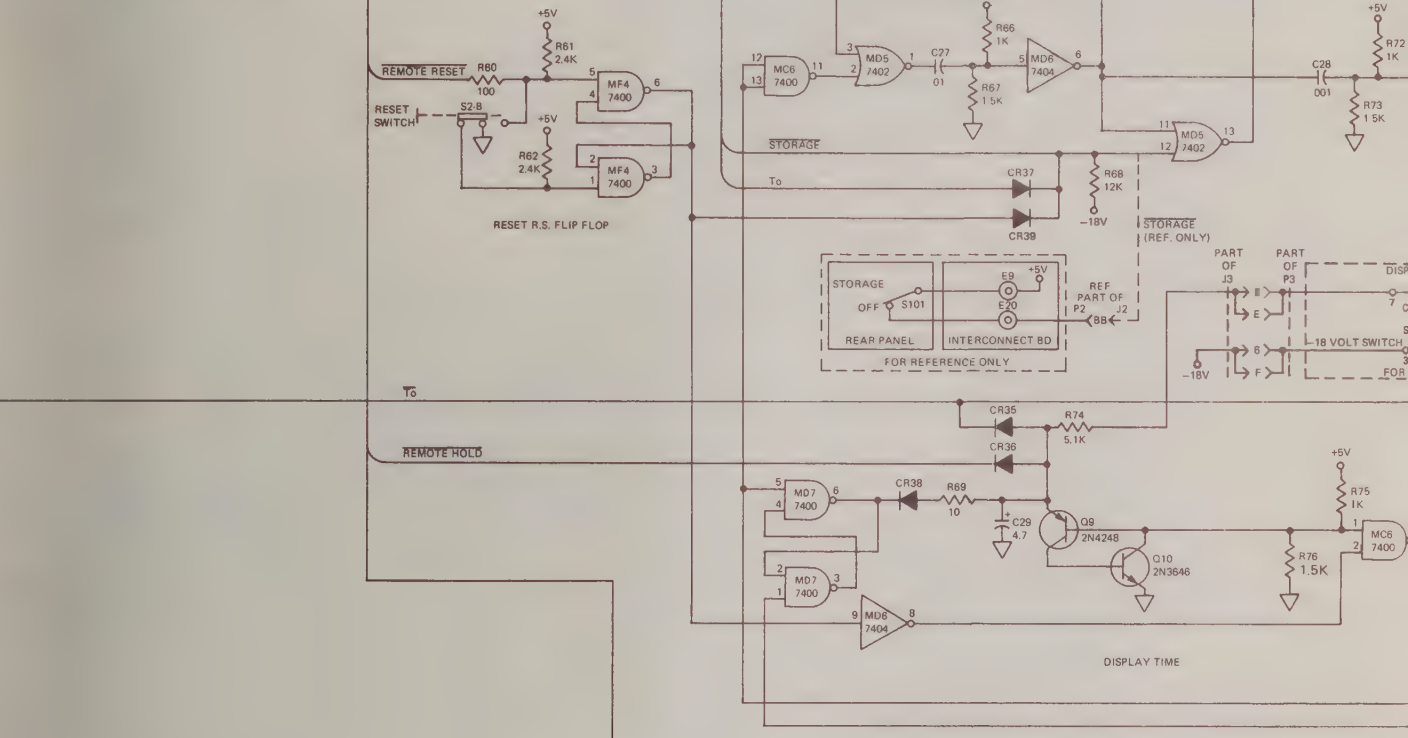
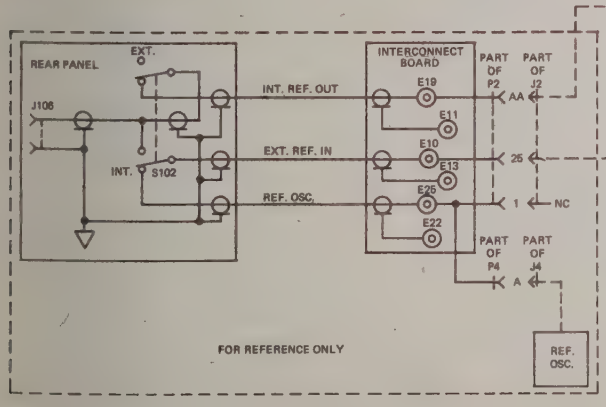

TO POWER TRANSFORMER ASSEMBLY P1
TO REMOVE ASSEMBLY REMOVE 7 PPH 6-32 x 5/16 SCREWS (615068) AND LOCK WASHERS (617079)
REF OSC. ADJ.
Y1 TCXO
STANDARD REFERENCE OSCILLATOR 730561
USE WITH STANDARD REF OSC.
W2 ADDED TO 406146 ONLY
OPTION 060 730578
REMOVE R76 AND REPLACE WITH JUMPER W5
GND
OUTPUT
+5V
REGULATOR IN
+28V REGULATED
+12V OR +18V
OPTION 200 REFERENCE OSCILLATOR Y101 (TCRO) MOUNTED ON REAR PANEL
28 VOLT REGULATOR MOUNTED IN PLACE OF STANDARD OSCILLATOR ON READOUT BOARD.
408130
TO INTERCONNECT BOARD ASSEMBLY P4
715145E
406145A/146A

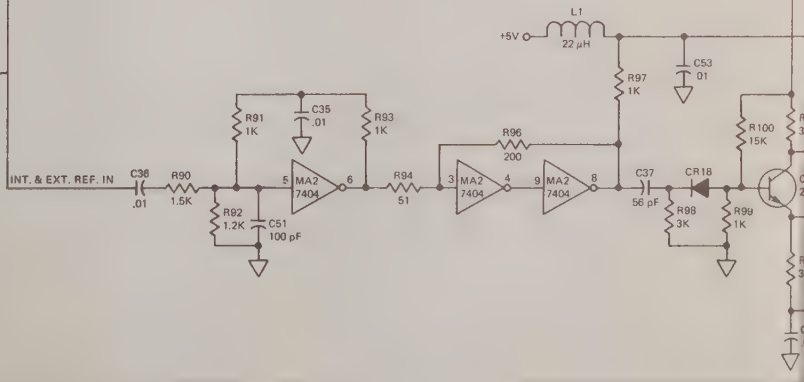
Figure 6.5 - Layout, Readout Board






REMOTE RESET
R61 2.4K
R60 100
RESET SWITCH
S2-B
R62 2.4K
MF4 7400
RESET R.S. FLIP FLOP
MC6 7400
MD5 7402
C27 .01
R66 1K
R67 1.5K
MD6 7404
C28 .001
R72 1K
R73 1.5K
STORAGE
To
CR37
CR39
R68 12K
-18V
STORAGE (REF. ONLY)
STORAGE
OFF
S101
REAR PANEL
INTERCONNECT BD
FOR REFERENCE ONLY
REF PART OF P2
J2
PART OF J3
PART OF P3
-18 VOLT SWITCH
REMOTE HOLD
CR35
CR36
R74 5.1K
MD7 7400
CR38
R69 10
C29 4.7
Q9 2N4248
Q10 2N3646
R75 1K
R76 1.5K
MC6 7400
DISPLAY TIME


REAR PANEL
EXT.
J108
INT.
S102
INTERCONNECT BOARD
INT. REF. OUT
EXT. REF. IN
REF. OSC.
E19
E11
E10
E13
E25
E22
PART OF P2
PART OF J2
AA
26
1
NC
PART OF P4
PART OF J4
A
FOR REFERENCE ONLY
REF. OSC.


INT. & EXT. REF. IN
C36 .01
R90 1.5K
R91 1K
C35 .01
R93 1K
R92 1.2K
C51 100 pF
MA2 7404
R94 51
R96 200
L1 22 μH
+5V
R97 1K
C53 .01
R100 15K
C37 56 pF
CR18
R98 3K
R99 1K

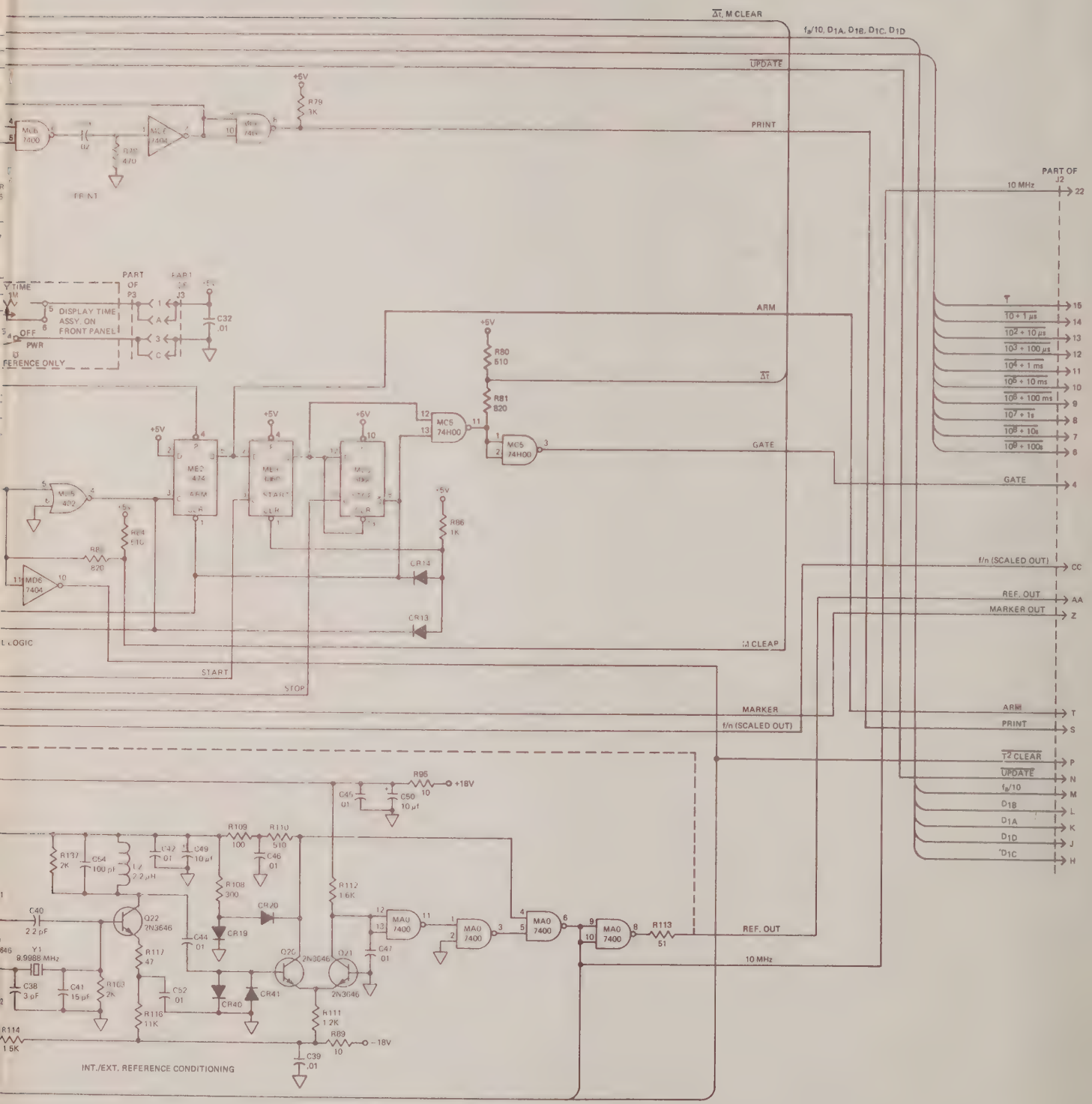
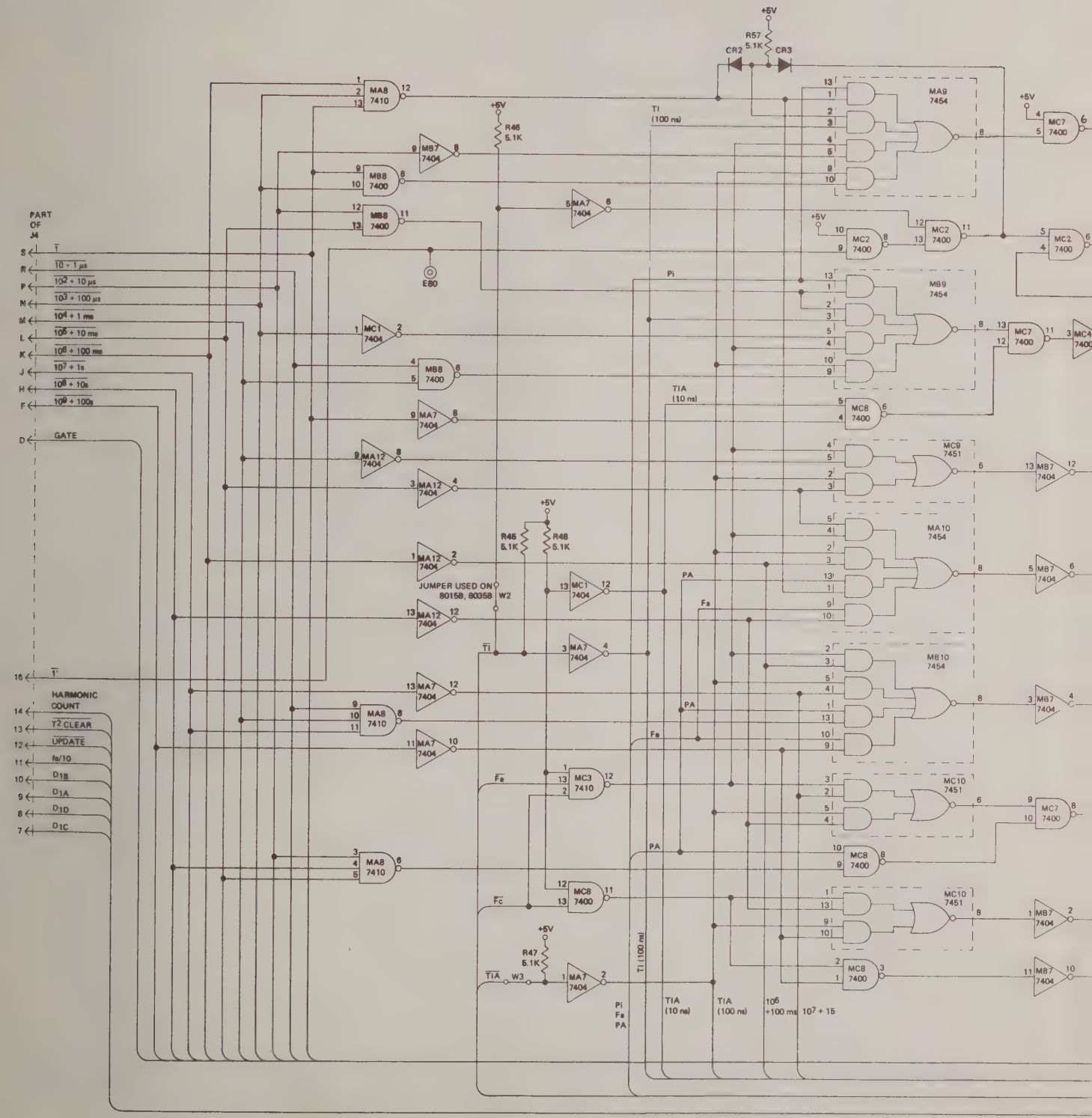


Figure 6.4 - Schematic, Switch Board TIA continued


PART OF J4
S
R
P
N
M
L
K
J
H
F
D
GATE
16
HARMONIC COUNT
14
13 T2 CLEAR
12 UPDATE
11 fe/10
10 D1B
9 D1A
8 D1D
7 D1C
+5V
R57 5.1K
CR2
CR3
R46 5.1K
R45 5.1K
R48 5.1K
R47 5.1K
E80
JUMPER USED ON 80158, 80358 W2
W3
MA8 7410
MB7 7404
MB8 7400
MB8 7400
MA7 7404
MC1 7404
MB8 7400
MA7 7404
MA12 7404
MA12 7404
MA12 7404
MA12 7404
MA7 7404
MA7 7404
MA8 7410
MA7 7404
MA8 7410
MC3 7410
MC8 7400
MA7 7404
MA9 7454
MC7 7400
MC2 7400
MC2 7400
MC2 7400
MB9 7454
MC7 7400
MC8 7400
MC9 7451
MB7 7404
MA10 7454
MB7 7404
MB10 7454
MB7 7404
MC10 7451
MC7 7400
MC8 7400
MC10 7451
MB7 7404
MC8 7400
MB7 7404
T1 (100 ns)
Pi
TIA (10 ns)
PA
Fe
T1 (100 ns)
Pi
Fe
PA
TIA (10 ns)
TIA (100 ns)
10^6 +100 ms
10^7 + 1s

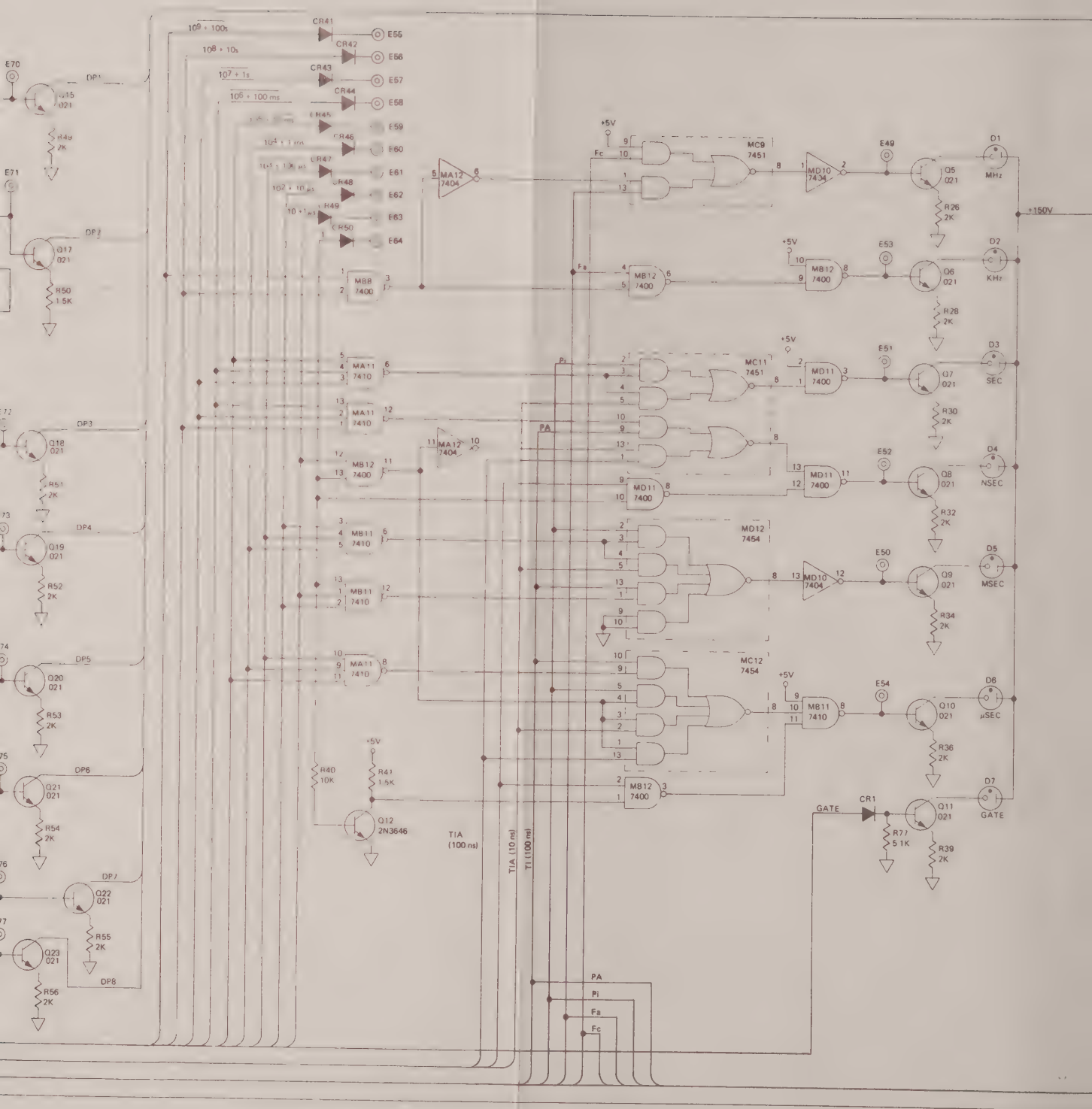
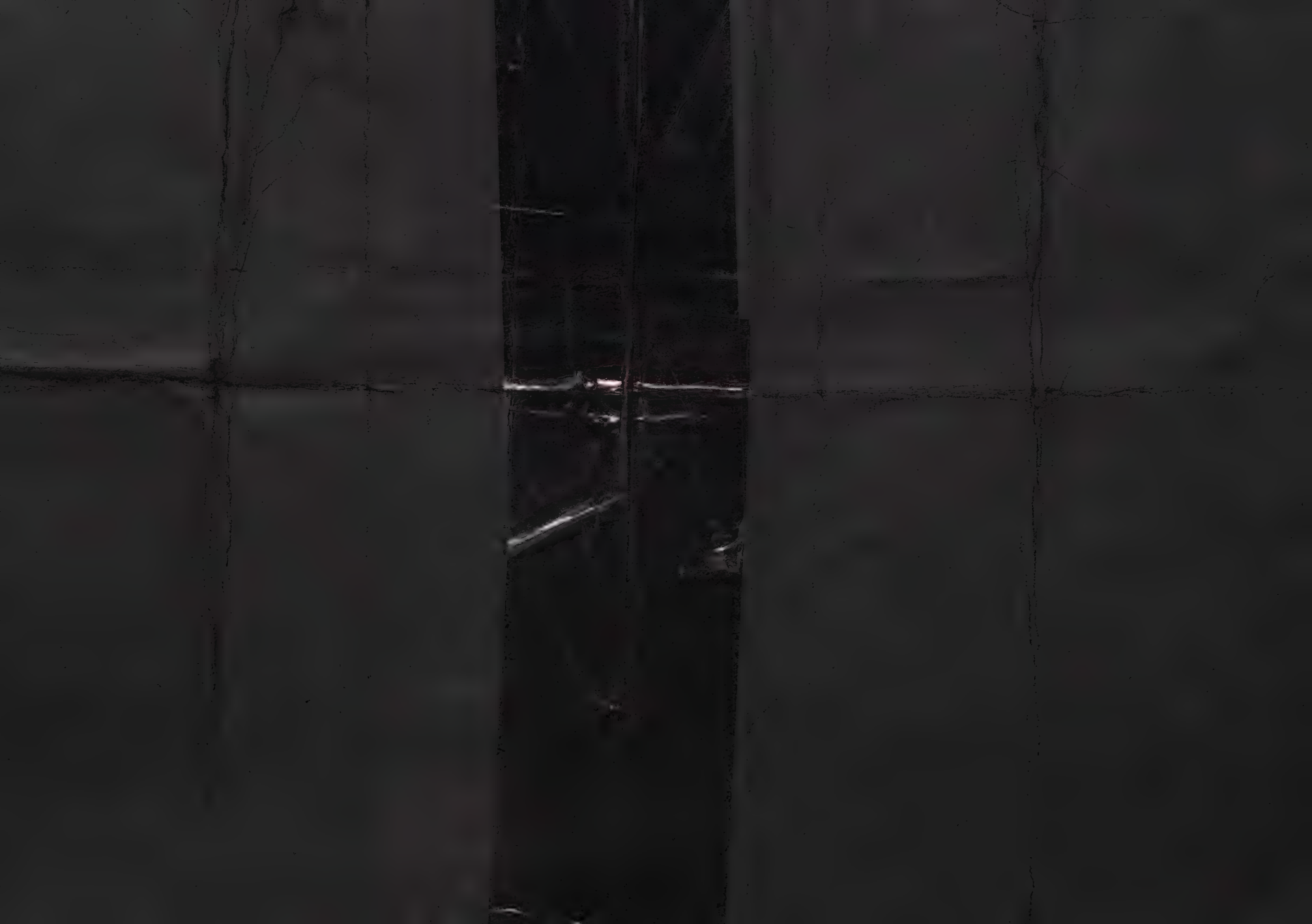
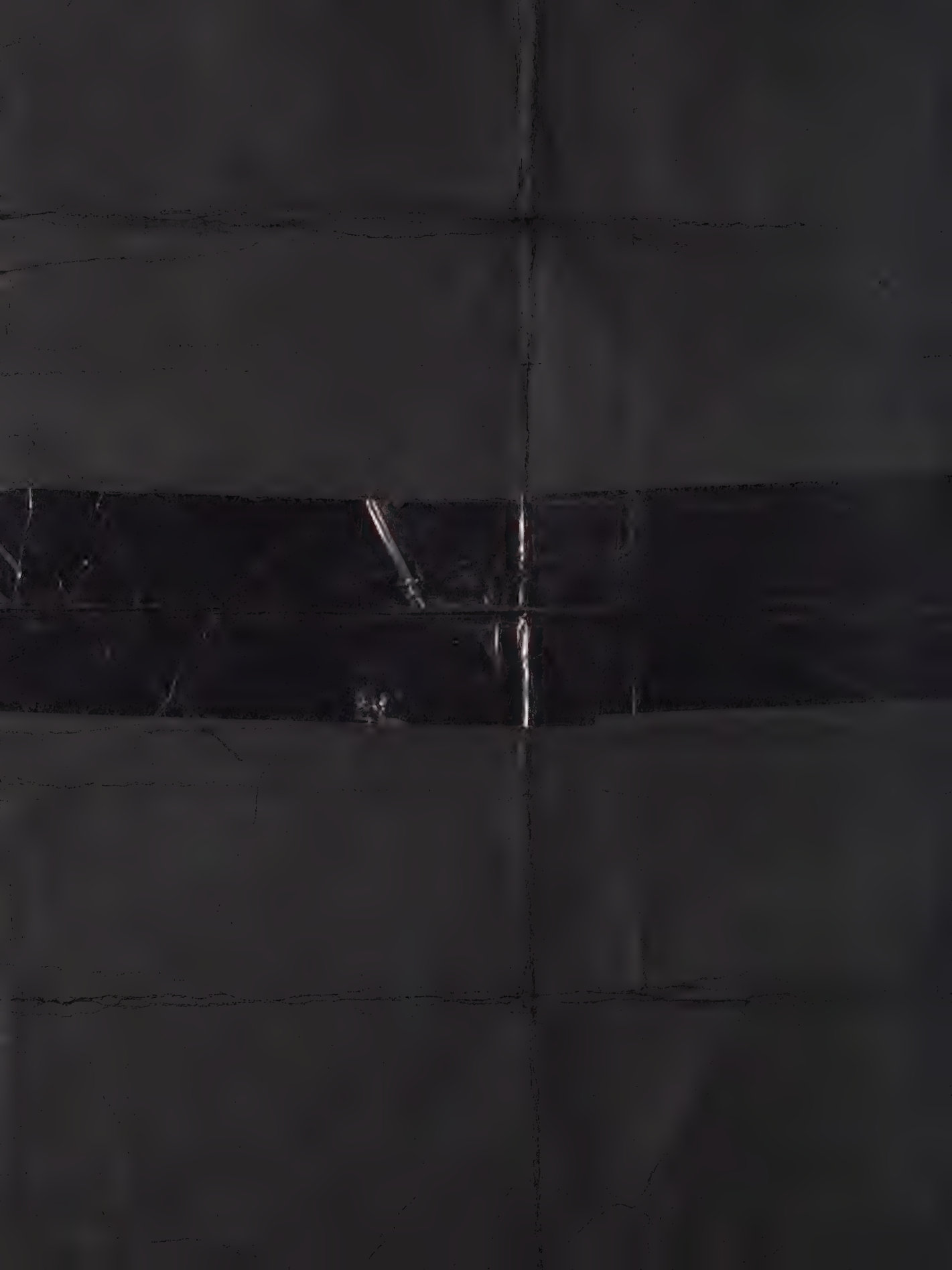
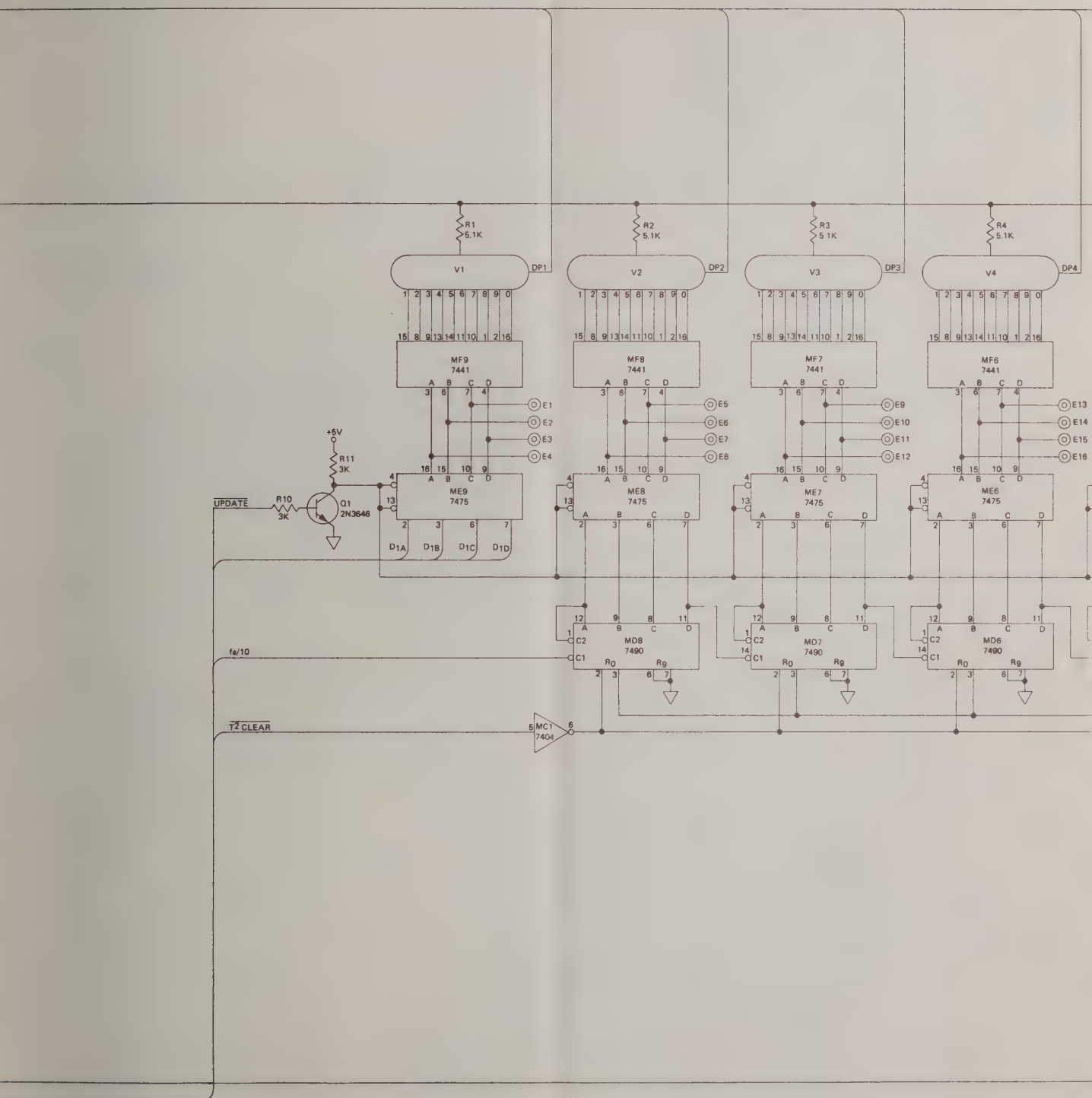
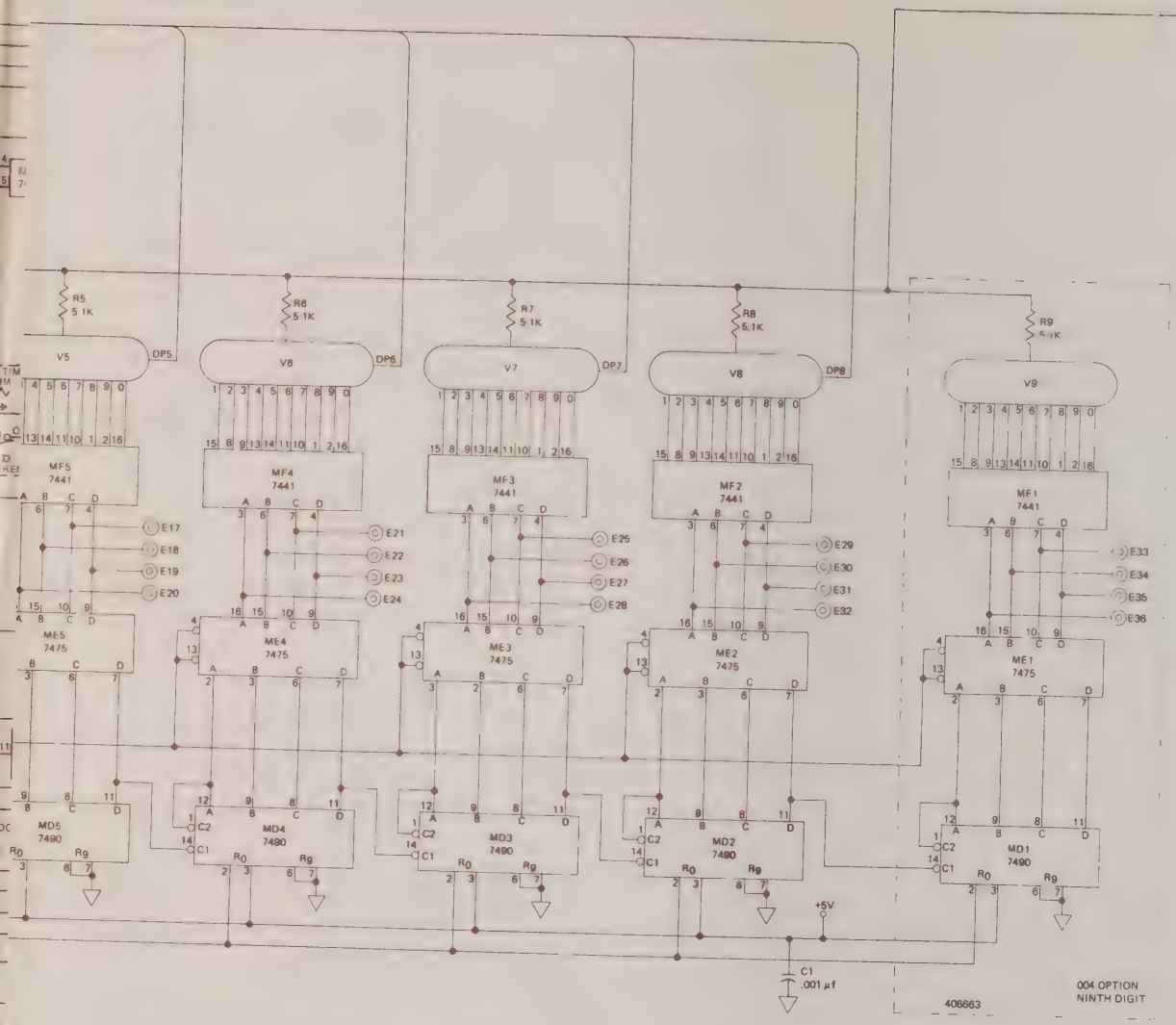


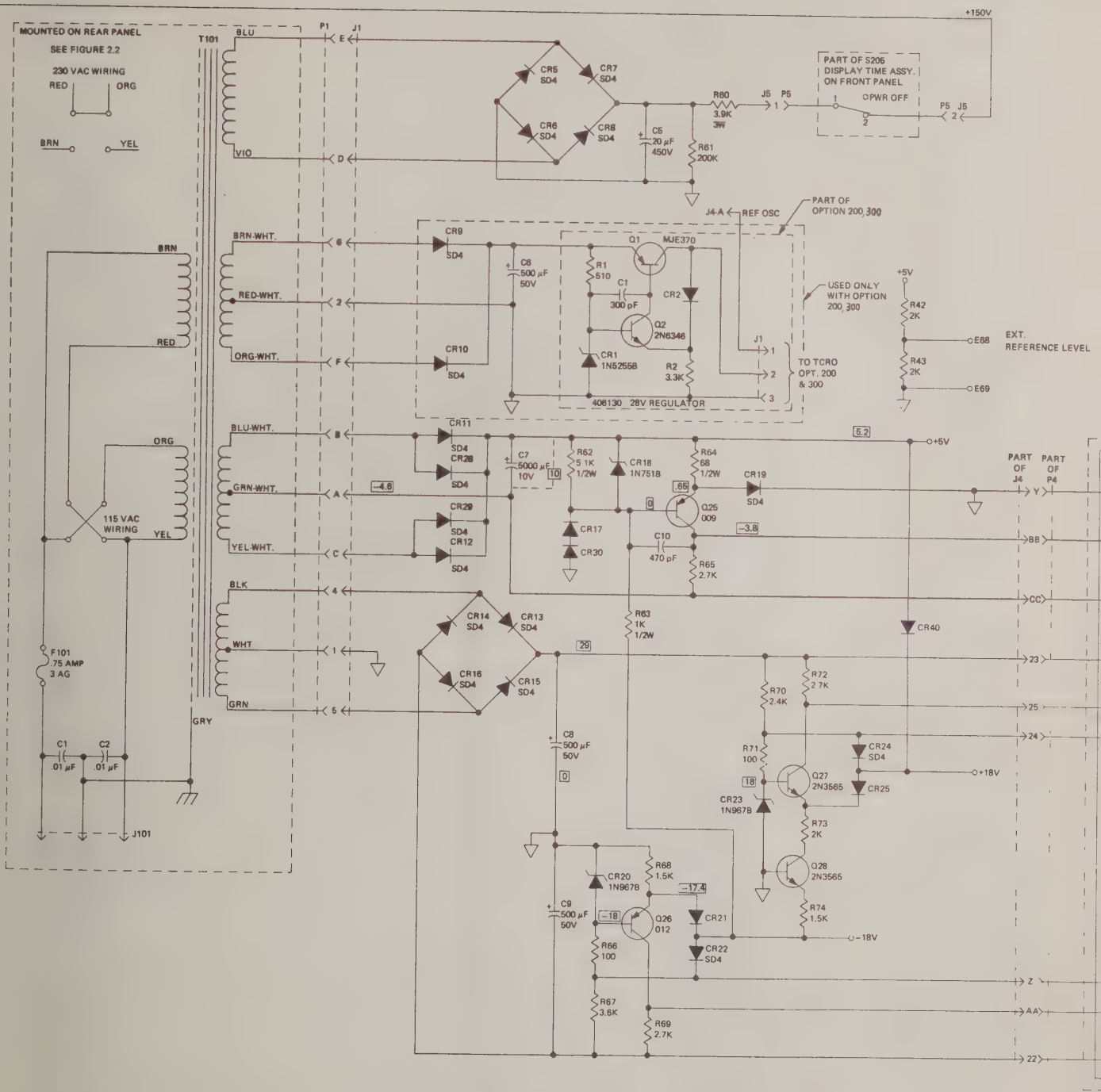
Figure 6.6 - Schematic, Readout Board






R1
5.1K
R2
5.1K
R3
5.1K
R4
5.1K
V1
V2
V3
V4
DP1
DP2
DP3
DP4
MF9
7441
MF8
7441
MF7
7441
MF6
7441
E1
E2
E3
E4
E5
E6
E7
E8
E9
E10
E11
E12
E13
E14
E15
E16
+5V
R11
3K
UPDATE
R10
3K
Q1
2N3646
ME9
7475
ME8
7475
ME7
7475
ME6
7475
D1A
D1B
D1C
D1D
MD8
7490
MD7
7490
MD6
7490
fa/10
T2 CLEAR
MC1
7404


R5 5.1K
R6 5.1K
R7 5.1K
R8 5.1K
R9 5.1K
V5
V6
V7
V8
V9
DP5
DP6
DP7
DP8
MF5 7441
MF4 7441
MF3 7441
MF2 7441
MF1 7441
E17
E18
E19
E20
E21
E22
E23
E24
E25
E26
E27
E28
E29
E30
E31
E32
E33
E34
E35
E36
ME5 7475
ME4 7475
ME3 7475
ME2 7475
ME1 7475
MD5 7490
MD4 7490
MD3 7490
MD2 7490
MD1 7490
+5V
C1 .001 µf
406663
004 OPTION NINTH DIGIT


MOUNTED ON REAR PANEL
SEE FIGURE 2.2
230 VAC WIRING
RED
ORG
BRN
YEL
T101
BLU
VIO
P1
J1
E
D
CR5 SD4
CR7 SD4
CR6 SD4
CR8 SD4
C5 20 µF 450V
R61 200K
R60 3.9K 3W
J5 P5
1
2
PART OF S205 DISPLAY TIME ASSY. ON FRONT PANEL
PWR OFF
P5 J5
+150V
J4-A
REF OSC
PART OF OPTION 200,300
BRN-WHT.
RED-WHT.
ORG-WHT.
BRN
RED
ORG
YEL
115 VAC WIRING
BLU-WHT.
GRN-WHT.
YEL-WHT.
BLK
WHT
GRN
GRY
CR9 SD4
CR10 SD4
C6 500 µF 50V
Q1 MJE370
R1 510
C1 300 pF
CR2
Q2 2N6346
CR1 1N5255B
R2 3.3K
J1
TO TCRO OPT. 200 & 300
USED ONLY WITH OPTION 200, 300
406130 28V REGULATOR
+5V
R42 2K
R43 2K
E68
E69
EXT. REFERENCE LEVEL
CR11 SD4
CR28 SD4
CR29 SD4
CR12 SD4
C7 5000 µF 10V
R62 5.1K 1/2W
CR18 1N751B
R64 68 1/2W
CR19 SD4
Q25 009
CR17
CR30
C10 470 pF
R65 2.7K
R63 1K 1/2W
CR40
PART OF J4
PART OF P4
Y
BB
CC
23
25
24
+18V
CR14 SD4
CR13 SD4
CR16 SD4
CR15 SD4
C8 500 µF 50V
R70 2.4K
R72 2.7K
R71 100
CR24 SD4
CR25
Q27 2N3565
CR23 1N967B
R73 2K
Q28 2N3565
R74 1.5K
-18V
CR20 1N967B
R68 1.5K
C9 500 µF 50V
Q26 012
CR21
CR22 SD4
R66 100
R67 3.6K
R69 2.7K
Z
AA
22
F101 .75 AMP 3 AG
C1 .01 µF
C2 .01 µF
J101

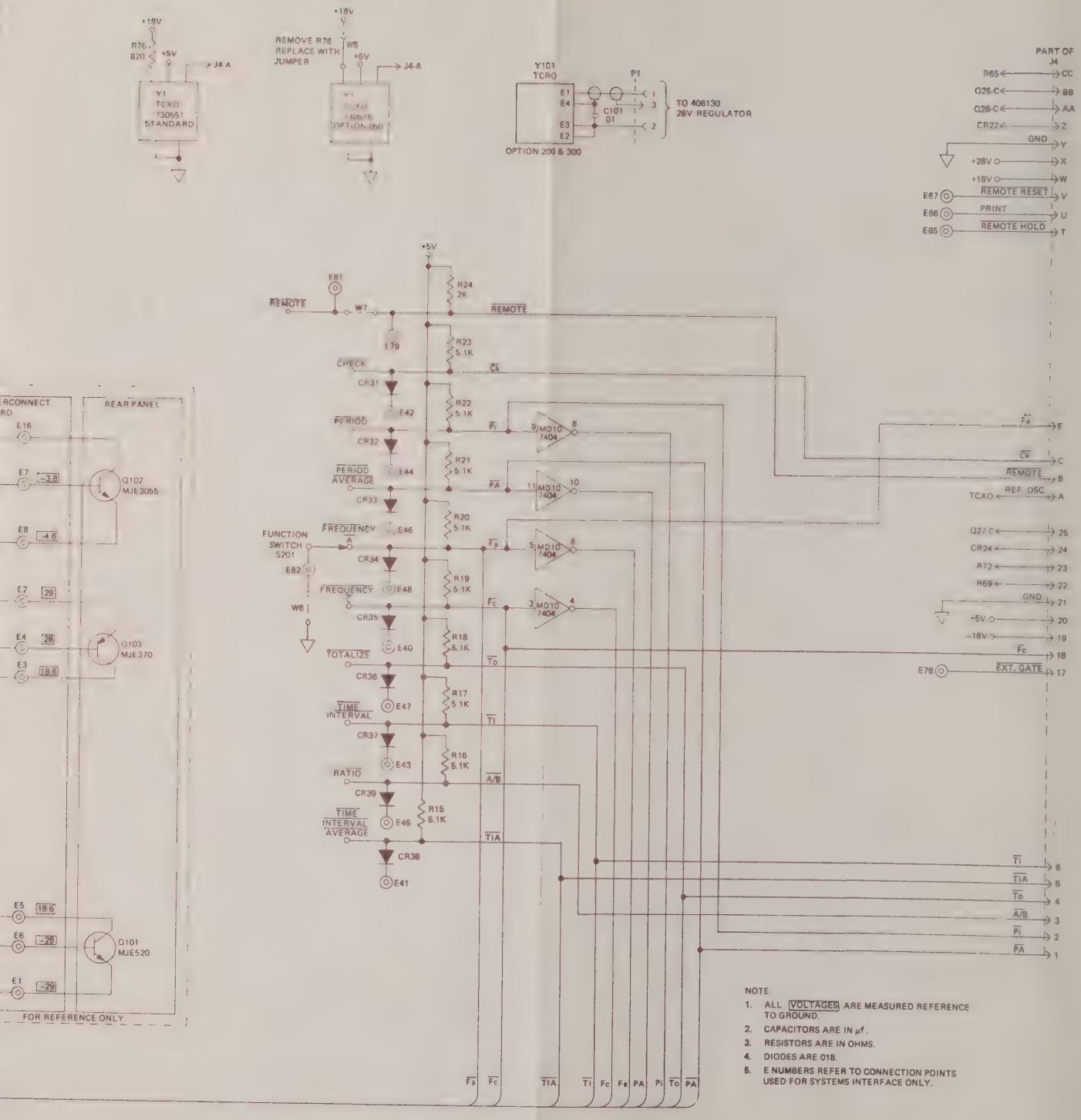
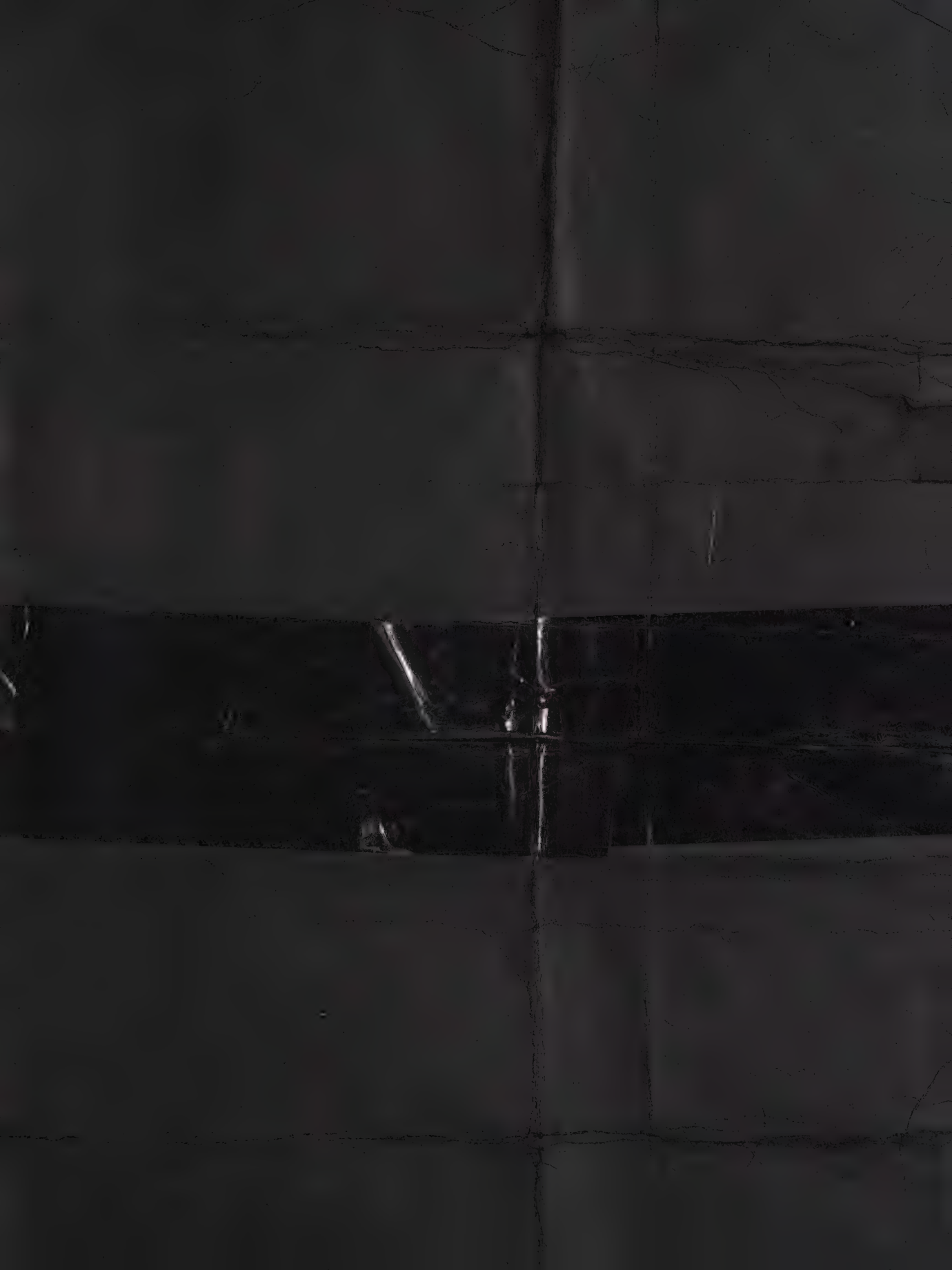


Figure 6.6 - Schematic, Readout Board continued



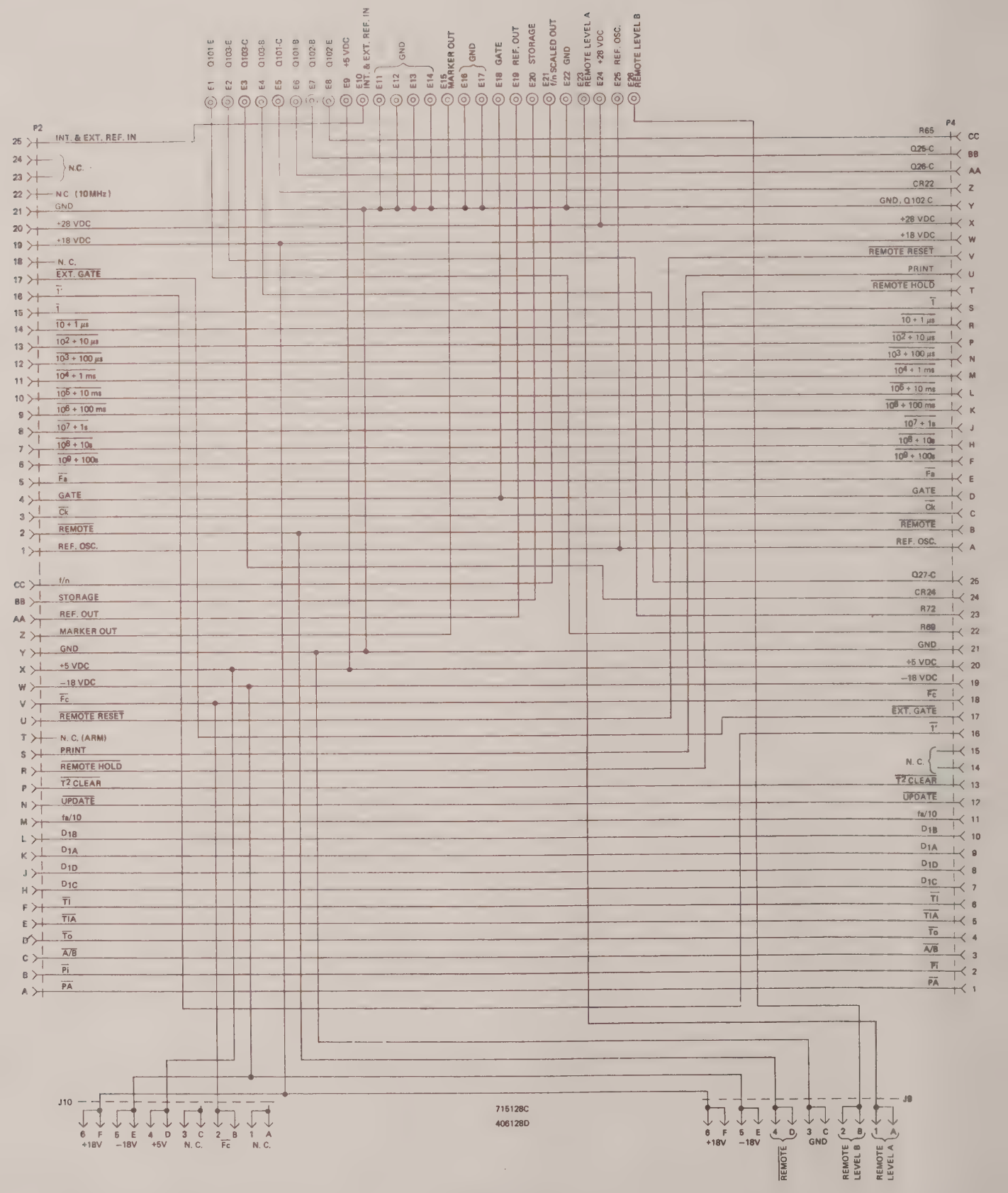
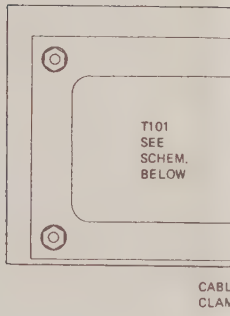
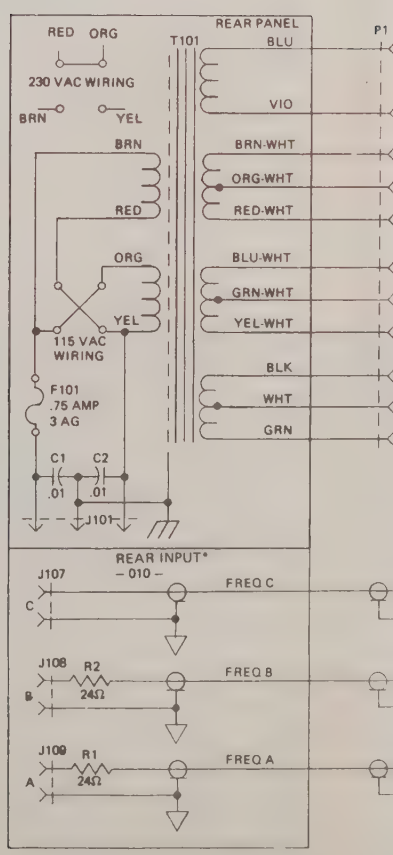


Figure 6.7 - Schematic, Interconnect Board





*INSTRUMENTS EQUIPPED WITH OPTION 200 OR 300 REFER TO PAGE 6-15 TO SHOW LAYOUT OF OPTION 010 REAR INPUT

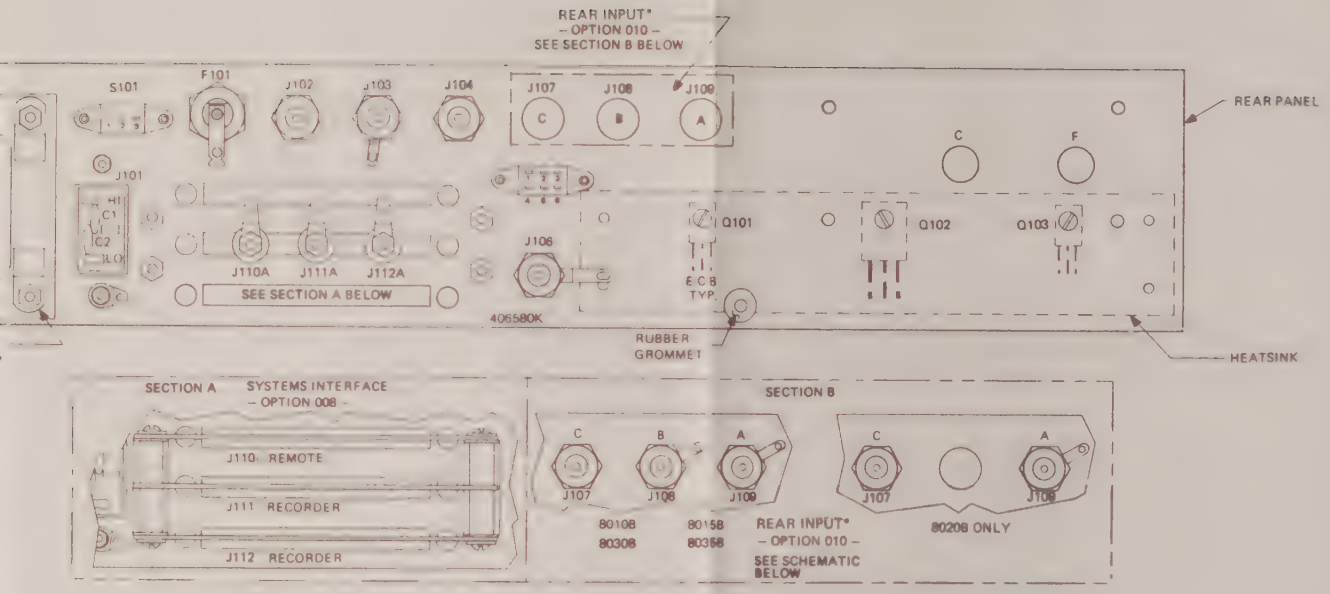


Figure 6.8 - Layout, Rear Panel

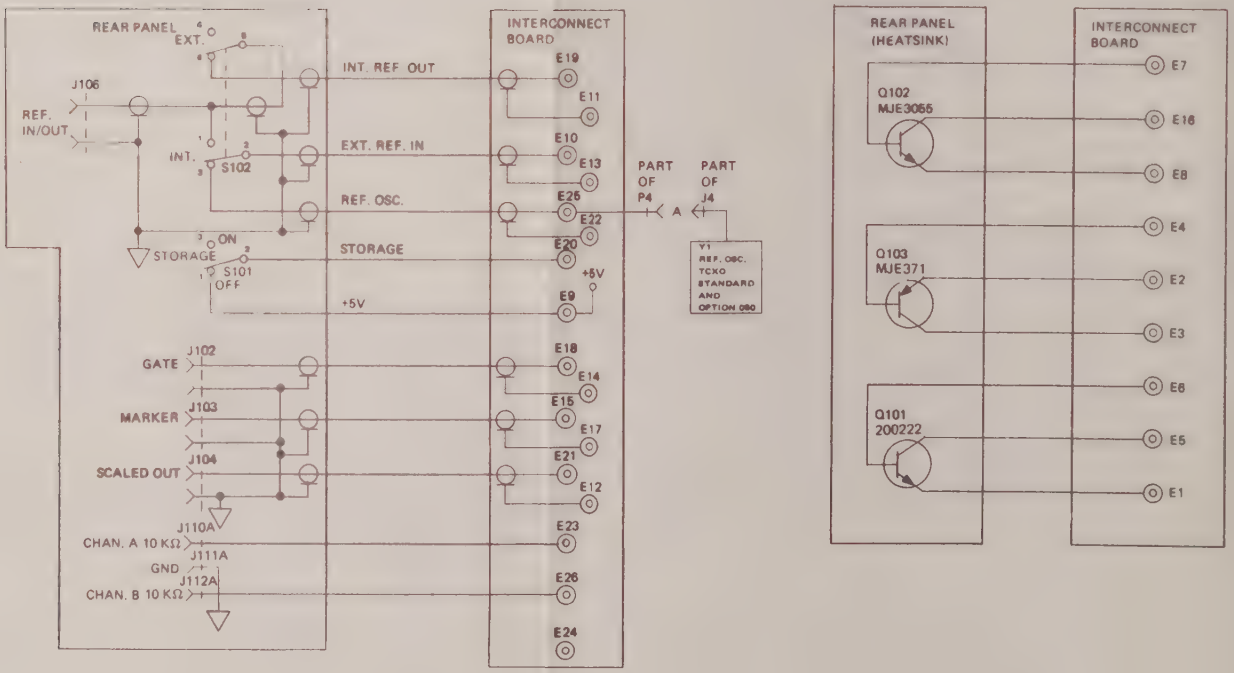
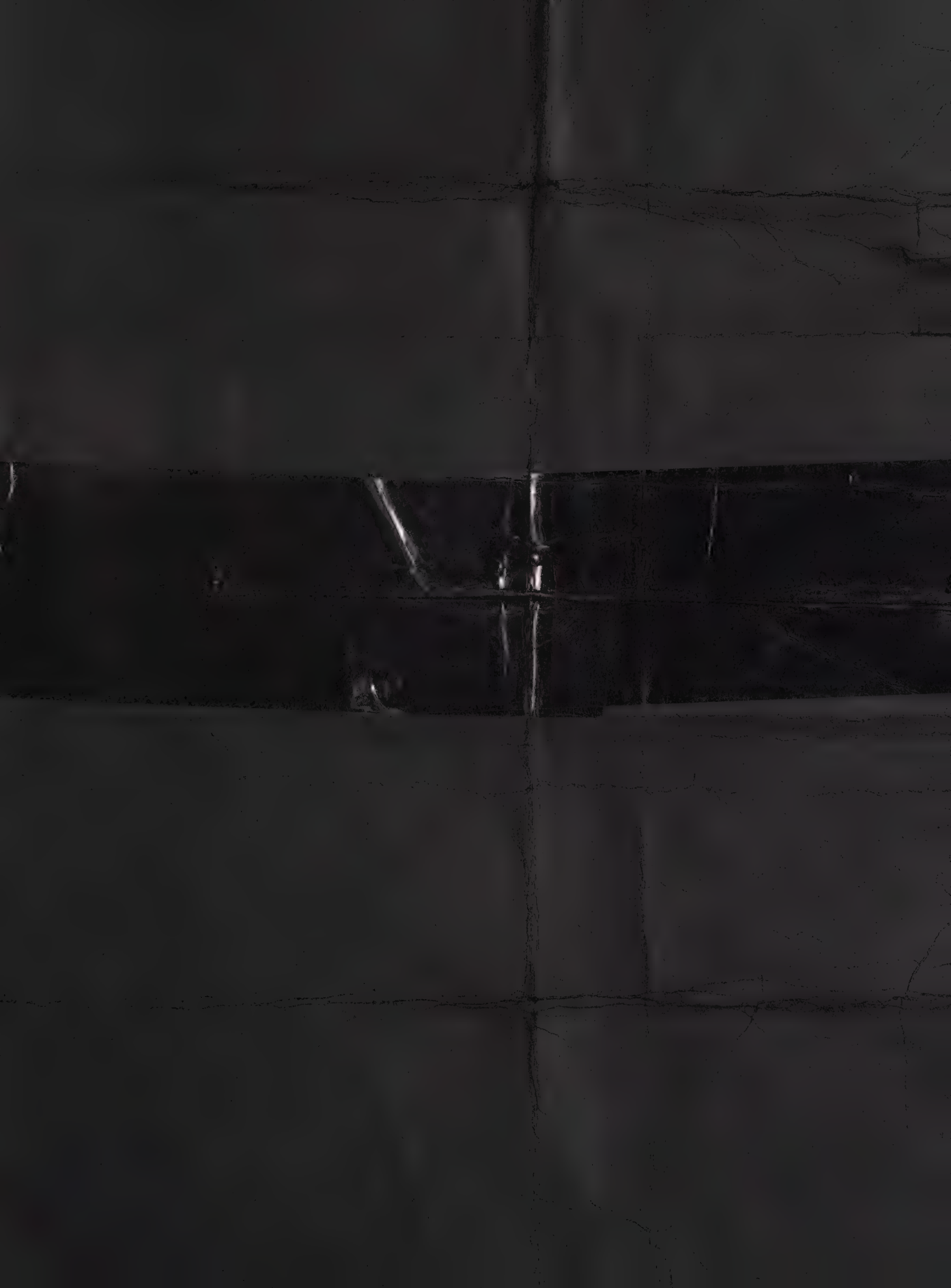
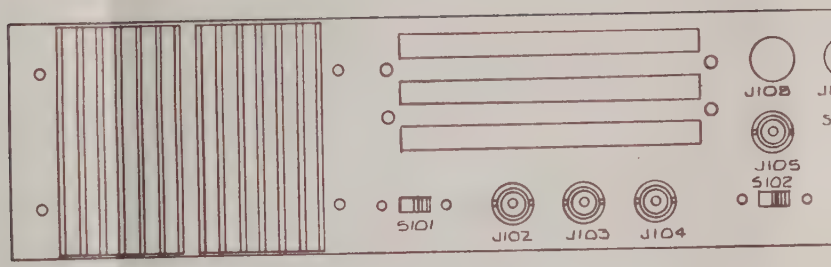
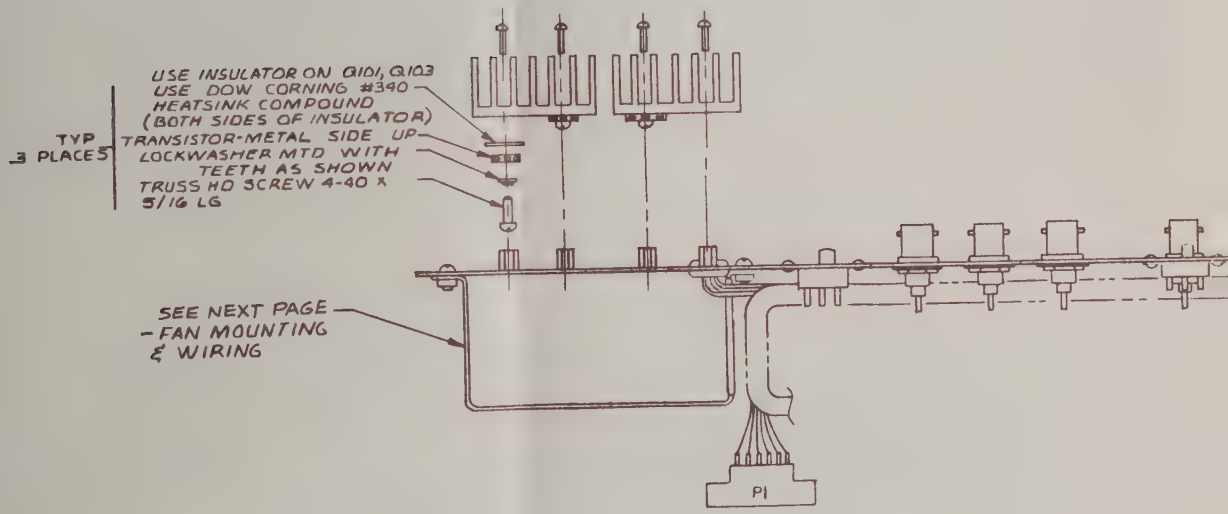
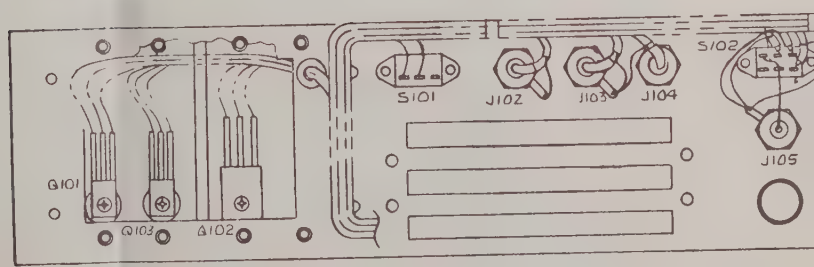


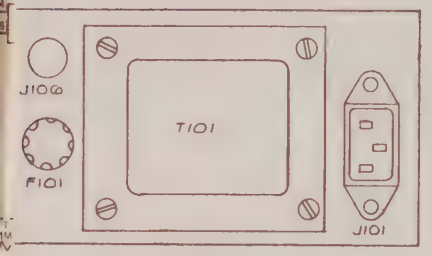
Figure 6.9 - Schematic, Rear Panel

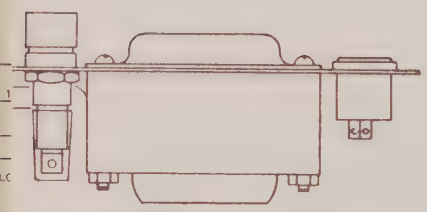


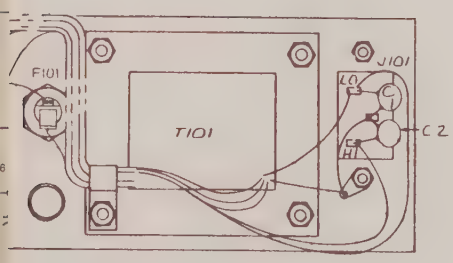

J108
J105
S102
S101
J102
J103
J104


USE INSULATOR ON Q101, Q103
USE DOW CORNING #340
HEATSINK COMPOUND
(BOTH SIDES OF INSULATOR)
TYP
3 PLACES
TRANSISTOR-METAL SIDE UP
LOCKWASHER MTD WITH
TEETH AS SHOWN
TRUSS HD SCREW 4-40 X
5/16 LG
SEE NEXT PAGE
- FAN MOUNTING
& WIRING
P1


S101
J102
J103
J104
S102
J105
Q101
Q103
Q102







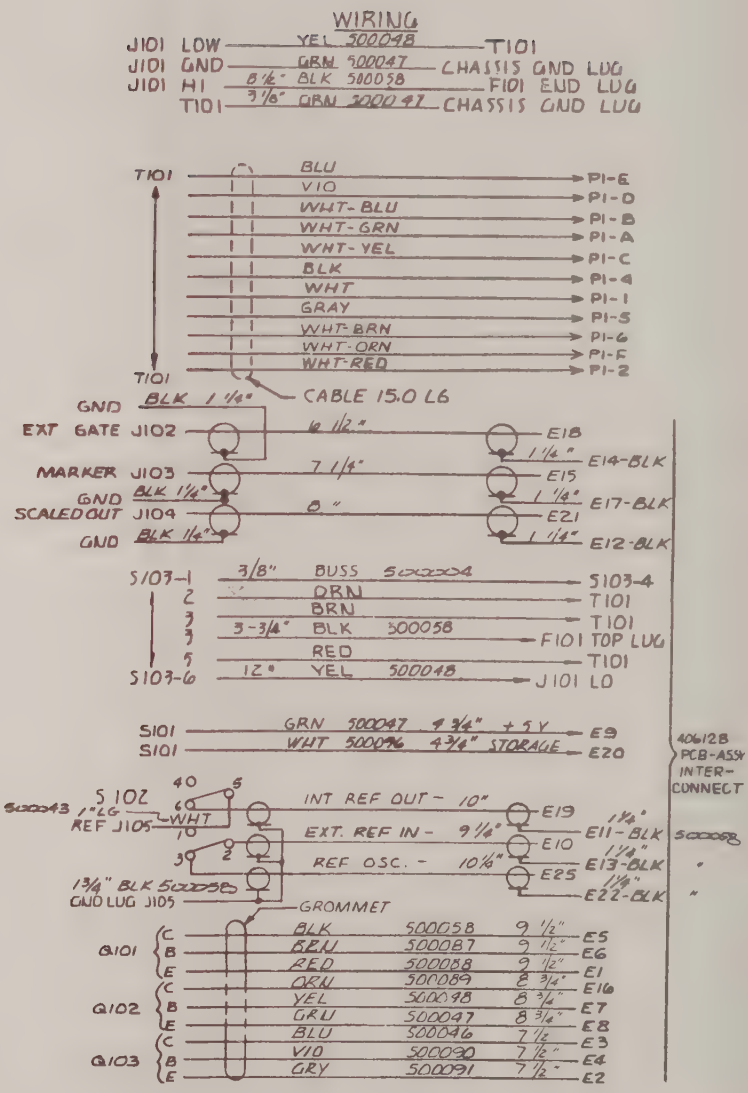
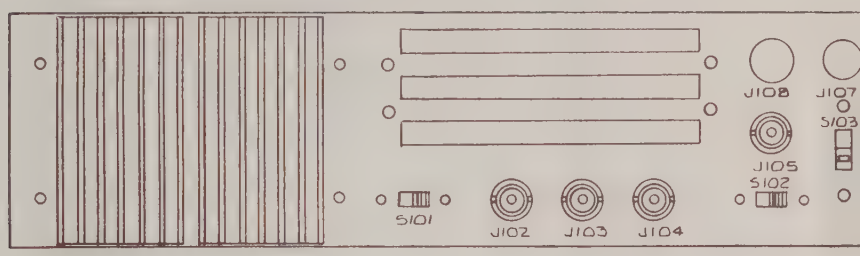
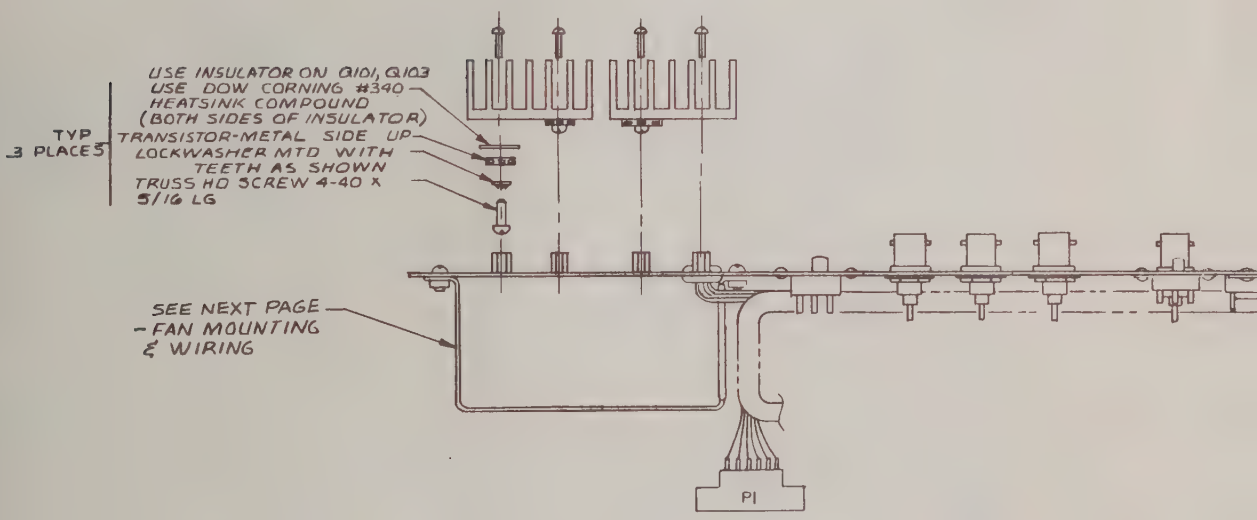
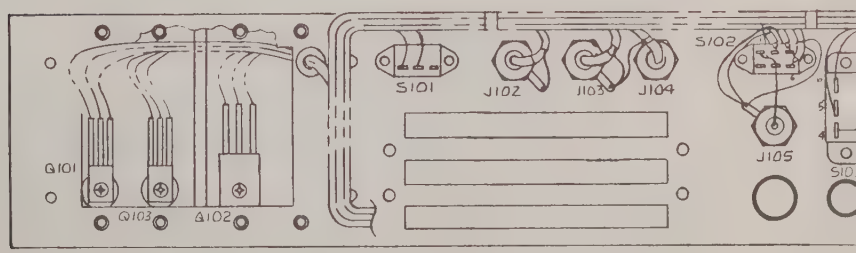
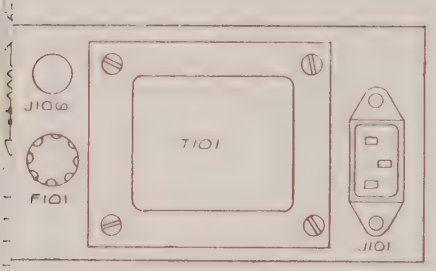

WIRING
J101 LOW YEL 500048 T101
J101 GND GRN 500047 CHASSIS GND LUG
J101 HI 8½" BLK 500058 F101 END LUG
T101 3⅛" ORN 500047 CHASSIS GND LUG
T101
BLU P1-E
VIO P1-D
WHT-BLU P1-B
WHT-GRN P1-A
WHT-YEL P1-C
BLK P1-4
WHT P1-1
GRAY P1-5
WHT-BRN P1-6
WHT-ORN P1-F
WHT-RED P1-2
CABLE 15.0 L6
GND BLK 1 ¼"
EXT GATE J102 6 ½" E18
1 ¼" E14-BLK
MARKER J103 7 ¼" E15
GND BLK 1¼"
SCALED OUT J104 8 " E21
1 ¼" E17-BLK
GND BLK 1¼" 1 ¼" E12-BLK
S107-1 3/8" BUSS 500004 S103-4
2 ORN T101
3 BRN T101
3-3/4" BLK 500058 F101 TOP LUG
5 RED T101
S107-6 12" YEL 500048 J101 LO
S101 GRN 500047 9 ¾" +5V E9
S101 WHT 500096 4 ¾" STORAGE E20
406128 PCB-ASSY INTER-CONNECT
S102
500043 1"LG
REF J105 WHT
INT REF OUT - 10" E19
EXT. REF IN - 9⅛" E10
REF OSC. - 10⅛" E25
1¾" BLK 500058
GND LUG J105
GROMMET
Q101 BLK 500058 9 ½" E5
BRN 500087 9 ½" E6
RED 500088 9 ½" E1
Q102 ORN 500089 8 ¾" E16
YEL 500098 8 ¾" E7
GRN 500097 8 ¾" E8
Q103 BLU 500046 7 ½" E3
VIO 500090 7 ½" E4
GRY 500091 7 ½" E2

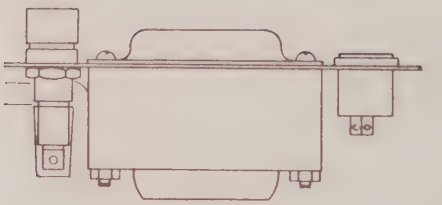
Figure 6.10 - Layout, Rear Panel (Part of Option 200 & 300)

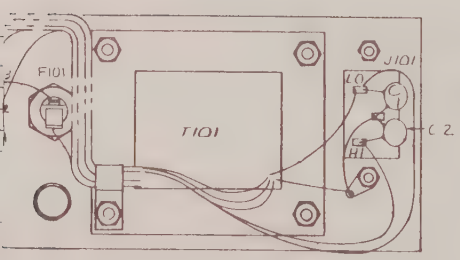

J108
J107
S103
J105
S102
S101
J102
J103
J104


USE INSULATOR ON Q101, Q103
USE DOW CORNING #340
HEATSINK COMPOUND
(BOTH SIDES OF INSULATOR)
TYP
3 PLACES
TRANSISTOR-METAL SIDE UP
LOCKWASHER MTD WITH
TEETH AS SHOWN
TRUSS HD SCREW 4-40 X
5/16 LG
SEE NEXT PAGE
- FAN MOUNTING
& WIRING
P1


S102
S101
J102
J103
J104
J105
Q101
Q103
Q102







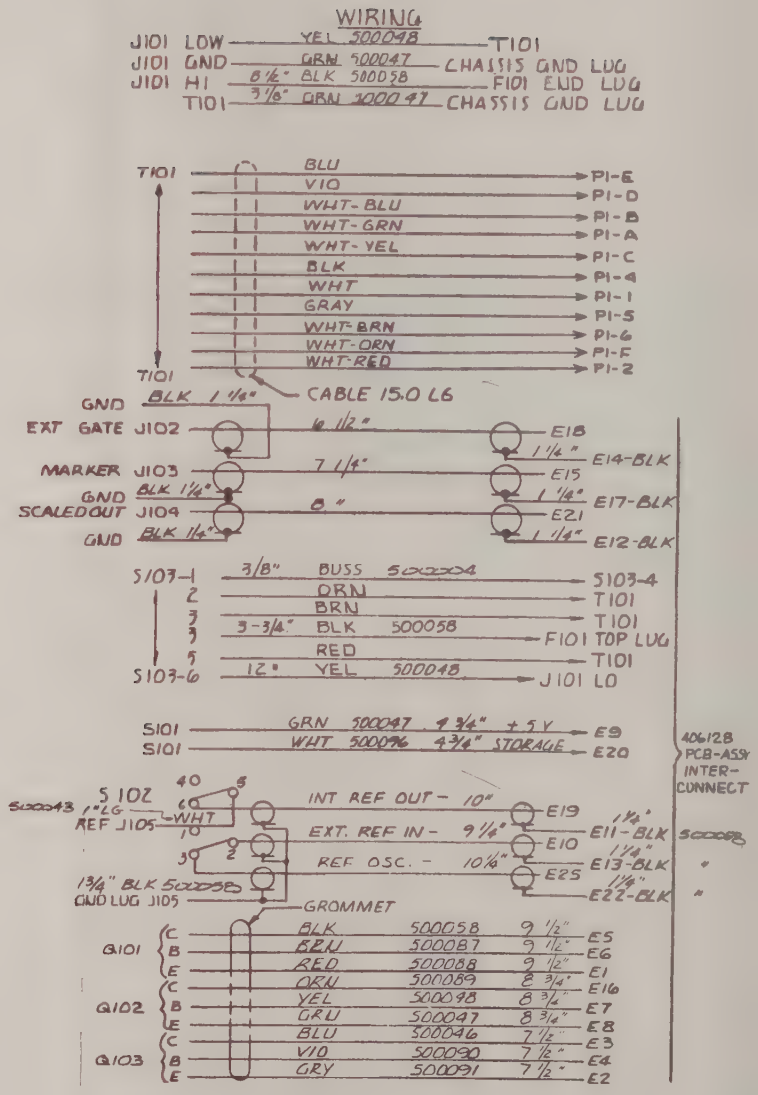
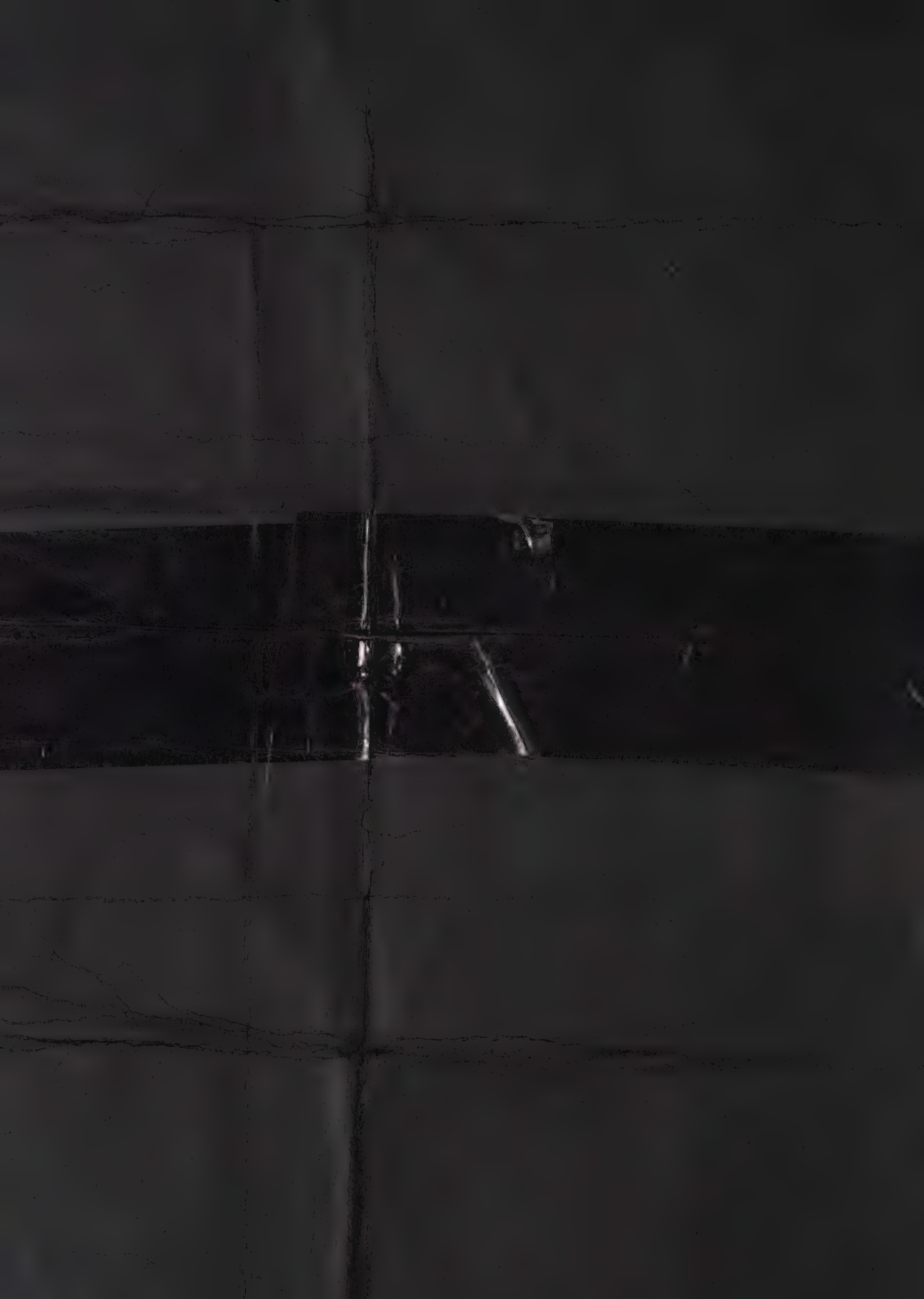
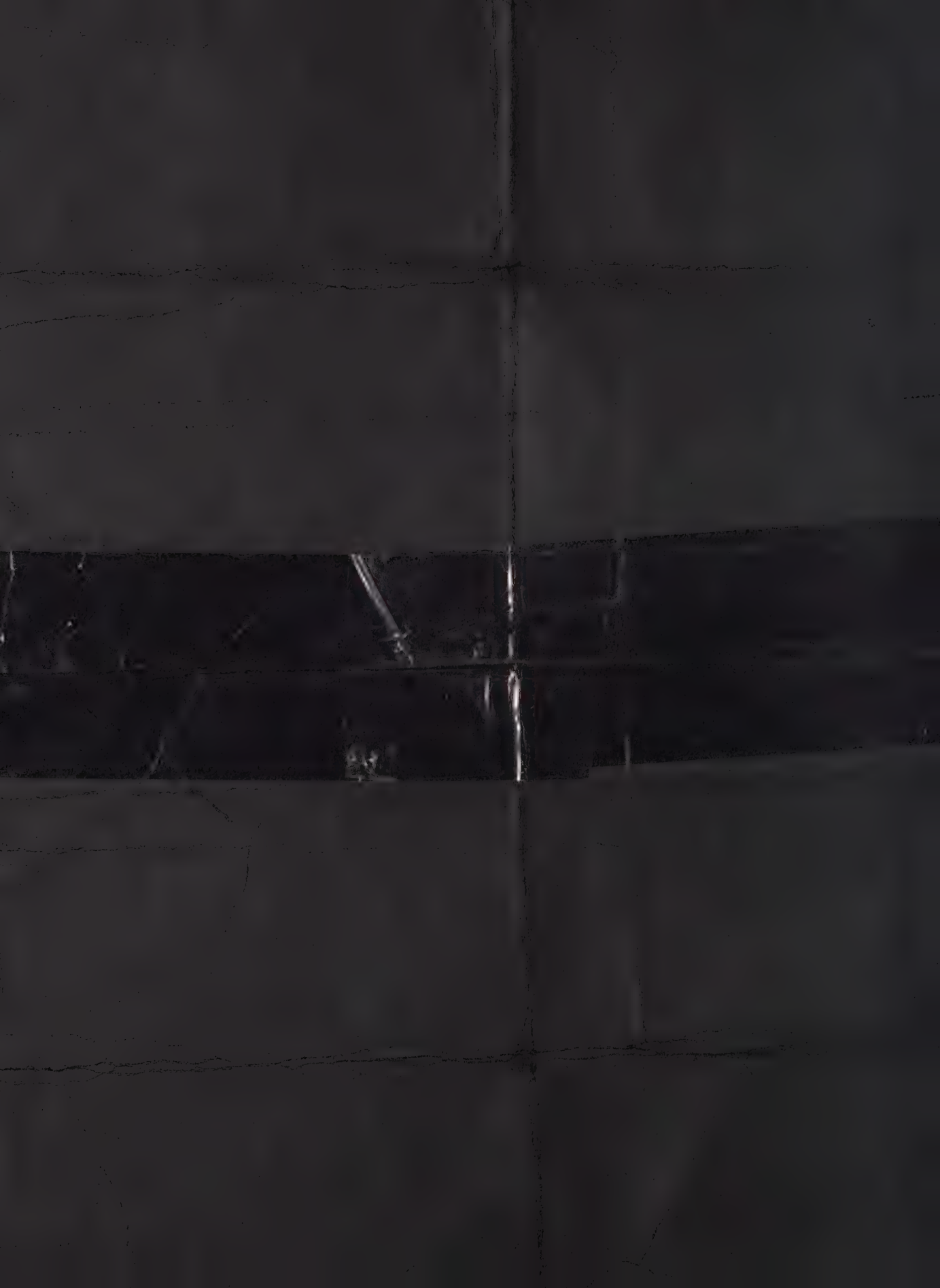
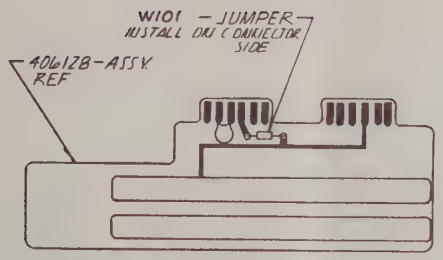
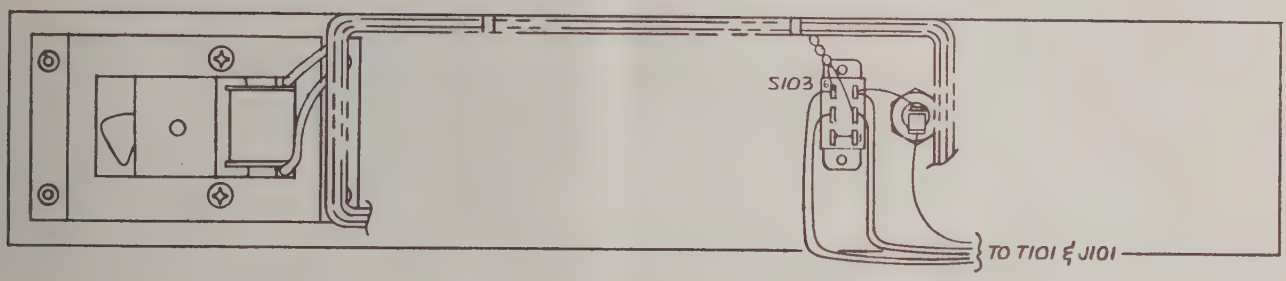

WIRING
J101 LOW — YEL 500048 — T101
J101 GND — GRN 500047 — CHASSIS GND LUG
J101 HI — 8 1/2" BLK 500058 — F101 END LUG
T101 — 3 1/8" GRN 500047 — CHASSIS GND LUG
T101
BLU — P1-E
VIO — P1-D
WHT-BLU — P1-B
WHT-GRN — P1-A
WHT-YEL — P1-C
BLK — P1-4
WHT — P1-1
GRAY — P1-5
WHT-BRN — P1-6
WHT-ORN — P1-F
WHT-RED — P1-2
CABLE 15.0 L6
GND BLK 1 1/4"
EXT GATE J102 — 6 1/2" — E18
MARKER J103 — 7 1/4" — E15 — 1 1/4" — E14-BLK
GND BLK 1 1/4"
SCALED OUT J104 — 0" — E21 — 1 1/4" — E17-BLK
GND BLK 1 1/4" — E12-BLK
S103-1 — 3/8" BUSS 500004 — S103-4
2 — ORN — T101
3 — BRN — T101
3 — 3-3/4" BLK 500058 — F101 TOP LUG
5 — RED — T101
S103-6 — 12" YEL 500048 — J101 LO
S101 — GRN 500047 — 9 3/4" + 5 V — E9
S101 — WHT 500096 — 4 3/4" STORAGE — E20
406128 PCB-ASSY INTER-CONNECT
S102
500043 1" LG WHT
REF J105
INT REF OUT - 10" — E19
EXT. REF IN - 9 1/4" — E10 — 1 1/4" — E11-BLK 500058
REF OSC. - 10 1/4" — E25 — 1 1/4" — E13-BLK "
1 3/4" BLK 500058 GND LUG J105 — 1 1/4" — E22-BLK "
GROMMET
Q101 C BLK 500058 9 1/2" E5
Q101 B BRN 500087 9 1/2" E6
Q101 E RED 500088 9 1/2" E1
Q102 C ORN 500089 8 3/4" E16
Q102 B YEL 500098 8 3/4" E7
Q102 E GRN 500047 8 3/4" E8
Q103 C BLU 500046 7 1/2" E3
Q103 B VIO 500090 7 1/2" E4
Q103 E GRY 500091 7 1/2" E2

Figure 6.14 - Layout, Rear Panel (Part of Option 200 & 300)

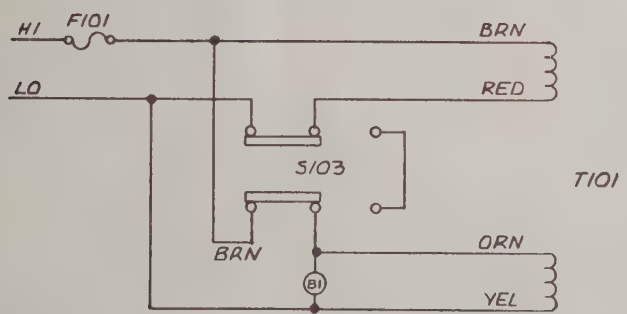




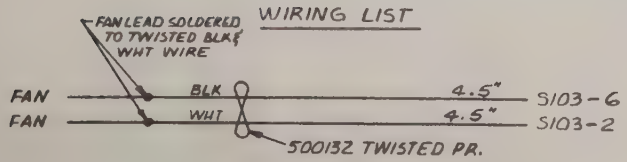




FAN MOUNTING



WIRING DIAGRAM FOR FAN & P5



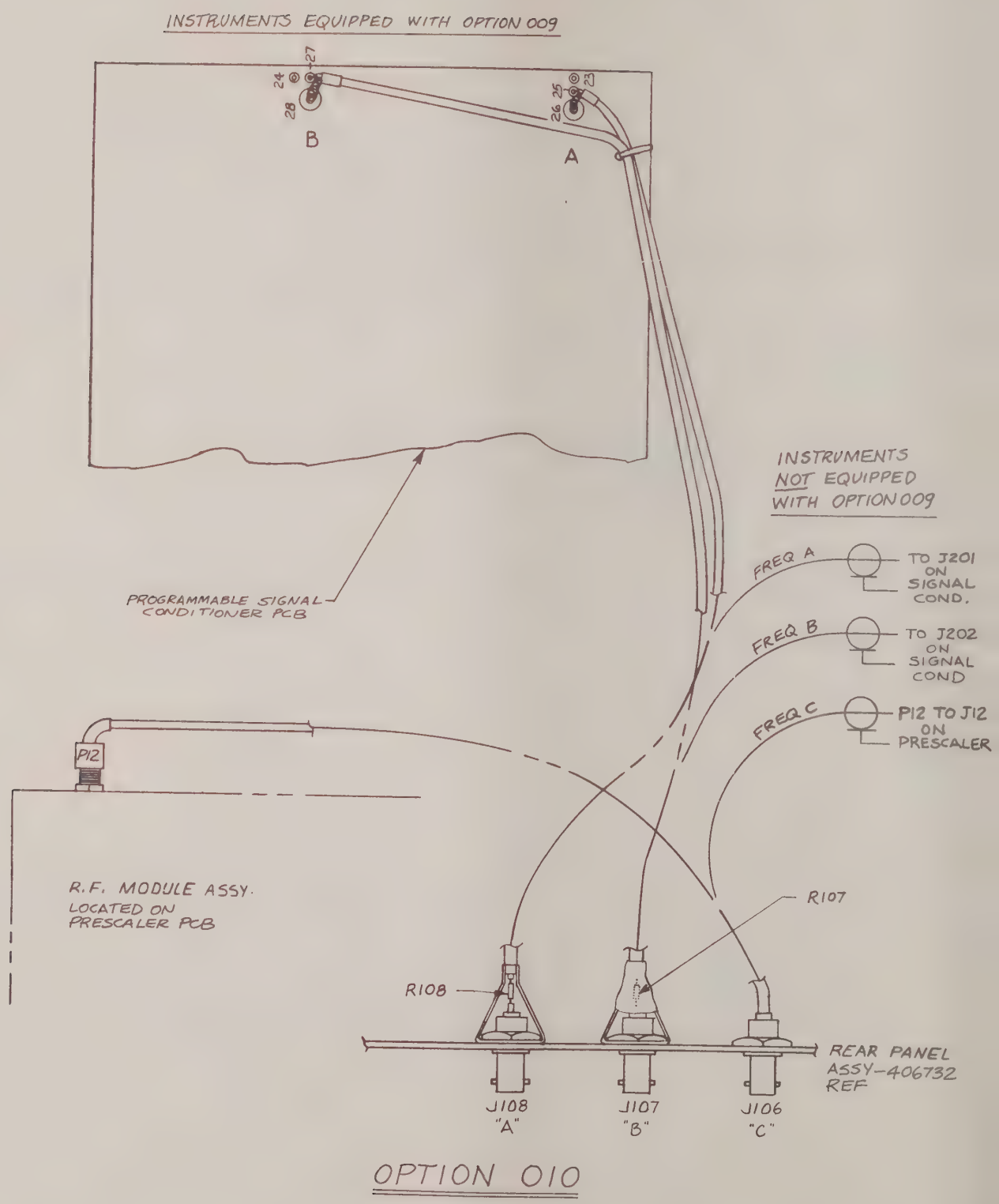


Figure 6.14 - Layout, Rear Panel (Part of Option 200 & 300) continued

SECTION 7 PARTS LIST

7.1 This section contains lists of replaceable parts arranged in the order of the following subassemblies:

	Page
List of Suppliers	7-1/7-2
Signal Conditioning Attenuator	7-3
Signal Conditioning, PCB	7-4
Switch Board	7-8
Readout Board	7-14
Rear Panel	7-19
Rear Panel, Part of Option 200 & 300	7-20
Display Time Control	7-21
Interconnect Board	7-22
9th Digit Readout, Option 004	7-23
Systems Interface, Option 008	7-24
Rear Input, Option 010	7-25
TCXO Oscillator, Option 050	7-26
TCRO Oscillator, Option 200 & 300	7-27
28V Regulator, Part of Option 200 & 300	7-28

7.2 Manufacturers are identified by FSC numbers listed in table 7.2, "List of Suppliers". The code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1, H4-2, and their supplements.

7.3 Certain parts having 21793 (Dana) listed in the "FSC" column are specially-selected semiconductors. For some of these, standard commercial parts will serve as satisfactory replacements. These Dana parts are identified in table 7.1 along with the commercial equivalent.

Table 7.1

Semiconductor Type:		Equivalent:
007	Diode	Fairchild FD300
009	Transistor	Motorola 2N2905
014	Transistor	Motorola 2N3501
018	Diode	Texas Instruments 1N4448
021	Transistor	MPS A42

Table 7.2 - List of Suppliers

FSC	NAME	FSC	NAME
01121	ALLEN BRADLEY CO. MILWAUKEE, WISCONSIN	02660	AMPHENOL CORP. BROADVIEW, ILLINOIS
01295	TEXAS INSTRUMENTS, INC. (Components Group) DALLAS, TEXAS	04713	MOTOROLA, INC. (Semiconductor Products Division) PHOENIX, ARIZONA
02114	FERROXCUBE CORP. SAUGERTIES, NEW YORK	05397	UNION CARBIDE CORP. (Materials Systems Division) CLEVELAND, OHIO

Table 7.2 - List of Suppliers continued

FSC	NAME
05624	BARBER & COLMAN CO. ROCKFORD, ILLINOIS
11237	CTS KEENE, INC. PASO ROBLES, CALIFORNIA
21551	C-F ELECTRONICS, INC. VAN NUYS, CALIFORNIA
21793	DANA LABORATORIES, INC. IRVINE, CALIFORNIA
23095	AZTEC ELECTRONICS, INC. ANAHEIM, CALIFORNIA
27264	MOLEX PRODUCTS CO. DOWNERS GROVE, ILLINOIS
28520	HEYCO (Division of Heyman Mfg. Co.) KENILWORTH, NEW JERSEY
32767	GRIFFITH PLASTIC PRODUCT CO. (Nobex Division) BURLINGAME, CALIFORNIA
56289	SPRAGUE ELECTRIC CO. (Pacific Division) LOS ANGELES, CALIFORNIA
71471	AEROVOX CORP. (Cinema Plant) MONCKS CORNER, SOUTH CAROLINA
71590	CENTRALAB ELECTRONICS (Division of Globe-Union, Inc.) MILWAUKEE, WISCONSIN

FSC	NAME
71785	TRW ELECTRONIC COMPONENTS (Cinch Division) ELK GROVE VILLAGE, ILLINOIS
72982	ERIE TECHNOLOGICAL PRODUCTS, INC. ERIE, PENNSYLVANIA
73138	BECKMAN INSTRUMENTS, INC. (Helipot Division) FULLERTON, CALIFORNIA
73445	AMPEREX ELECTRONIC CORP. HICKSVILLE, LONG ISLAND, NEW YORK
74276	SIGNALITE, INC. NEPTUNE, NEW JERSEY
75915	LITTELFUSE, INC. DES PLAINES, ILLINOIS
79727	C-W INDUSTRIES WARMINSTER, PENNSYLVANIA
80131	ELECTRONIC INDUSTRIES ASSOC. WASHINGTON, D.C.
81349	MILITARY SPECIFICATION
82389	SWITCHCRAFT, INC. CHICAGO, ILLINOIS
98291	SEALECTRO CORP. MAMARONECK, NEW YORK
99800	AMERICAN PRECISION INDUSTRIES, INC. (Delevan Division) EAST AURORA, NEW YORK

406654 – Assy., ATTENUATOR, SIGNAL COND (DUAL CHANNEL)

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
B1	920563	BEADS, SHIELDING			56-59065-4B		02114	56-59065-4B
B1A	920563	BEADS, SHIELDING			56-59065-4B		02114	56-59065-4B
B2	920563	BEADS, SHIELDING			56-59065-4B		02114	56-59065-4B
B2A	920563	BEADS, SHIELDING			56-59065-4B		02114	56-59065-4B
B3	920563	BEADS, SHIELDING			56-59065-4B		02114	56-59065-4B
B4	920563	BEADS, SHIELDING			56-59065-4B		02114	56-59065-4B
C1	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	5GAS-S10
C1A	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	5GAS-S10
C2	101182	CAP	CERAM	47 PFD	500 V	10%	71471	TCD-DI-2(N750)
C2A	101182	CAP	CERAM	47 PFD	500 V	10%	71471	TCD-DI-2(N750)
C3	100009	CAP	CERAM	5 PFD	500 V	10%	71471	TCDI-1(N750)
C3A	100009	CAP	CERAM	5 PFD	500 V	10%	71471	TCDI-1(N750)
C4	100016	CAP	CERAM	27 PFD	N750	10%	71590	DD270
C4A	100016	CAP	CERAM	27 PFD	N750	10%	71590	DD270
C5	100009	CAP	CERAM	5 PFD	500 V	10%	71471	TCDI-1(N750)
C5A	100009	CAP	CERAM	5 PFD	500 V	10%	71471	TCDI-1(N750)
C6	101182	CAP	CERAM	47 PFD	500 V	10%	71471	TCD-DI-2(N750)
C6A	101182	CAP	CERAM	47 PFD	500 V	10%	71471	TCD-DI-2(N750)
J201	600567	CONN	RECPTLE		31-236-1050		02660	31-236-1050
J202	600567	CONN	RECPTLE		31-236-1050		02660	31-236-1050
R1	010609	RES	METAL	909 K	T-0	1%	81349	RN60D9093F
R1A	010609	RES	METAL	909 K	T-0	1%	81349	RN60D9093F
R2	010680	RES	METAL	90.9 K		1%	81349	RN55C9092F
R2A	010680	RES	METAL	90.9 K		1%	81349	RN55C9092F
R3	010529	RES	METAL	10 K	T-0	1%	81349	RN55D1002F
R3A	010529	RES	METAL	10 K	T-0	1%	81349	RN55D1002F
R4	000104	RES	CARBON	100 K		5% 1/4W	81349	RC07GF104J
R4A	000104	RES	CARBON	100 K		5% 1/4W	81349	RC07GF104J
S202A	600603	SWITCH	ATTENUATOR				11237	
S203A	600603	SWITCH	ATTENUATOR				11237	
S206	600613	SWITCH	SLIDE, SPDT				79727	GF-124
S207	600613	SWITCH	SLIDE, SPDT				79727	GF-124
S208	600613	SWITCH	SLIDE, SPDT				79727	GF-124
S209	600613	SWITCH	SLIDE, SPDT				79727	GF-124
S210	600613	SWITCH	SLIDE, SPDT				79727	GF-124

406147 – Assy., PCB, SIGNAL COND (DUAL CHANNEL)

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
B1	920563	BEADS, SHIELDING			56-59065-4B		02114	56-59065-4B
B1A	920563	BEADS, SHIELDING			56-59065-4B		02114	56-59065-4B
B2	920563	BEADS, SHIELDING			56-59065-4B		02114	56-59065-4B
B2A	920563	BEADS, SHIELDING			56-59065-4B		02114	56-59065-4B
B3	920563	BEADS, SHIELDING			56-59065-4B		02114	56-59065-4B
B3A	920563	BEADS, SHIELDING			56-59065-4B		02114	56-59065-4B
C1	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C1A	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C2	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C2A	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C3	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C3A	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C4	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C4A	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C6	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C6A	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C7	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C7A	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C8	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C8A	130103	CAP	CERAM	10000 PFD	25 V	20%	72982	9ACF-W5R103M
C9	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C9A	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C10	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C10A	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C11	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C11A	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C12	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C12A	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C13A	100041	CAP	CERAM	25 PFD	1000 V	5%	56289	10TCCQ25
CR1	220031	DIODE	SILICO	ZENER	1/4M3.3AZ5		04713	1/4M3.3AZ5
CR1A	220031	DIODE	SILICO	ZENER	1/4M3.3AZ5		04713	1/4M3.3AZ5
CR2	220031	DIODE	SILICO	ZENER	1/4M3.3AZ5		04713	1/4M3.3AZ5
CR2A	220031	DIODE	SILICO	ZENER	1/4M3.3AZ5		04713	1/4M3.3AZ5
CR3	211236	DIODE	SILICO		007		21793	211236
CR3A	211236	DIODE	SILICO		007		21793	211236
CR4	211236	DIODE	SILICO		007		21793	211236
CR4A	211236	DIODE	SILICO		007		21793	211236
CR5	220019	DIODE	SILICO	ZENER	1N752A		81349	1N752A
CR5A	220019	DIODE	SILICO	ZENER	1N752A		81349	1N752A
CR6	211083	DIODE	SILICO		018		21793	211083
CR6A	211083	DIODE	SILICO		018		21793	211083
CR7	211083	DIODE	SILICO		018		21793	211083

406147 – Assy., PCB, SIGNAL COND (DUAL CHANNEL) *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
CR7A	211083	DIODE SILICO 018	21793	211083
CR8	220004	DIODE SILICO ZENER 1N961B	81349	1N961B
CR8A	220004	DIODE SILICO ZENER 1N961B	81349	1N961B
J6	600573	CONN RF 50-051-0000	98291	50-051-0000
J7	600573	CONN RF 50-051-0000	98291	50-051-0000
L1	310068	CHOKE 1 UH 10%	99800	1537-12
L1A	310068	CHOKE 1 UH 10%	99800	1537-12
L2	310068	CHOKE 1 UH 10%	99800	1537-12
L2A	310068	CHOKE 1 UH 10%	99800	1537-12
L3A	310108	INDUCTOR 180 NH 10%	99800	1025-02
L4A	310108	INDUCTOR 180 NH 10%	99800	1025-02
Q1	200189	TRANS MATCHED PAIR WITH Q10 TIS58	21793	200189
Q1A	200189	TRANS MATCHED PAIR WITH Q10A TIS58	21793	200189
Q2	200186	TRANS MATCHED PAIR WITH Q9	21793	200186
Q2A	200186	TRANS MATCHED PAIR WITH Q9A	21793	200186
Q3	200195	TRANS SILICO NPN 2N5179	81349	2N5179
Q3A	200186	TRANS MATCHED PAIR WITH Q7A	21793	200186
Q4	200186	TRANS MATCHED PAIR WITH Q8	21793	200186
Q4A	200186	TRANS MATCHED PAIR WITH Q8A	21793	200186
Q5	200195	TRANS SILICO NPN 2N5179	81349	2N5179
Q5A	200151	TRANS SILICO 2N5179	81349	2N5179
Q6	200195	TRANS SILICO NPN 2N5179	81349	2N5179
Q6A	200151	TRANS SILICO 2N5179	81349	2N5179
Q7	200195	TRANS SILICO NPN 2N5179	81349	2N5179
Q7A	200186	TRANS MATCHED PAIR WITH Q3A	21793	200186
Q8	200186	TRANS MATCHED PAIR WITH Q4 2N5179	21793	200186
Q8A	200186	TRANS MATCHED PAIR WITH Q4A	21793	200186
Q9	200186	TRANS MATCHED PAIR WITH Q2	21793	200186
Q9A	200186	TRANS MATCHED PAIR WITH Q2A	21793	200186
Q10	200189	TRANS MATCHED PAIR WITH Q1 TIS58	21793	200189
Q10A	200189	TRANS MATCHED PAIR WITH Q1A TIS58	21793	200189
Q11	200043	TRANS	21793	200043
Q11A	200043	TRANS	21793	200043
Q12	200043	TRANS	21793	200043
Q12A	200043	TRANS	21793	200043
Q13	200037	TRANS SILICO NPN 2N3646	80131	2N3646
Q13A	200037	TRANS SILICO NPN 2N3646	80131	2N3646
Q14	200037	TRANS SILICO NPN 2N3646	80131	2N3646
Q14A	200037	TRANS SILICO NPN 2N3646	80131	2N3646
P9	600593	CONN 6 PIN 250-0630170	71785	250-0630170

406147 – Assy., PCB, SIGNAL COND (DUAL CHANNEL) *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R1	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R1A	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R2	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R2A	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R3	010720	RES	METAL	9.09 K	T-2	.25%	81349	RN55C9091C
R3A	010720	RES	METAL	9.09 K	T-2	.25%	81349	RN55C9091C
R4	000751	RES	CARBON	750 OHM		5% 1/4W	81349	RC07GF751J
R4A	000751	RES	CARBON	750 OHM		5% 1/4W	81349	RC07GF751J
R5	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R5A	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R6	010705	RES	METAL	4.53 K	T-0	1%	81349	RN55D4531F
R6A	010705	RES	METAL	4.53 K	T-0	1%	81349	RN55D4531F
R7	000910	RES	CARBON	91 OHM		5% 1/4W	81349	RC07GF910J
R7A	000910	RES	CARBON	91 OHM		5% 1/4W	81349	RC07GF910J
R8	000470	RES	CARBON	47 OHM		5% 1/4W	81349	RC07GF470J
R8A	000470	RES	CARBON	47 OHM		5% 1/4W	81349	RC07GF470J
R9A	000152	RES	CARBON	1.5 K		5% 1/4W	81349	RC07GF152J
R10	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R10A	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R11	000430	RES	CARBON	43 OHM		5% 1/4W	81349	RC07GF430J
R11A	000430	RES	CARBON	43 OHM		5% 1/4W	81349	RC07GF430J
R12	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R12A	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R13	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R13A	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R14	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R14A	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R15A	000152	RES	CARBON	1.5 K		5% 1/4W	81349	RC07GF152J
R16	001758	RES	CARBON	330 OHM		5% 1W	81349	RC32GF331J
R16A	001758	RES	CARBON	330 OHM		5% 1W	81349	RC32GF331J
R17	040114	POT	CERMET	50 OHM		10%	73138	62PR50
R17A	040114	POT	CERMET	50 OHM		10%	73138	62PR50
R18	000910	RES	CARBON	91 OHM		5% 1/4W	81349	RC07GF910J
R18A	000910	RES	CARBON	91 OHM		5% 1/4W	81349	RC07GF910J
R19	000470	RES	CARBON	47 OHM		5% 1/4W	81349	RC07GF470J
R19A	000470	RES	CARBON	47 OHM		5% 1/4W	81349	RC07GF470J
R20	040115	POT	CERMET	500 OHM		10%	73138	62PR500
R20A	040115	POT	CERMET	500 OHM		10%	73138	62PR500
R21	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R21A	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R22	010705	RES	METAL	4.53 K	T-0	1%	81349	RN55D4531F
R22A	010705	RES	METAL	4.53 K	T-0	1%	81349	RN55D4531F
R23	000751	RES	CARBON	750 OHM		5% 1/4W	81349	RC07GF751J
R23A	000751	RES	CARBON	750 OHM		5% 1/4W	81349	RC07GF751J
R24	010720	RES	METAL	9.09 K	T-2	.25%	81349	RN55C

406147 – Assy., PCB, SIGNAL COND (DUAL CHANNEL) *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R24A	010720	RES	METAL	9.09 K	T-2	.25%	81349	RN55C9091C
R25	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R25A	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R26	010704	RES	METAL	1 K	T-0	1%	81349	RN55D1001F
R26A	010704	RES	METAL	1 K	T-0	1%	81349	RN55D1001F
R27	010630	RES	METAL	9.09 K		1%	81349	RN55D9091F
R27A	010630	RES	METAL	9.09 K		1%	81349	RN55D9091F
R28	000682	RES	CARBON	6.8 K		5% 1/4W	81349	RC07GF682J
R28A	000682	RES	CARBON	6.8 K		5% 1/4W	81349	RC07GF682J
R29	000682	RES	CARBON	6.8 K		5% 1/4W	81349	RC07GF682J
R29A	000682	RES	CARBON	6.8 K		5% 1/4W	81349	RC07GF682J
R30	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R30A	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R31	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R31A	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R32	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R32A	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R33	010705	RES	METAL	4.53 K	T-0	1%	81349	RN55D4531F
R33A	010705	RES	METAL	4.53 K	T-0	1%	81349	RN55D4531F
R34	040212	POT		25 K	UPE200-25K		11237	UPE200-25K
R34A	040212	POT		25 K	UPE200-25K		11237	UPE200-25K
R35	000391	RES	CARBON	390 OHM		5% 1/4W	81349	RC07GF391J
R35A	000391	RES	CARBON	390 OHM		5% 1/4W	81349	RC07GF391J
R36	000241	RES	CARBON	240 OHM		5% 1/4W	81349	RC07GF241J
R36A	000241	RES	CARBON	240 OHM		5% 1/4W	81349	RC07GF241J
R37	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R37A	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R38	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R38A	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
S202B		SWITCH	(PART OF R34 & R34A)					
S203B		SWITCH	(PART OF R34 & R34A)					
W1	600245	JUMPER			L-2007-1LP			L-2007-1LP
W2	600245	JUMPER			L-2007-1LP			L-2007-1LP

406631/406632 – Assy., PCB, SWITCH BOARD

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C2	100069	CAP	CERAM	20 PFD	1000 V	20%	56289	C023B102E220M
C3	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C4	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C6	100003	CAP	CERAM	3.3 PFD			71590	DD3R3
C7	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C8	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C9	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C10	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C11	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C12	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C13	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C14	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C15	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C20	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C21	100040	CAP	CERAM	200 PFD	1000 V	20%	56289	5GA-T20
C27	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C28	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C29	110104	CAP	TANTA	4.7 MFD	10 V	10%	05397	T310A475K010AS
C31	100068	CAP	CERAM	.02 MFD	100 V	20%	56289	TG-S20
C32	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C35	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C36	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C37	100053	CAP	CERAM	56 PFD	1000 V	5%	56289	10TCCQ56
C38	100051	CAP	CERAM	3 PFD	500 V		71471	TCD-B1-0
C39	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C40	100050	CAP	CERAM	2.2 PFD	1000 V	5%	56289	10TCCQ22
C41	100060	CAP	CERAM	15 PFD		5%	56289	10TCCQ15
C42	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C44	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C45	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C46	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C47	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C48	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C49	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C50	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C51	101145	CAP	CERAM	100 PFD	500 V	10%	71471	ETCD-DI-1(N5600)
C52	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C53	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C54	101145	CAP	CERAM	100 PFD	500 V	10%	71471	ETCD-DI-1(N5600)
C54	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C55	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C56	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A

406631/406632 – Assy., PCB, SWITCH BOARD *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
CR1	211083	DIODE SILICO 018	21793	211083
CR2	211083	DIODE SILICO 018	21793	211083
CR3	211083	DIODE SILICO 018	21793	211083
CR4	211083	DIODE SILICO 018	21793	211083
CR5	211083	DIODE SILICO 018	21793	211083
CR6	211083	DIODE SILICO 018	21793	211083
CR7	211083	DIODE SILICO 018	21793	211083
CR8	211083	DIODE SILICO 018	21793	211083
CR9	211083	DIODE SILICO 018	21793	211083
CR10	211083	DIODE SILICO 018	21793	211083
CR11	211083	DIODE SILICO 018	21793	211083
CR12	211083	DIODE SILICO 018	21793	211083
CR13	211083	DIODE SILICO 018	21793	211083
CR14	211083	DIODE SILICO 018	21793	211083
CR18	211083	DIODE SILICO 018	21793	211083
CR19	211083	DIODE SILICO 018	21793	211083
CR20	211083	DIODE SILICO 018	21793	211083
CR35	211083	DIODE SILICO 018	21793	211083
CR36	211083	DIODE SILICO 018	21793	211083
CR37	211083	DIODE SILICO 018	21793	211083
CR38	211083	DIODE SILICO 018	21793	211083
CR39	211083	DIODE SILICO 018	21793	211083
CR40	211083	DIODE SILICO 018	21793	211083
CR41	211083	DIODE SILICO 018	21793	211083
L1	310062	CHOKE RF 22 UH 1537-44	99800	1537-44
L2	310072	INDUCTOR 2.20 UH 10%	99800	1537-20
MA0	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
MA2	230064	INTEGRATED CIRCUIT SN7404N	01295	SN7404N
MA8	230099	INTEGRATED CIRCUIT SN7454N	01295	SN7454N
MA9	230037	INTEGRATED CIRCUIT SN7490N	01295	SN7490N
MA10	230037	INTEGRATED CIRCUIT SN7490N	01295	SN7490N
MB8	230064	INTEGRATED CIRCUIT SN7404N	01295	SN7404N
MB9	230037	INTEGRATED CIRCUIT SN7490N	01295	SN7490N
MB10	230037	INTEGRATED CIRCUIT SN7490N	01295	SN7490N
MC1	230043	INTEGRATED CIRCUIT MC1010P	04713	MC1010P
MC2	230064	INTEGRATED CIRCUIT SN7404N	01295	SN7404N
MC5	230079	INTEGRATED CIRCUIT SN74H00N	01295	SN74H00N
MC6	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
MC8	230099	INTEGRATED CIRCUIT SN7454N	01295	SN7454N
MC9	230037	INTEGRATED CIRCUIT SN7490N	01295	SN7490N
MC10	230037	INTEGRATED CIRCUIT SN7490N	01295	SN7490N
MD0	230112	INTEGRATED CIRCUIT MC10131P	04713	MC10131P
MD1	230039	INTEGRATED CIRCUIT MC1023P	04713	MC1023P

406631/406632 – Assy., PCB, SWITCH BOARD *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
MD2	230097	INTEGRATED CIRCUIT			MC1034P	04713	MC1034P
MD3	230096	INTEGRATED CIRCUIT			MC1032P	04713	MC1032P
MD4	230048	INTEGRATED CIRCUIT			MC1027P	04713	MC1027P
MD5	230030	INTEGRATED CIRCUIT			SN7402N	01295	SN7402N
MD6	230064	INTEGRATED CIRCUIT			SN7404N	01295	SN7404N
MD7	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
MD8	230064	INTEGRATED CIRCUIT			SN7404N	01295	SN7404N
MD9	230037	INTEGRATED CIRCUIT			SN7490N	01295	SN7490N
MD10	230037	INTEGRATED CIRCUIT			SN7490N	01295	SN7490N
ME0	230112	INTEGRATED CIRCUIT			MC10131P	04713	MC10131P
ME1	230072	INTEGRATED CIRCUIT			SN7474N	01295	SN7474N
ME2	230072	INTEGRATED CIRCUIT			SN7474N	01295	SN7474N
ME3	230081	INTEGRATED CIRCUIT			MC3060P	04713	MC3060P
ME4	230032	INTEGRATED CIRCUIT			SN7420N	01295	SN7420N
ME5	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
ME6	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
ME7	230030	INTEGRATED CIRCUIT			SN7402N	01295	SN7402N
ME8	230032	INTEGRATED CIRCUIT			SN7420N	01295	SN7420N
ME9	230064	INTEGRATED CIRCUIT			SN7404N	01295	SN7404N
ME10	230037	INTEGRATED CIRCUIT			SN7490N	01295	SN7490N
MF3	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
MF4	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
MF5	230031	INTEGRATED CIRCUIT			SN7410N	01295	SN7410N
MF6	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
MF7	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
MF8	230099	INTEGRATED CIRCUIT			SN7454N	01295	SN7454N
MF9	230072	INTEGRATED CIRCUIT			SN7474N	01295	SN7474N
MF10	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
P6	600483	CONN	COAX		27-7	02660	27-7
P7	600483	CONN	COAX		27-7	02660	27-7
P13*	600483	CONN	COAX		27-7	02660	27-7
Q1	200099	TRANS			2N4258	81349	2N4258
Q2	200099	TRANS			2N4258	81349	2N4258
Q3	200099	TRANS			2N4258	81349	2N4258
Q4	200099	TRANS			2N4258	81349	2N4258
Q5	200099	TRANS			2N4258	81349	2N4258
Q6	200099	TRANS			2N4258	81349	2N4258
Q7	200037	TRANS	SILICO	NPN	2N3646	80131	2N3646
Q9	200088	TRANS	SILICO	PNP	2N4248	80131	2N4248
Q10	200037	TRANS	SILICO	NPN	2N3646	80131	2N3646
Q11	200099	TRANS			2N4258	81349	2N4258
Q16	200037	TRANS	SILICO	NPN	2N3646	80131	2N3646
Q17	200088	TRANS	SILICO	PNP	2N4248	80131	2N4248

*Used only on 8030B Assy. 406632

406631/406632 -- Assy., PCB, SWITCH BOARD *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
Q19	200037	TRANS	SILICO	NPN	2N3646		80131	2N3646
Q20	200037	TRANS	SILICO	NPN	2N3646		80131	2N3646
Q21	200037	TRANS	SILICO	NPN	2N3646		80131	2N3646
Q22	200037	TRANS	SILICO	NPN	2N3646		80131	2N3646
Q23	200037	TRANS	SILICO	NPN	2N3646		80131	2N3646
R3	000821	RES	CARBON	820 OHM		5% 1/4W	81349	RC07GF821J
R4	000821	RES	CARBON	820 OHM		5% 1/4W	81349	RC07GF821J
R5	000200	RES	CARBON	20 OHM		5% 1/4W	81349	RC07GF200J
R6	000750	RES	CARBON	75 OHM		5% 1/4W	81349	RC07GF750J
R7	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R8	000471	RES	CARBON	470 OHM		5% 1/4W	81349	RC07GF471J
R9	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R10	000621	RES	CARBON	620 OHM		5% 1/4W	81349	RC07GF621J
R11	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R12	000240	RES	CARBON	24 OHM		5% 1/4W	81349	RC07GF240J
R13	000750	RES	CARBON	75 OHM		5% 1/4W	81349	RC07GF750J
R14	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R15	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R16	000821	RES	CARBON	820 OHM		5% 1/4W	81349	RC07GF821J
R17	000821	RES	CARBON	820 OHM		5% 1/4W	81349	RC07GF821J
R18	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R19	000112	RES	CARBON	1.1 K		5% 1/4W	81349	RC07GF112J
R20	000621	RES	CARBON	620 OHM		5% 1/4W	81349	RC07GF621J
R21	000621	RES	CARBON	620 OHM		5% 1/4W	81349	RC07GF621J
R22	000301	RES	CARBON	300 OHM		5% 1/4W	81349	RC07GF301J
R23	000391	RES	CARBON	390 OHM		5% 1/4W	81349	RC07GF391J
R24	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R25	000301	RES	CARBON	300 OHM		5% 1/4W	81349	RC07GF301J
R26	000242	RES	CARBON	2.4 K		5% 1/4W	81349	RC07GF242J
R27	000182	RES	CARBON	1.8 K		5% 1/4W	81349	RC07GF182J
R28	000391	RES	CARBON	390 OHM		5% 1/4W	81349	RC07GF391J
R29	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R30	000750	RES	CARBON	75 OHM		5% 1/4W	81349	RC07GF750J
R31	000240	RES	CARBON	24 OHM		5% 1/4W	81349	RC07GF240J
R32	000750	RES	CARBON	75 OHM		5% 1/4W	81349	RC07GF750J
R33	000240	RES	CARBON	24 OHM		5% 1/4W	81349	RC07GF240J
R34	000472	RES	CARBON	4.7 K		5% 1/4W	81349	RC07GF472J
R35	000472	RES	CARBON	4.7 K		5% 1/4W	81349	RC07GF472J
R36	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R37	000182	RES	CARBON	1.8 K		5% 1/4W	81349	RC07GF182J
R38	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R40	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R41	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R42	000430	RES	CARBON	43 OHM		5% 1/4W	81349	RC07GF430J

406631/406632 – Assy., PCB, SWITCH BOARD *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
R43	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R44	000200	RES	CARBON	20 OHM	5% 1/4W	81349	RC07GF200J
R45	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R46	000391	RES	CARBON	390 OHM	5% 1/4W	81349	RC07GF391J
R47	000182	RES	CARBON	1.8 K	5% 1/4W	81349	RC07GF182J
R48	000242	RES	CARBON	2.4 K	5% 1/4W	81349	RC07GF242J
R60	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R61	000242	RES	CARBON	2.4 K	5% 1/4W	81349	RC07GF242J
R62	000242	RES	CARBON	2.4 K	5% 1/4W	81349	RC07GF242J
R66	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R67	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R68	000123	RES	CARBON	12 K	5% 1/4W	81349	RC07GF123J
R69	000100	RES	CARBON	10 OHM	5% 1/4W	81349	RC07GF100J
R72	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R73	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R74	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R75	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R76	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R78	000471	RES	CARBON	470 OHM	5% 1/4W	81349	RC07GF471J
R79	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R80	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R81	000821	RES	CARBON	820 OHM	5% 1/4W	81349	RC07GF821J
R83	000821	RES	CARBON	820 OHM	5% 1/4W	81349	RC07GF821J
R84	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R86	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R89	000100	RES	CARBON	10 OHM	5% 1/4W	81349	RC07GF100J
R90	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R91	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R92	000122	RES	CARBON	1.2 K	5% 1/4W	81349	RC07GF122J
R93	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R94	000510	RES	CARBON	51 OHM	5% 1/4W	81349	RC07GF510J
R95	000100	RES	CARBON	10 OHM	5% 1/4W	81349	RC07GF100J
R96	000201	RES	CARBON	200 OHM	5% 1/4W	81349	RC07GF201J
R97	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R98	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R99	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R100	000153	RES	CARBON	15 K	5% 1/4W	81349	RC07GF153J
R101	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R102	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R103	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R108	000301	RES	CARBON	300 OHM	5% 1/4W	81349	RC07GF301J
R109	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R110	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R111	000122	RES	CARBON	1.2 K	5% 1/4W	81349	RC07GF122J
R112	000162	RES	CARBON	1.6 K	5% 1/4W	81349	RC07GF162J

406631/406632 – Assy., PCB, SWITCH BOARD *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
R113	000510	RES CARBON 51 OHM 5% 1/4W	81349	RC07GF510J
R114	000152	RES CARBON 1.5 K 5% 1/4W	81349	RC07GF152J
R116	000113	RES CARBON 11 K 5% 1/4W	81349	RC07GF113J
R117	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R118	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R119	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R120	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R121	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R122	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R123	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R124	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R126	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R127	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R128	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R129	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R130	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R131	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R132	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R133	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R134	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R135	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R136	000153	RES CARBON 15 K 5% 1/4W	81349	RC07GF153J
R137	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J
S1	600605	SWITCH PUSHBUTTON	71590	C18-PB101L
S2	600604	SWITCH PUSHBUTTON	71590	C18-PB2M
Y1	920583	CRYSTAL 9.9988 MHz	21793	920583

406145 – Assy., PCB, READOUT BOARD

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C5	110131	CAP	ELECT	20 MFD	450 V		56289	39D206F450GL4
C7	110146	CAP	ELECT	5000 MFD	10 V	–20% + 80%	56289	39D508G010HP4
C8	110062	CAP	ELECT	500 MFD	50 V		56289	39D507G050GL4
C9	110062	CAP	ELECT	500 MFD	50 V		56289	39D507G050GL4
C10	101641	CAP	CERAM	470 PFD	500 V	10%	71471	SCD1X5F
CR1	211083	DIODE	SILICO		018		21793	211083
CR2	211083	DIODE	SILICO		018		21793	211083
CR3	211083	DIODE	SILICO		018		21793	211083
CR4	211083	DIODE	SILICO				21793	211083
CR5	210004	DIODE	SILICO				81349	1N4004
CR6	210004	DIODE	SILICO				81349	1N4004
CR7	210004	DIODE	SILICO				81349	1N4004
CR8	210004	DIODE	SILICO				81349	1N4004
CR11	210004	DIODE	SILICO				81349	1N4004
CR12	210004	DIODE	SILICO				81349	1N4004
CR13	210004	DIODE	SILICO				81349	1N4004
CR14	210004	DIODE	SILICO				81349	1N4004
CR15	210004	DIODE	SILICO				81349	1N4004
CR16	210004	DIODE	SILICO				81349	1N4004
CR17	211083	DIODE	SILICO		018		21793	211083
CR18	220067	DIODE		ZENER	5.1 V	2%	04713	.4M5.1AZ2
CR19	210004	DIODE	SILICO				81349	1N4004
CR20	220015	DIODE	SILICO	ZENER	1N967B		81349	1N967B
CR21	211083	DIODE	SILICO		018		21793	211083
CR22	210004	DIODE	SILICO				81349	1N4004
CR23	220015	DIODE	SILICO	ZENER	1N967B		81349	1N967B
CR24	210004	DIODE	SILICO				81349	1N4004
CR25	211083	DIODE	SILICO		018		21793	211083
CR28	210004	DIODE	SILICO				81349	1N4004
CR29	210004	DIODE	SILICO				81349	1N4004
CR30	211083	DIODE	SILICO		018		21793	211083
CR40	211083	DIODE	SILICO		018		21793	211083
D1	920602	NEON	BULB		A1C-A		74276	A1C-A
D2	920602	NEON	BULB		A1C-A		74276	A1C-A
D3	920602	NEON	BULB		A1C-A		74276	A1C-A
D4	920602	NEON	BULB		A1C-A		74276	A1C-A
D5	920602	NEON	BULB		A1C-A		74276	A1C-A
D6	920602	NEON	BULB		A1C-A		74276	A1C-A

406145 – Assy., PCB, READOUT BOARD *continued*

REF DES	DANA P/N	DESCRIPTION		FSC	MANU P/N
D7	920602	NEON BULB	A1C-A	74276	A1C-A
J5	600665	TERMINAL, PC	R62-3	27264	R62-3
MA7	230064	INTEGRATED CIRCUIT	SN7404N	01295	SN7404N
MA8	230031	INTEGRATED CIRCUIT	SN7410N	01295	SN7410N
MA9	230099	INTEGRATED CIRCUIT	SN7454N	01295	SN7454N
MA10	230099	INTEGRATED CIRCUIT	SN7454N	01295	SN7454N
MA11	230031	INTEGRATED CIRCUIT	SN7410N	01295	SN7410N
MA12	230064	INTEGRATED CIRCUIT	SN7404N	01295	SN7404N
MB7	230064	INTEGRATED CIRCUIT	SN7404N	01295	SN7404N
MB8	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
MB9	230099	INTEGRATED CIRCUIT	SN7454N	01295	SN7454N
MB10	230099	INTEGRATED CIRCUIT	SN7454N	01295	SN7454N
MB11	230031	INTEGRATED CIRCUIT	SN7410N	01295	SN7410N
MB12	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
MC1	230064	INTEGRATED CIRCUIT	SN7404N	01295	SN7404N
MC2	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
MC3	230031	INTEGRATED CIRCUIT	SN7410N	01295	SN7410N
MC7	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
MC8	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
MC9	230098	INTEGRATED CIRCUIT	SN7451N	01295	SN7451N
MC10	230098	INTEGRATED CIRCUIT	SN7451N	01295	SN7451N
MC11	230098	INTEGRATED CIRCUIT	SN7451N	01295	SN7451N
MC12	230099	INTEGRATED CIRCUIT	SN7454N	01295	SN7454N
MD2	230037	INTEGRATED CIRCUIT	SN7490N	01295	SN7490N
MD3	230037	INTEGRATED CIRCUIT	SN7490N	01295	SN7490N
MD4	230037	INTEGRATED CIRCUIT	SN7490N	01295	SN7490N
MD5	230037	INTEGRATED CIRCUIT	SN7490N	01295	SN7490N
MD6	230037	INTEGRATED CIRCUIT	SN7490N	01295	SN7490N
MD7	230037	INTEGRATED CIRCUIT	SN7490N	01295	SN7490N
MD8	230037	INTEGRATED CIRCUIT	SN7490N	01295	SN7490N
MD10	230064	INTEGRATED CIRCUIT	SN7404N	01295	SN7404N
MD11	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
MD12	230099	INTEGRATED CIRCUIT	SN7454N	01295	SN7454N
ME2	230065	INTEGRATED CIRCUIT	SN7475N	01295	SN7475N
ME3	230065	INTEGRATED CIRCUIT	SN7475N	01295	SN7475N
ME4	230065	INTEGRATED CIRCUIT	SN7475N	01295	SN7475N
ME5	230065	INTEGRATED CIRCUIT	SN7475N	01295	SN7475N
ME6	230065	INTEGRATED CIRCUIT	SN7475N	01295	SN7475N
ME7	230065	INTEGRATED CIRCUIT	SN7475N	01295	SN7475N
ME8	230065	INTEGRATED CIRCUIT	SN7475N	01295	SN7475N
ME9	230065	INTEGRATED CIRCUIT	SN7475N	01295	SN7475N
MF2	230034	INTEGRATED CIRCUIT	SN74141N	01295	SN74141N
MF3	230034	INTEGRATED CIRCUIT	SN74141N	01295	SN74141N

406145 – Assy., PCB, READOUT BOARD *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
MF4	230034	INTEGRATED CIRCUIT SN74141N	01295	SN74141N
MF5	230034	INTEGRATED CIRCUIT SN74141N	01295	SN74141N
MF6	230034	INTEGRATED CIRCUIT SN74141N	01295	SN74141N
MF7	230034	INTEGRATED CIRCUIT SN74141N	01295	SN74141N
MF8	230034	INTEGRATED CIRCUIT SN74141N	01295	SN74141N
MF9	230034	INTEGRATED CIRCUIT SN74141N	01295	SN74141N
Q1	200037	TRANS SILICO NPN 2N3646	80131	2N3646
Q5	200087	TRANS SILICO 021	21793	200087
Q6	200087	TRANS SILICO 021	21793	200087
Q7	200087	TRANS SILICO 021	21793	200087
Q8	200087	TRANS SILICO 021	21793	200087
Q9	200087	TRANS SILICO 021	21793	200087
Q10	200087	TRANS SILICO 021	21793	200087
Q11	200087	TRANS SILICO 021	21793	200087
Q12	200037	TRANS SILICO NPN 2N3646	80131	2N3646
Q15	200087	TRANS SILICO 021	21793	200087
Q17	200087	TRANS SILICO 021	21793	200087
Q18	200087	TRANS SILICO 021	21793	200087
Q19	200087	TRANS SILICO 021	21793	200087
Q20	200087	TRANS SILICO 021	21793	200087
Q21	200087	TRANS SILICO 021	21793	200087
Q22	200087	TRANS SILICO 021	21793	200087
Q23	200087	TRANS SILICO 021	21793	200087
Q25	200052	TRANS SILICO PNP 009	21793	200052
Q26	200088	TRANS SILICO PNP 2N4248	80131	2N4248
Q27	200043	TRANS	21793	200043
Q28	200043	TRANS	21793	200043
R1	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R2	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R3	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R4	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R5	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R6	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R7	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R8	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R10	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R11	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R12	000622	RES CARBON 6.2 K 5% 1/4W	81349	RC07GF622J
R15	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R16	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R17	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R18	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R19	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J

406145 – Assy., PCB, READOUT BOARD *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
R20	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R21	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R22	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R23	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R24	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R26	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R28	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R30	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R32	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R34	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R36	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R39	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R40	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R41	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R42	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R43	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R45	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R46	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R47	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R48	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R49	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R50	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R51	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R52	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R53	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R54	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R55	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R56	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R57	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R60	020620	RES	WW	3.9 K	5% 3 W	21551	M20D
R61	000204	RES	CARBON	200 K	5% 1/4W	81349	RC07GF204J
R62	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R63	001793	RES	CARBON	1 K	5% 1/2W	01121	See Descrpt.
R64	001765	RES	CARBON	68 OHM	5% 1/2W	81349	RC07GF680J
R65	000272	RES	CARBON	2.7 K	5% 1/4W	81349	RC07GF272J
R66	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R67	000362	RES	CARBON	3.6 K	5% 1/4W	81349	RC07GF362J
R68	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R69	000272	RES	CARBON	2.7 K	5% 1/4W	81349	RC07GF272J
R70	000242	RES	CARBON	2.4 K	5% 1/4W	81349	RC07GF242J
R71	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R72	000272	RES	CARBON	2.7 K	5% 1/4W	81349	RC07GF272J
R73	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R74	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J

406145 – Assy., PCB, READOUT BOARD *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R76	000821	RES	CARBON	820 OHM		5% 1/4W	81349	RC07GF821J
R77	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
V1	920506	TUBE	NEON		ZM1000		73445	ZM1000
V2	920506	TUBE	NEON		ZM1000		73445	ZM1000
V3	920506	TUBE	NEON		ZM1000		73445	ZM1000
V4	920506	TUBE	NEON		ZM1000		73445	ZM1000
V5	920506	TUBE	NEON		ZM1000		73445	ZM1000
V6	920506	TUBE	NEON		ZM1000		73445	ZM1000
V7	920506	TUBE	NEON		ZM1000		73445	ZM1000
V8	920506	TUBE	NEON		ZM1000		73445	ZM1000
W3	600245	JUMPER			L-2007-1LP			L-2007-1LP

406580 – Assy.,PCB, REAR PANEL

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	5GAS-S10
C2	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	5GAS-S10
F101	920205	FUSE		.75 A	250 V		75915	3AG3/4ASB
H1	730423	HEATSINK			730423		21793	730423
J101	600619	CONN	RECPTLE				82389	EAC-301
J102	600567	CONN	RECPTLE		31-236		02660	31-236
J103	600567	CONN	RECPTLE		31-236		02660	31-236
J104	600567	CONN	RECPTLE		31-236		02660	31-236
J106	600567	CONN	RECPTLE		31-236		02660	31-236
J107	920574	COVER	HOLE		P-562		28520	P-562
J108	920573	COVER	HOLE		P-437		28520	P-437
J109	920573	COVER	HOLE		P-437		28520	P-437
J110	600589	POST	BINDING	RED	820-65		32767	820-65
J111	600587	POST	BINDING	BLK	820-45		32767	820-45
J112	600586	POST	BINDING	WHITE	820-25		32767	820-25
P1	600566	CONN	6 PIN		251-0630160		71785	251-0630160
Q101	200223	TRANS		NPN	MJE521		04713	MJE521
Q102	200130	TRANS	SILICO	NPN	MJE3055		04713	MJE3055
Q103	200183	TRANS	SILICO	PNP	MJE371		04713	MJE371
S101	600680	SWITCH	SLIDE, SPDT		GF-124		79727	GF-124
S102	600617	SWITCH	SLIDE, DPDT		G126		79727	G126
T101	300065	TRANSFORMER		115 V	11824		23095	11824

406732 – Assy., REAR PANEL, PART OF OPTION 200 & 300

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
B1	600759	MOTOR	FAN	TYPE AYAA	115 V		05624	AYAA
C1	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	5GAS-S10
C2	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	5GAS-S10
F101	920205	FUSE	GLASS	.75 A	250 V (115V Operation)		75915	3AG3/4ASB
	920204	FUSE	SLOW	.50 A	250 V (220V Operation)		75915	3AG1/2ASB
J101	600619	CONN	RECPTLE		EAC-301		82389	EAC-301
J102	600567	CONN	RECPTLE		31-236		02660	31-236
J103	600567	CONN	RECPTLE		31-236		02660	31-236
J104	600567	CONN	RECPTLE		31-236		02660	31-236
J105	600567	CONN	RECPTLE		31-236		02660	31-236
J106	920573	COVER	HOLE		P-437		28520	P-437
J107	920573	COVER	HOLE		P-437		28520	P-437
J108	920574	COVER	HOLE		P-562		28520	P-562
P1	600566	CONN	6 PIN		251-0630160		71785	251-0630160
Q101	200155	TRANS	SILICO	NPN	MJE520		04713	MJE520
Q102	200130	TRANS	SILICO	NPN	MJE3055		04713	MJE3055
Q103	200154	TRANS	SILICO	PNP	MJE370		04713	MJE370
S101	600680	SWITCH	SLIDE	SPDT	GF124		79727	GF124
S102	600617	SWITCH	SLIDE	DPDT	G126		79727	G126
S103	600521	SWITCH	SLIDE	DPDT	46256LFR		82389	46256LFR
T101	300065	TRANSFORMER		POWER	115 V		23095	11824
W101	600245	JUMPER			L-2007-1LP			L-2007-1LP

406561 – Assy., PCB, DISPLAY TIME CONTROL

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
P3	600593	CONN 6 PIN 250-0630170	71785	250-0630170
	600250	KEY	71785	456-07-35-003
P5	600545	PLUG 3 PIN 1625-3P-1	27264	1625-3P-1
	600381	TERM, PIN 1561	27264	1561
R1		POT 1 MEG (PART OF 600600)		
S205	600600	SWITCH ROTARY SPST CTS45	11237	CTS45

406128 – Assy., PCB, INTERCONNECT BOARD

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
P2	600575	CONN 25 PIN 252-2530160	71785	252-2530160
P4	600575	CONN 25 PIN 252-2530160	71785	252-2530160

406663 – Assy., PCB, 9 DIGIT READOUT, OPTION 004

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
MD1	230037	INTEGRATED CIRCUIT			SN7490N		01295	SN7490N
ME1	230065	INTEGRATED CIRCUIT			SN7475N		01295	SN7475N
MF1	230034	INTEGRATED CIRCUIT			SN74141N		01295	SN74141N
R9	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
V9	920506	TUBE	NEON		ZM1000		73445	ZM1000

For location of parts:

Refer to Layout and Schematic Readout Board, Pages 6-8 and 6-10

406660-662 – Assy., REAR INPUT, OPTION 010 (Rear Panel 406580, Page 6-13)

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
J107	406564	CONN ASSY, BNC CABLE 406564	21793	406564
J108	600567	CONN RECPTLE 31-236	02660	31-236
J109	600567	CONN RECPTLE 31-236	02660	31-236
R108	001803	RES CARBON 24 OHM 5% 1/8W	81349	RC05GF240J
R109	001803	RES CARBON 24 OHM 5% 1/8W	81349	RC05GF240J

406735 – Assy., REAR INPUT, OPTION 010 (Rear Panel 406732, Page 6-15)

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
J106	406564	CONN ASSY, BNC CABLE 406564	21793	406564
J107	600567	CONN RECPTLE 31-236	02660	31-236
J108	600567	CONN RECPTLE 31-236	02660	31-236
R107	000240	RES CARBON 24 OHM 5% 1/4W	81349	RC07GF240J
R108	000240	RES CARBON 24 OHM 5% 1/4W	81349	RC07GF240J

406659 – Assy., PCB, TCXO OSCILLATOR, OPTION 050

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
W5	600245	JUMPER L-2007-1LP		L-2007-1LP
Y1	730578	OSCILLATOR CRYSTAL 730578	21793	730578

For location of parts:

Refer to Layout and Schematic Readout Board, Pages 6-8 and 6-11

406749 – Assy., OSCILLATOR, OPTION 200

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
A1*	406130	28V REGULATOR ASSY			406130		21793	406130
A2**	406732	REAR PANEL ASSY			406732		21793	406732
C1	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	5GAS-S10
C6*	110062	CAP	ELECT	500 MFD	50 V		56289	39D507G050GL4
CR9*	210004	DIODE	SILICO		1N4004		81349	1N4004
CR10*	210004	DIODE	SILICO		1N4004		81349	1N4004
Y101	730647	OSCILLATOR			730647		21793	730647

406748 – Assy., OSCILLATOR, OPTION 300

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
A1*	406130	28V REGULATOR ASSY			406130		21793	406130
A2**	406732	REAR PANEL ASSY			406732		21793	406732
C1	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	5GAS-S10
C6*	110062	CAP	ELECT	500 MFD	50 V		56289	39D507G050GL4
CR9*	210004	DIODE	SILICO		1N4004		81349	1N4004
CR10*	210004	DIODE	SILICO		1N4004		81349	1N4004
Y101	730648	OSCILLATOR			730648		21793	730648

*Located on Readout Board
**Schematic and Assy. Rear Panel, Pages 6-14, 6-15
Parts List, Page 7-20

406130 – Assy., PCB, 28V REGULATOR, PART OF OPTION 200 & 300

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
J1	600664	TERMINAL BOARD PIN					27264	M93-102
	600665	TERMINAL BOARD PIN					27264	R62-3
C1	101098	CAP	CERAM	330 PFD		10%	56289	C016B102E331K
CR1	220061	DIODE	ZENER		28 V	5% 1/2W	81349	1N5255B
CR2	211083	DIODE	SILICO		018		21793	211083
Q1	200154	TRANS	SILICO	PNP	MJE370		04713	MJE370
Q2	200037	TRANS	SILICO	NPN	2N3646		80131	2N3646
R1	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R2	000332	RES	CARBON	3.3 K		5% 1/4W	81349	RC07GF332J

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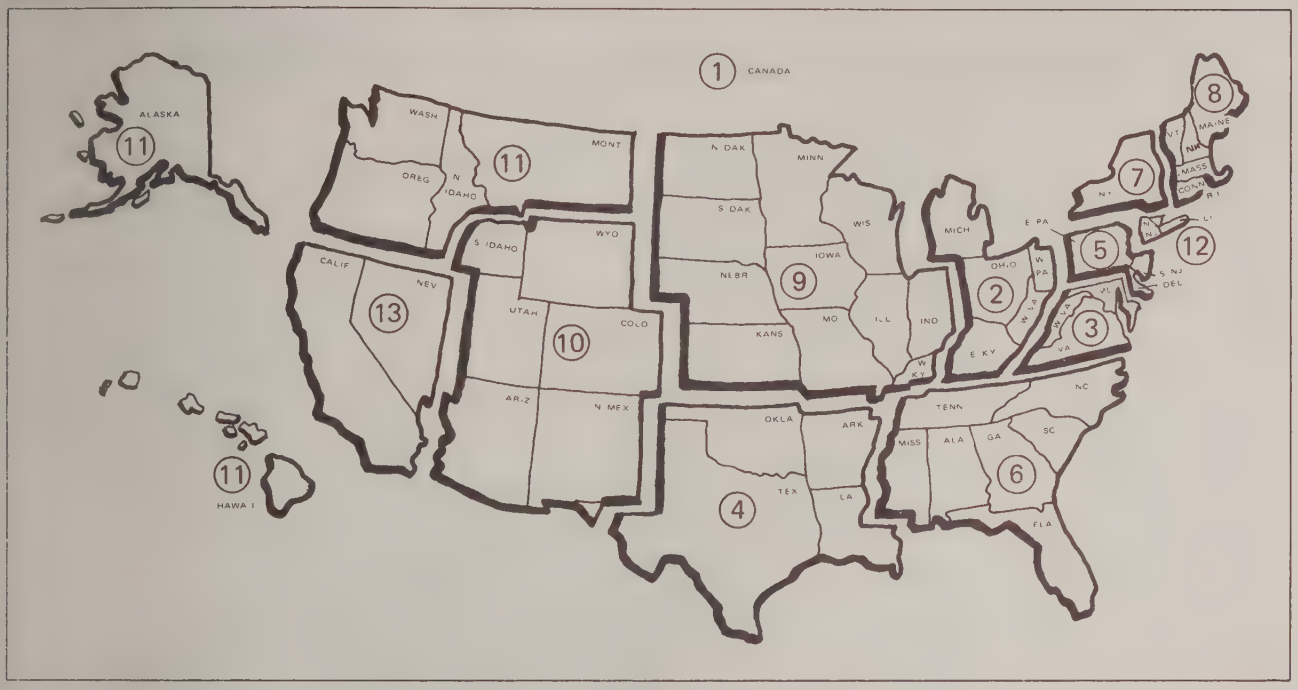

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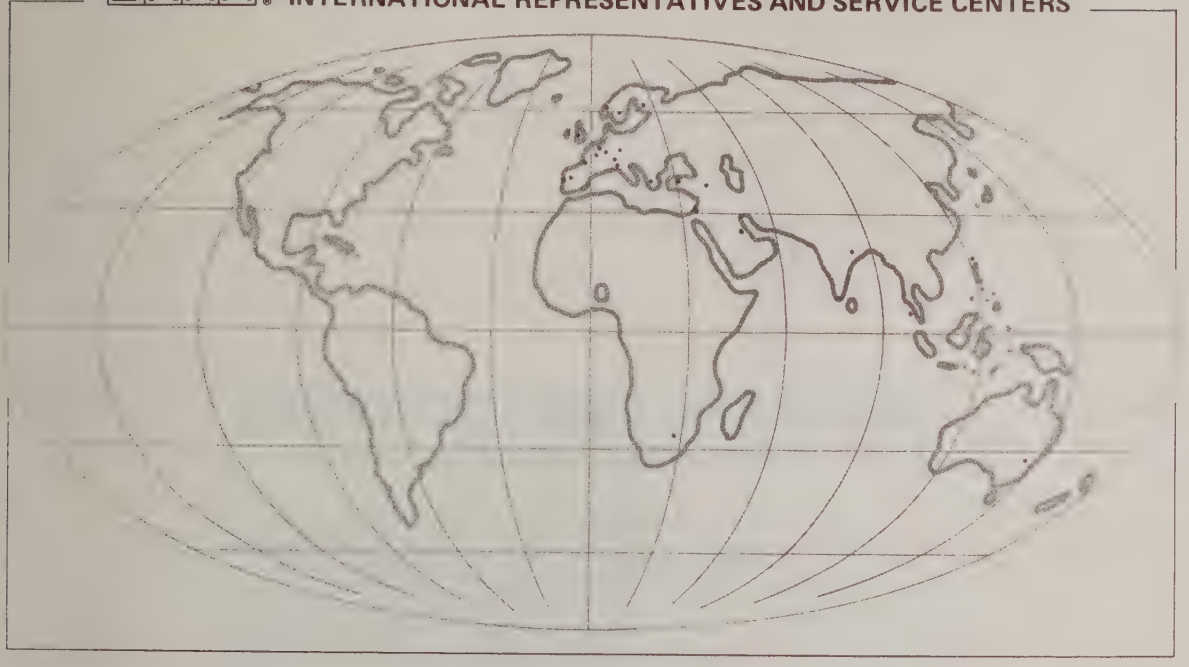

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INSTRUCTION MANUAL

SYSTEMS INTERFACE

FOR 8000B SERIES COUNTERS

DANA®

PUBLICATION NO. 980469

SYSTEMS INTERFACE

FOR 8000B SERIES COUNTERS

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SECTION 1 GENERAL DESCRIPTION

1.1 INTRODUCTION.

1.2 This manual describes the use and operation of the Models 008 and 009 Systems Interface options, used on the Dana Series 8000B Electronic Counters. The options are internally mounted in the counter and receive all operational power from the counter. The options permit the instrument to be operated remotely by electrical input and provide data from the counter readout in Binary Coded Decimal (BCD) form for use by a digital recorder or other digitally operated device.

1.3 RECORDER.

1.4 The Recorder output from both options is the same and is in the form of BCD, positive-true, 1-2-4-8 code from TTL integrated circuits. The output supplies, in digital form, the numeric value of the readout, the annunciator displayed, and the position of the decimal.

1.5 Physically the output consists of a cable assembly connecting various points on the counters readout board to two edge-type connectors (J111, J112), located on the rear panel of the counter.

1.6 008 PROGRAMMING OPTION.

1.7 The programming portion of the 008 option consists of a cable assembly providing interconnection between programming edge connector J110 on the rear panel and the readout PC board, and interconnection from J110 through connector P8 to the signal control module.

1.8 The programming portion of the 008 option provides single line commands for the control of function, time base, external gate, +/– slope, hold, and reset. The single line inputs are held true by internal pull up resistors; commands are initiated on these lines by means of a contact closure to ground potential or low TTL level (inputs are TTL gates). Analog programming is available through programming connector J110. The analog inputs determine the trigger level of the signal control module circuitry. A synopsis of 008 capabilities is provided in table 1.1.

1.9 009 PROGRAMMING OPTION.

1.10 The programming portion of the 009 option also consists of a cable assembly and provides interconnection between a 50 pin programming connector J113 on the rear panel and the readout PC board. The cabling also includes interconnection from J113 and a specially modified version of the signal control module.

1.11 The programming portion of the 009 module provides binary encoded commands for the control of function, time base, channel range, and trigger level. It provides single line commands for external gate, +/– slope, hold, reset, separate/common, and ac/dc.

1.12 The digital input lines are held true by internal pull up resistors; commands are generated on these lines, for both single line commands or binary encoded, by contact closure to ground potential or low TTL level (inputs are TTL gates). Analog programming is also available through programming connector J113. The analog inputs are provided as an alternative to digitally selecting the trigger level of the signal control module or can be used in conjunction with the digital controlled input for continuous adjustment between the incremental steps. A synopsis of 009 capabilities is shown in table 1.2.

1.13 SPECIFICATIONS.

1.14 The specifications for all remote selected instrument functions, with the exception of trigger levels, are the same as for local selection and are provided in the counter manual. Specifications for remote selection of trigger levels are provided in table 1.3.

1.15 Miscellaneous.

1.16 ITEMS FURNISHED (008).

1.17 Included with instruments equipped with the 008 option are three edge-type mating connectors, Dana P/N 600698 (with hoods, Dana P/N 453890).

1.18 ITEMS FURNISHED (009).

1.19 Included with instruments equipped with the 009 option are two edge-type mating connectors, Dana P/N 600698 (with hoods, Dana P/N 453890), and one 50-pin connector, Dana P/N 600047.

1.20 REQUIRED TOOLS AND TEST EQUIPMENT.

1.21 No calibration is required for the 008 option. The calibration equipment needed and the tools used for the 009 option are a portion of the equipment used for the calibration of the counter. An aid for calibrating the 009 option consists of a 50-pin mating connector for programming connector J113 with certain pins interconnected. This is described in Section 4.

Table 1.1 - Option 008 Programming

Program Title	Program Mode	Applicable to Models:				
		8010B	8015B	8020B	8030B	8035B
Functions:						
Remote	Single Line Digital	X	X	X	X	X
Check	Single Line Digital	X	X	X	X	X
Period	Single Line Digital	X	X	X	X	X
Period Ave.	Single Line Digital	X	X	X	X	X
Frequency A	Single Line Digital	X	X	X	X	X
Frequency C	Single Line Digital			X	X	X
Totalize	Single Line Digital	X	X	X	X	X
A/B Ratio	Single Line Digital	X	X		X	X
Time Interval	Single Line Digital	X	X		X	X
Time Int. Ave.	Single Line Digital	X			X	
Input Controls:						
Slope A	Single Line Digital	X	X	X	X	X
Trig Level A	Single Line Analog	X	X	X	X	X
Slope B	Single Line Digital	X	X		X	X
Trig Level B	Single Line Analog	X	X		X	X
Time Base:						
10 ns	Single Line Digital		X			X
1+100 ns	Single Line Digital	X	X	X	X	X
10+1 μs	Single Line Digital	X	X	X	X	X
10^2+10 μs	Single Line Digital	X	X	X	X	X
10^3+100 μs	Single Line Digital	X	X	X	X	X
10^4+1 ms	Single Line Digital	X	X	X	X	X
10^5+10 ms	Single Line Digital	X	X	X	X	X
10^6+100 ms	Single Line Digital	X	X	X	X	X
10^7+1 sec	Single Line Digital	X	X	X	X	X
10^8+10 sec	Single Line Digital	X	X	X	X	X
10^9+100 sec	Single Line Digital	X	X	X	X	X
Program Functions:						
HOLD	Single Line Digital	X	X	X	X	X
RESET	Single Line Digital	X	X	X	X	X
Ext. Gate	Single Line Digital	X	X	X	X	X

SECTION 1 GENERAL DESCRIPTION

1.1 INTRODUCTION.

1.2 This manual describes the use and operation of the Models 008 and 009 Systems Interface options, used on the Dana Series 8000B Electronic Counters. The options are internally mounted in the counter and receive all operational power from the counter. The options permit the instrument to be operated remotely by electrical input and provide data from the counter readout in Binary Coded Decimal (BCD) form for use by a digital recorder or other digitally operated device.

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1.12 The digital input lines are held true by internal pull up resistors; commands are generated on these lines, for both single line commands or binary encoded, by contact closure to ground potential or low TTL level (inputs are TTL gates). Analog programming is also available through programming connector J113. The analog inputs are provided as an alternative to digitally selecting the trigger level of the signal control module or can be used in conjunction with the digital controlled input for continuous adjustment between the incremental steps. A synopsis of 009 capabilities is shown in table 1.2.

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1.17 Included with instruments equipped with the 008 option are three edge-type mating connectors, Dana P/N 600698 (with hoods, Dana P/N 453890).

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1.19 Included with instruments equipped with the 009 option are two edge-type mating connectors, Dana P/N 600698 (with hoods, Dana P/N 453890), and one 50-pin connector, Dana P/N 600047.

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1.21 No calibration is required for the 008 option. The calibration equipment needed and the tools used for the 009 option are a portion of the equipment used for the calibration of the counter. An aid for calibrating the 009 option consists of a 50-pin mating connector for programming connector J113 with certain pins interconnected. This is described in Section 4.

Table 1.1 - Option 008 Programming

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		8010B	8015B	8020B	8030B	8035B
Functions:						
Remote	Single Line Digital	X	X	X	X	X
Check	Single Line Digital	X	X	X	X	X
Period	Single Line Digital	X	X	X	X	X
Period Ave.	Single Line Digital	X	X	X	X	X
Frequency A	Single Line Digital	X	X	X	X	X
Frequency C	Single Line Digital			X	X	X
Totalize	Single Line Digital	X	X	X	X	X
A/B Ratio	Single Line Digital	X	X		X	X
Time Interval	Single Line Digital	X	X		X	X
Time Int. Ave.	Single Line Digital	X			X	
Input Controls:						
Slope A	Single Line Digital	X	X	X	X	X
Trig Level A	Single Line Analog	X	X	X	X	X
Slope B	Single Line Digital	X	X		X	X
Trig Level B	Single Line Analog	X	X		X	X
Time Base:						
10 ns	Single Line Digital		X			X
1+100 ns	Single Line Digital	X	X	X	X	X
10+1 μs	Single Line Digital	X	X	X	X	X
10^2+10 μs	Single Line Digital	X	X	X	X	X
10^3+100 μs	Single Line Digital	X	X	X	X	X
10^4+1 ms	Single Line Digital	X	X	X	X	X
10^5+10 ms	Single Line Digital	X	X	X	X	X
10^6+100 ms	Single Line Digital	X	X	X	X	X
10^7+1 sec	Single Line Digital	X	X	X	X	X
10^8+10 sec	Single Line Digital	X	X	X	X	X
10^9+100 sec	Single Line Digital	X	X	X	X	X
Program Functions:						
HOLD	Single Line Digital	X	X	X	X	X
RESET	Single Line Digital	X	X	X	X	X
Ext. Gate	Single Line Digital	X	X	X	X	X

Table 1.2 - Option 009 Programming

Program Title	Program Mode	Applicable to Models:			
		8010B	8015B	8030B	8035B
Functions:					
Remote	4-Line BCD	X	X	X	X
Check	4-Line BCD	X	X	X	X
Period	4-Line BCD	X	X	X	X
Period Ave.	4-Line BCD	X	X	X	X
Frequency A	4-Line BCD	X	X	X	X
Frequency C	4-Line BCD			X	X
Totalize	4-Line BCD	X	X	X	X
A/B Ratio	4-Line BCD	X	X	X	X
Time Interval	4-Line BCD	X	X	X	X
Time Int. Avg.	4-Line BCD	X		X	
Input Controls:					
Sep/Com	Single Line Digital	X	X	X	X
Slope A	Single Line Digital	X	X	X	X
AC/DC A	Single Line Digital	X	X	X	X
Range A	2-Line BCD	X	X	X	X
Anal. Trig. Level A	Single Line Analog	X	X	X	X
Dig. Trig. Level A	7-Line Binary	X	X	X	X
Slope B	Single Line Digital	X	X	X	X
AC/DC B	Single Line Digital	X	X	X	X
Range B	2-Line BCD	X	X	X	X
Anal. Trig. Level B	Single Line Analog	X	X	X	X
Dig. Trig. Level B	7-Line Binary	X	X	X	X
Time Base:					
10 ns	Single Line Digital		X		X
1+100 ns	4-Line BCD	X	X	X	X
10+1 μs	4-Line BCD	X	X	X	X
10^2+10 μs	4-Line BCD	X	X	X	X
10^3+100 μs	4-Line BCD	X	X	X	X
10^4+1 ms	4-Line BCD	X	X	X	X
10^5+10 ms	4-Line BCD	X	X	X	X
10^6+100 ms	4-Line BCD	X	X	X	X
10^7+1 sec	4-Line BCD	X	X	X	X
10^8+10 sec	4-Line BCD	X	X	X	X
10^9+100 sec	4-Line BCD	X	X	X	X
Program Functions:					
HOLD	Single Line Digital	X	X	X	X
RESET	Single Line Digital	X	X	X	X
Ext. Gate	Single Line Digital	X	X	X	X

Table 1.3 - Trigger Level Specifications

Analog (Options 008/009)	Supply Voltage (.1V per % of range) into 10 kohms to set desired level; Accuracy: ±2% of range ±.2% of range per °C ±Transient Error* ±Attenuator Error**
Digital (Option 009)	7 Bit Code, 5% of range per step, ±300% of Range Span; Accuracy: ±5% of range ±.2% of range/°C ±Transient Error* ±Attenuator Error**

*Transient Error $\leq \left[\frac{\text{Slope}}{\text{Range}}\left(\frac{V}{\mu S}\right)\right]^{1/2}$ Percent of Range

**Attenuator Error

Frequency	Accuracy (% of Range)		
	Range		
	X1	X10	X100
0 ⟶ 1 kHz	1	2	3
1 kHz ⟶ 10 kHz	1	4	4
10 kHz ⟶ 100 kHz	1	8	8
100 kHz ⟶ 1 MHz	1	8	8

2.1 RECORDER OUTPUT.

2.2 The recorder output is provided at the back panel of the instrument on two edge-type connectors J111 and J112. The connectors are slotted between pins 2 and 3 of J111 and pins 3 and 4 of J112 to permit keying of the mating connectors.

2.3 The data from the two connectors is a Binary Coded Decimal (BCD), positive-true, 1-2-4-8 code. The logic levels for the output are defined as:

"0" = 0 volts to +0.8 volts

"1" = +2.4 volts to +5 volts

2.4 The recorder produces a binary coded representation of the instrument display. This includes the numeric readout, the decimal position and the annunciator as shown in figure 2.1.

2.5 Cabling.

2.6 Two mating connectors (Dana P/N 600698) come with the instrument for the RECORDER output. Pin identification for the connectors is provided in figure 2.2, and table 2.1. The outputs are described in the following paragraphs.

2.7 NUMERIC READOUT.

2.8 The numeric readout lines have the designations V1 through V9. The designators represent the corresponding readout "windows" with V1 to the right, the least-significant bit. For example, a seven in the most-significant bit is shown as:

V9-8	logic 0
V9-4	logic 1
V9-2	logic 1
V9-1	logic 1

2.9 ANNUNCIATOR.

2.10 A separate line is provided for each unit on the annunciator. The units identify the units of time or frequency in which the measurement is expressed and is indicated when the particular output line is at logic true.

2.11 DECIMAL.

2.12 A separate line is provided for each of the eight decimal points. The designators DP1 through DP8 describe the number of places to the left of the least-significant digit the decimal is located. The decimal position is indicated by a logic true.

2.13 PRINT.

2.14 The print command indicates that the data is at the output connectors and is available for recording. The print pulse is a 0 to +5 volt pulse of 5 microsecond duration.

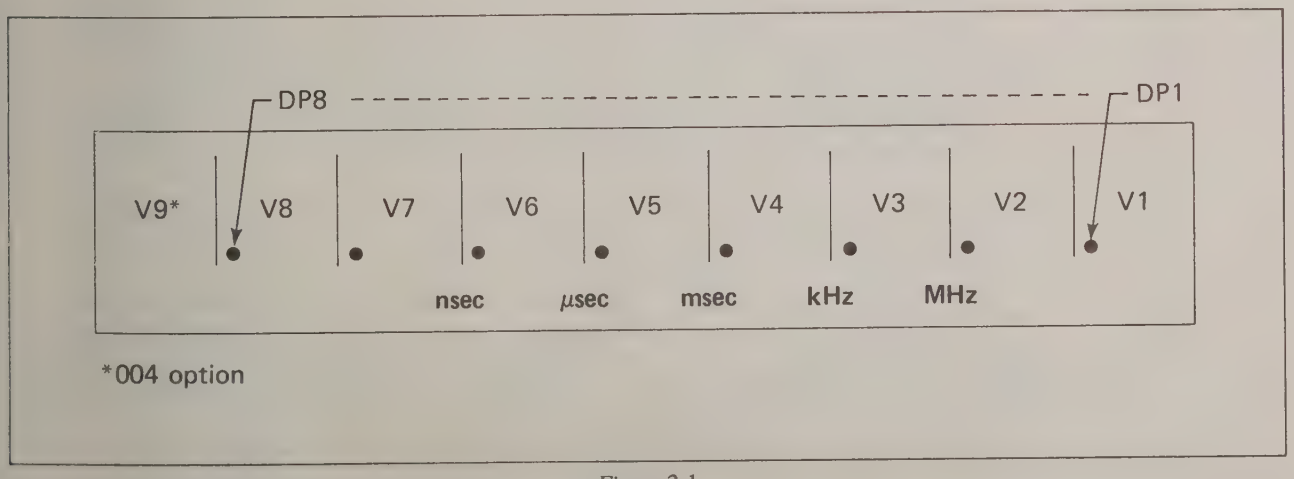


Figure 2.1

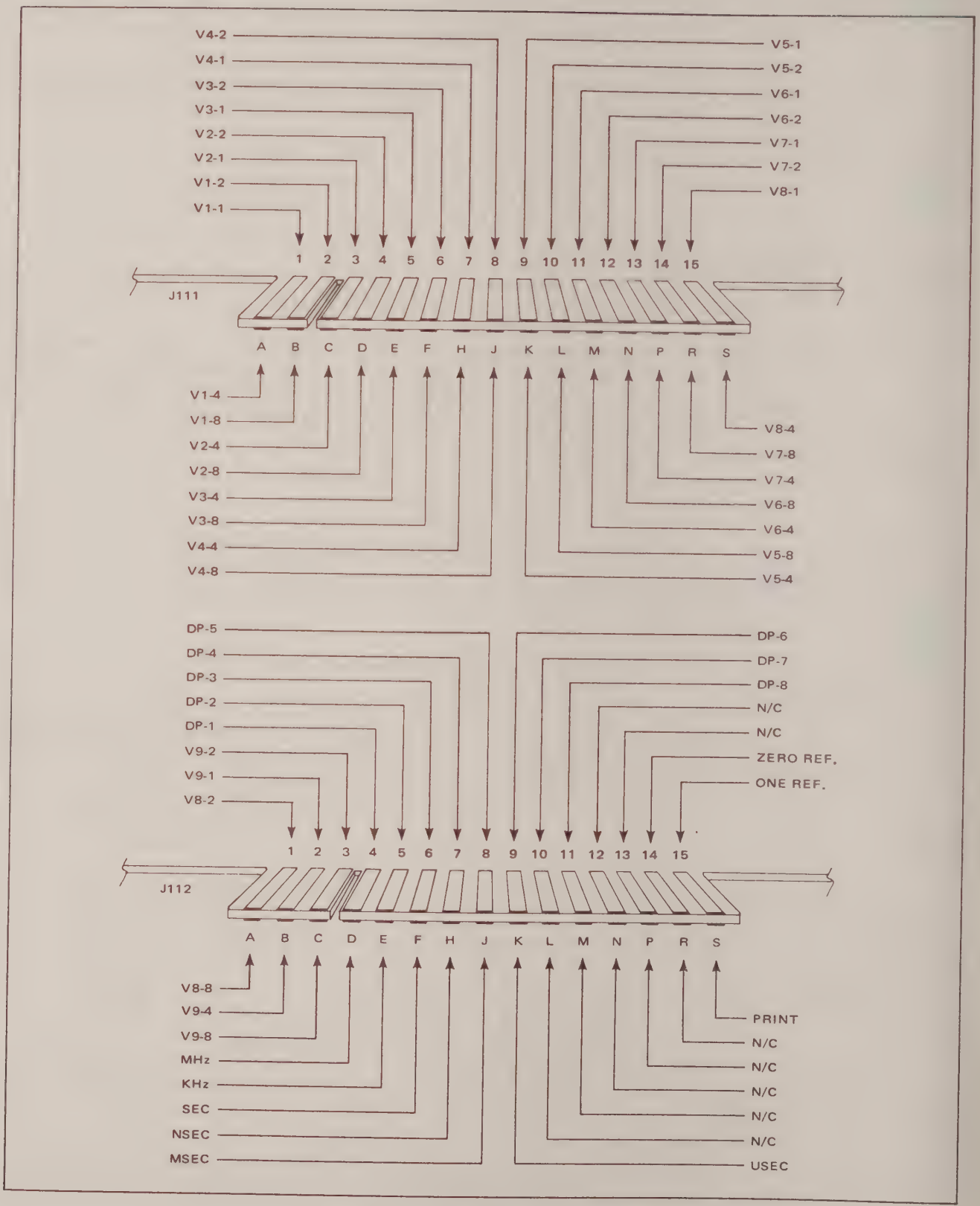


Figure 2.2 - J111 and J112 Recorder Outputs

Table 2.1 - Recorder Cabling Guide

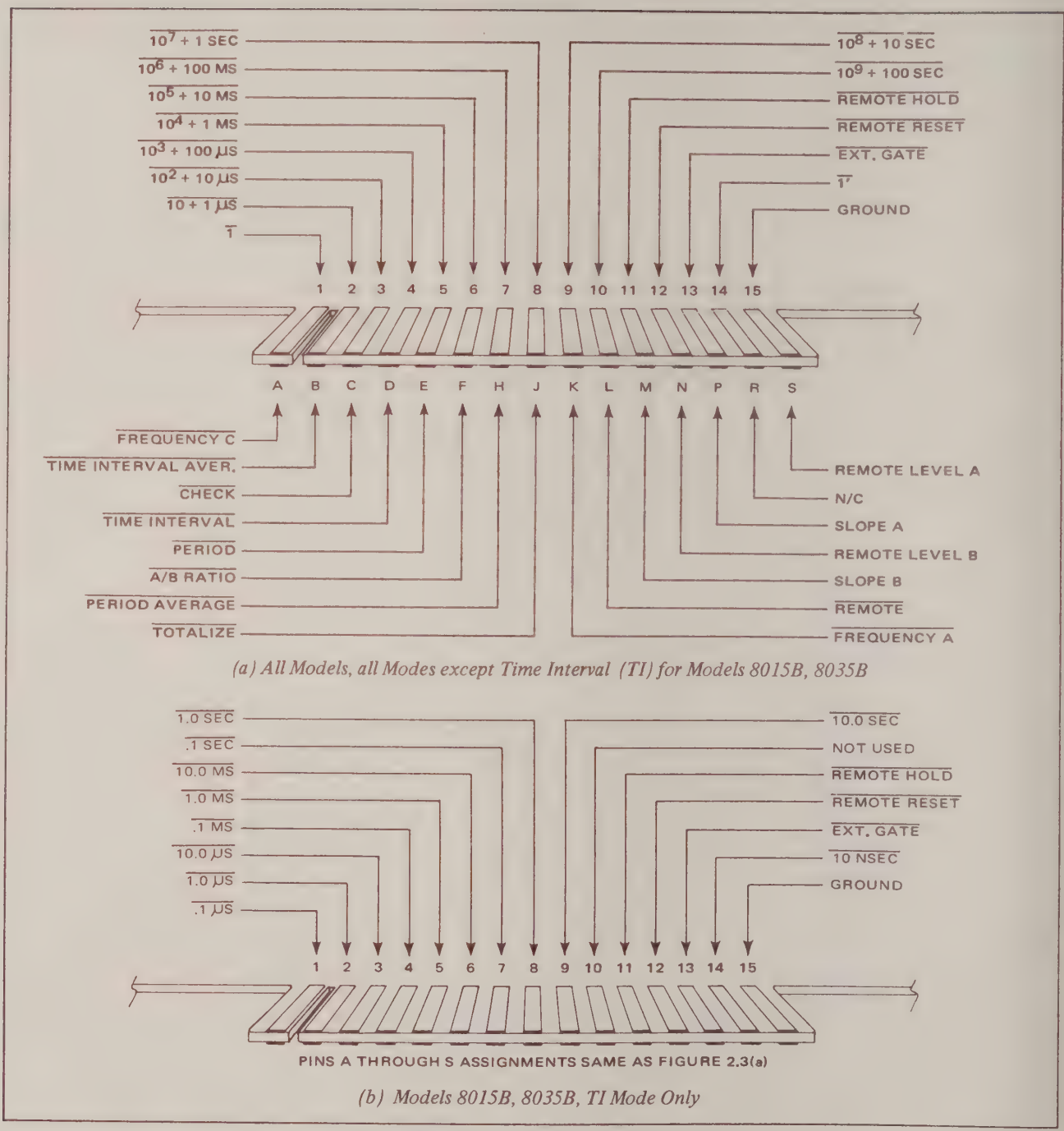
Output	Designator	Connector	Pin No.	Output	Designator	Connector	Pin No.
Numeric	V1-1	J111	1	Numeric	V7-4	J111	P
	V1-2		2		V7-8		R
	V1-4		A		V8-1		15
	V1-8		B		V8-2	J112	1
	V2-1		3		V8-4	J111	S
	V2-2		4		V8-8	J112	A
	V2-4		C		V9-1		2
	V2-8		D		V9-2		3
	V3-1		5		V9-4		B
	V3-2		6		V9-8		C
	V3-4		E	Decimal	DP-1	J112	4
	V3-8		F		DP-2		5
	V4-1		7		DP-3		6
	V4-2		8		DP-4		7
	V4-4		H		DP-5		8
	V4-8		J		DP-6		9
	V5-1		9		DP-7		10
	V5-2		10		DP-8		7
	V5-4		K	Unit	MHz	J112	D
	V5-8		L		kHz		E
	V6-1		11		SEC		F
	V6-2		12		MSEC		H
	V6-4		M		NSEC		J
	V6-8		N		μSEC		K
	V7-1		13	Other	PRINT	J112	S
	V7-2		14		ONE REF.		15
					ZERO REF.		14

2.15 ONE REFERENCE.

2.16 The one reference is provided for those recorders requiring a reference voltage. The line supplies approximately +2.5 volts with an impedance of 1 kilohm ±5%.

2.17 ZERO REFERENCE.

2.18 Zero reference is the recorder common line to which all of the other output lines are referenced.



(a) All Models, all Modes except Time Interval (TI) for Models 8015B, 8035B

(b) Models 8015B, 8035B, TI Mode Only

Figure 2.3 - REMOTE Connector J110 Pin Assignments

2.19 REMOTE PROGRAMMING, 008.

2.20 The Option 008 REMOTE input is connector J110, located on the rear panel of the instrument. A slot between pins 1 and 2 of the edge-type connector is provided for the keying of the mating connector (Dana P/N 600698), supplied with the instrument.

2.21 Remote programming commands are received through the remote connector and are generated by a

Table 2.2 - 008 Programming Cabling Guide

Input	Designator	J110 Pin No.	Mode
Function	$\overline{\text{Freq. C}}$	A	Single Line
	$\overline{\text{TI Ave.}}$	B	
	$\overline{\text{Check}}$	C	
	$\overline{\text{TI}}$	D	
	$\overline{\text{Period}}$	E	
	$\overline{\text{A/B Ratio}}$	F	
	$\overline{\text{Period Avg.}}$	H	
	$\overline{\text{Totalize}}$	J	
	$\overline{\text{Freq A}}$	K	
Signal In	Slope A	P	
	Level A	S	Analog
	Slope B	M	Single Line
	Level B	N	Analog
Time Base All Functions/ Models except TI of 8015B, 8035B	$\overline{1'}$	14	Single Line
	$\overline{1}$	1	
	$\overline{10+1\ \mu s}$	2	
	$\overline{10^2+10\ \mu s}$	3	
	$\overline{10^3+100\ \mu s}$	4	
	$\overline{10^4+1\ ms}$	5	
	$\overline{10^5+10\ ms}$	6	
(Time Base 'Std.' cont.)	$\overline{10^6+100\ ms}$	7	Single Line
	$\overline{10^7+1\ sec}$	8	
	$\overline{10^8+10\ sec}$	9	
	$\overline{10^9+100\ sec}$	10	
Time Base (for TI of 8015B, 8035B only)	$\overline{10\ ns}$	14	
	$\overline{100\ ns}$	1	
	$\overline{1\ \mu s}$	2	
	$\overline{10\ \mu s}$	3	
	$\overline{100\ \mu s}$	4	
	$\overline{1\ ms}$	5	
	$\overline{10\ ms}$	6	
	$\overline{100\ ms}$	7	
	$\overline{1\ sec}$	8	
	$\overline{10\ sec}$	9	
Other	$\overline{\text{REMOTE}}$	L	
	$\overline{\text{HOLD}}$	11	
	$\overline{\text{RESET}}$	12	
	$\overline{\text{Ext. Gate}}$	13	
	GROUND	15	

closure to the $\overline{\text{REMOTE}}$ line (pin L of J110). Pin assignments of J110 are listed in figure 2.3 and table 2.2. Typical programming timing is shown in figure 2.4. Programming requirements are as follows:

a. Logic "1" is the passive state and is defined as +2 volts to +5 volts.

b. Logic "0" is the command state and is defined as 0 to +0.8 volts.

c. Output of programmer must be able to sink 3 milliamps.

2.22 FUNCTION.

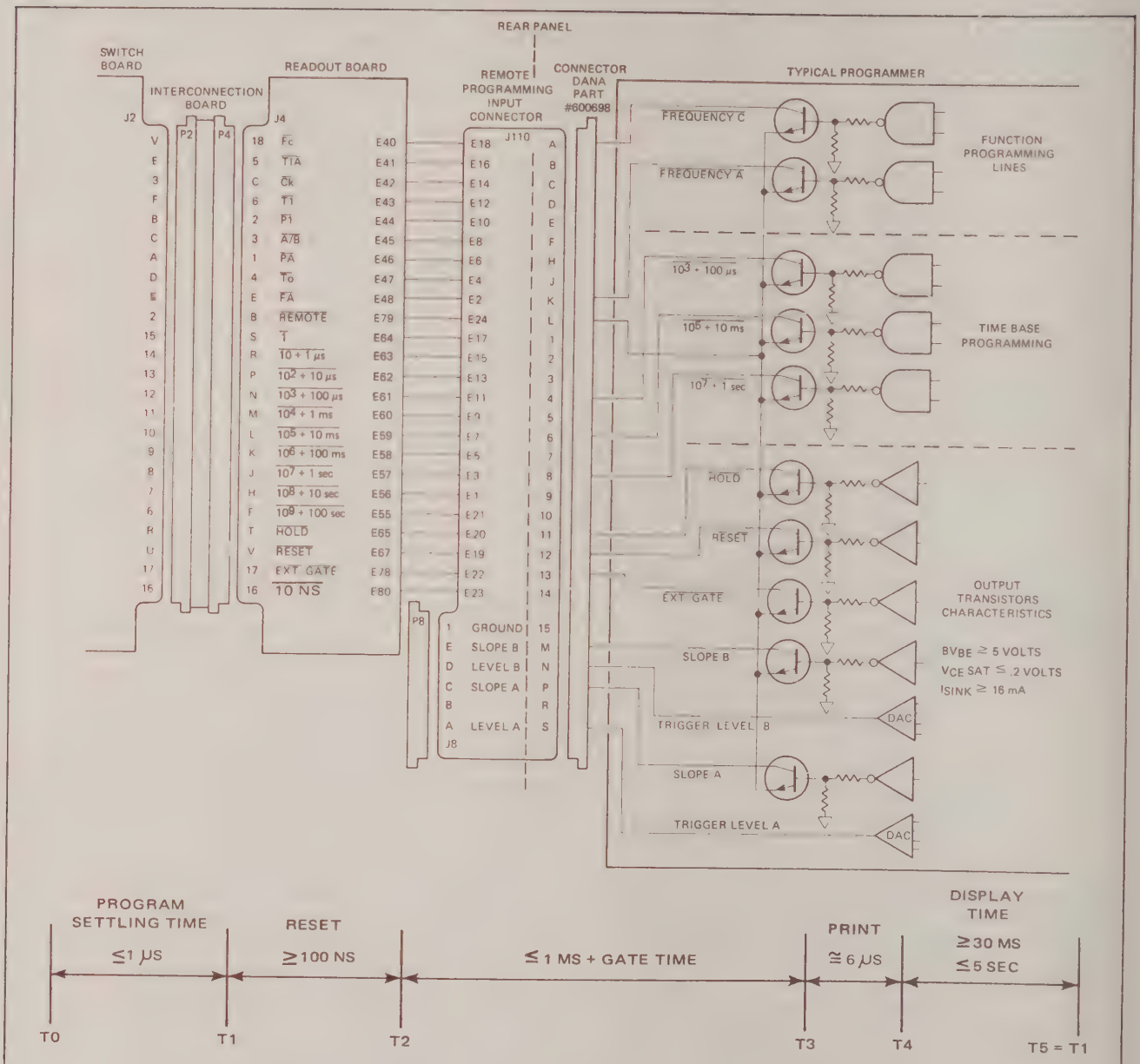
2.23 Pins A through K of J110 are the input lines corresponding to the FUNCTION switch on the front panel. Note that the function lines are the complements of the corresponding function as indicated by a bar over the name. For example: with FREQ A function selected the line marked Freq A should be low ($\overline{\text{Freq A}}$). To remotely program any of the operating modes, the front panel FUNCTION switch must be in the REMOTE position. The function is then programmed by a closure to J110 - pin L from the appropriate pin. Settling time for the function lines are 100 ns.

2.24 MULTIPLIER TIME BASE.

2.25 Pins 1 through 10 of J110 are lines corresponding to each of the MULTIPLIER/TIME BASE pushbutton switches. Settling time for the Multiplier Time Base lines is 100 ns.

2.26 INPUT CONTROLS.

2.27 The INPUT CONTROLS and the "+/−" slope switch on the front panel are duplicated by lines on pins M through S of J110. For remote programming of these input controls, the trigger level for input A and B must be in the PRESET



T0	Select function, multiplier time base, slope, trigger level. The following are set internally: units, decimal point and the arm flip-flop.
T0 - T1	Time for inputs to settle ≤100 ns; trigger levels ≤1 μs.
T1 - T2	Reset or external gate time ≥100 ns.
T2 - T3	≤1 ms + gate time, gate opens, counts accumulate in the counter, gate closes, display flip-flop is reset, arm flip-flop cleared and fires a 1 μsec delay for update.
T3 - T4	Print pulse External Hold takes effect if applied.
T4 - T5	Display time times out ≥30 ms to ≤5 sec selectable on front panel.

Figure 2.4 - Typical Programmer and Timing Diagram

position. The channel A trigger level is then controlled by the voltage applied to J110, pin S; channel B trigger level is controlled by the voltage applied to pin N. The value of the external trigger level voltage applied to pins S and N can be calculated according to the following formula.

$$Vp = 10 \frac{TL}{R}$$

Where: Vp = external trigger level voltage
TL = desired trigger level
R = input voltage range

Example 1: to obtain a trigger level of .7 volts on the 1 volt range.

$$Vp = 10 \frac{.7}{1} = 7 \text{ volts to pin S or N}$$

Example 2: to obtain a trigger level of –50 volts on the 100 volt range.

$$Vp = 10 \frac{-50}{100} = -5 \text{ volts}$$

2.28 Both positive and negative trigger levels may be programmed into pins S or N. Settling time is 1 microsecond for the trigger level up to ±300% of the input range.

2.29 SLOPE.

2.30 The counter triggers on the positive slope unless there is a closure from pin M to pin L for channel B slope or (and) pin P to pin L for channel A slope. With a closure, a negative slope is programmed. Settling time is less than 1 microsecond.

2.31 HOLD.

2.32 The Hold line, pin 11 of J110, corresponds to the full clockwise position of the DISPLAY TIME control on the front panel. When the Hold line is low, the counter takes one reading and holds the measurement until the Reset is activated.

2.33 RESET.

2.34 Reset corresponds to the front panel RESET switch. The reset must be held low for a minimum of 100 nanoseconds. The main gate opens in less than 1 millisecond after the positive edge of the reset closure.

2.35 EXTERNAL GATE.

2.36 The external gate line, pin 13 of J110, is used in the Totalize mode to externally establish a gate time during which Frequency A is counted. The external gate must be greater than 100 nanoseconds. Two contact closures are required per gate time or measurement. The gate is initiated in less than 50 nanoseconds after the falling edge of the first contact closure. The next contact closure terminates the gate and holds the accumulated reading. The next external gate continues the count and so on. The count may be cleared by pulling the Reset line low.

2.37 REMOTE PROGRAMMING, 009 (8010B, 8015B, 8030B, 8035B).

2.38 The Option 009 enables external electrical operation of all front panel controls (except POWER and DISPLAY TIME) and provides BCD output data including numeric value, annunciator and decimal position. All inputs* and outputs are in the form of logic levels with logic "1" levels defined as +2 volts to +5 volts and logic "0" levels defined as 0 volts to 0.8 volts.

2.39 Programming data is applied through a 50-pin blue ribbon connector (J113), located on the rear panel. All command lines* are initially biased at a logic "1" level, control settings are made by 'pulling' the appropriate control lines to GROUND (J113, pin 33). Pin locations are indicated in figure 2.5 and table 2.3.

2.40 System Control.

2.41 The $\overline{\text{SYSTEM CONTROL}}$ line (pin 37 of connector J113) programs remote operation when placed at logic 0 (pin 33 of J113); all front panel controls are inhibited (except POWER and DISPLAY TIME) when system control is selected. When system control is not selected, the instrument can be placed in remote operation by setting the front panel FUNCTION switch to the REMOTE position.

2.42 FUNCTION.

2.43 The remote selection of function is made by applying a binary code to the four function command lines located on J113. The remote selection duplicates the

*except ANALOG TRIGGER LEVEL inputs

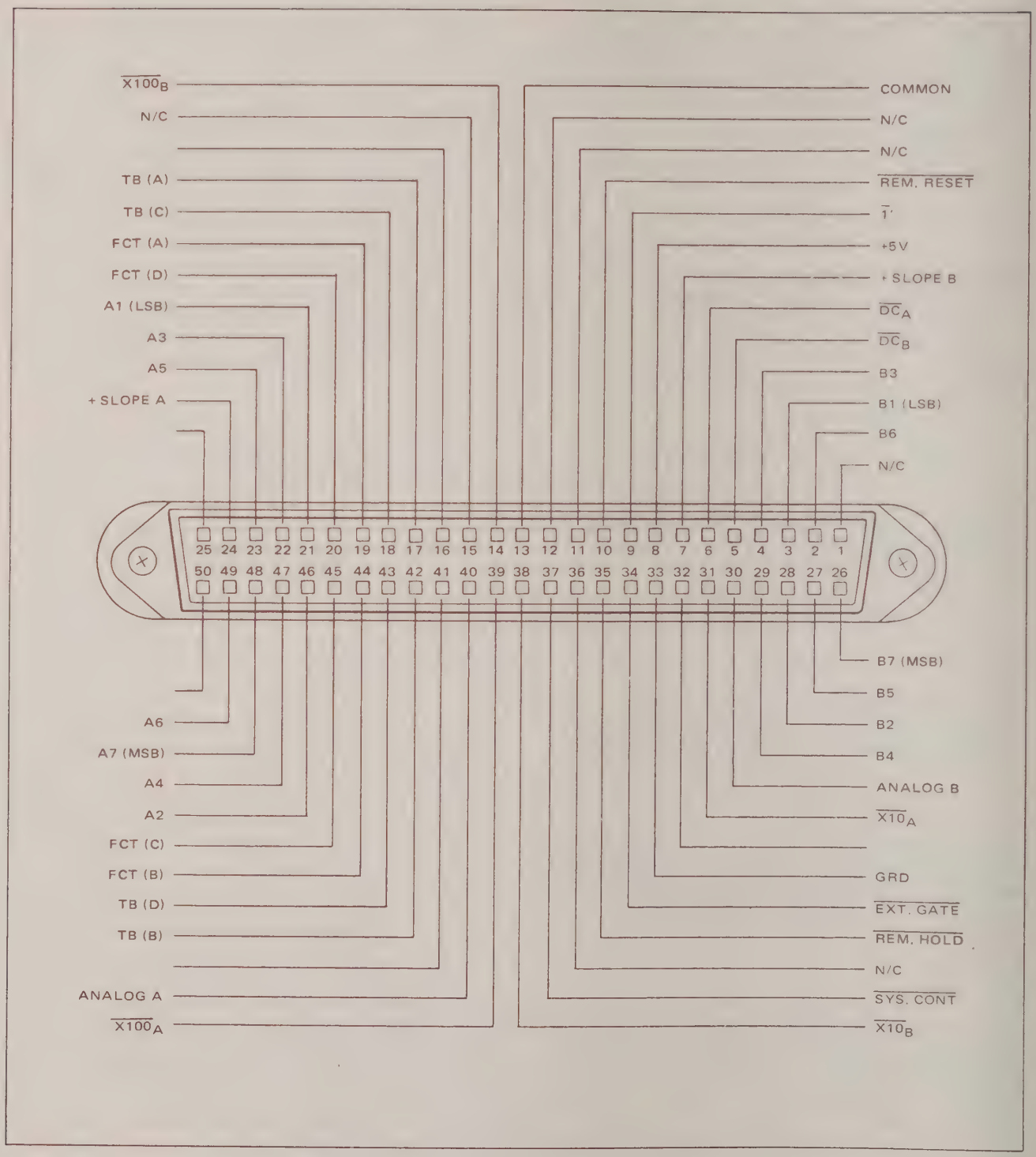


Figure 2.5 - Pin Location of J113 Programming Connector

Table 2.3 - 009 Programming Cabling Guide

Input	Designator	J113 Pin No.	Mode
Function	FCT A	19	4-Line
	FCT B	44	
	FCT C	45	
	FCT D	20	
Time Base	TB A	17	
	TB B	42	
	TB C	18	
	TB D	43	
	$\overline{1'}$	9	Single Line
Sep/Com	Common	13	
A Range	$\overline{X10A}$	31	2-Line
	$\overline{X100A}$	39	
A Slope	+A	24	Single Line
A AC/DC	DC A	6	
A Trigger (Binary)	A_1	21	7-Line
	A_2	46	
	A_3	22	
	A_4	47	
	A_5	23	
	A_6	49	

Input	Designator	J113 Pin No.	Mode
(A Trig cont.)	A7	48	7-Line
A Trig Analog	Analog A	40	Analog
B Range	$\overline{X10B}$	38	2-Line
	$\overline{X100B}$	14	
B Slope	+B	7	Single Line
B AC/DC	DC B	5	
B Trigger (Binary)	B_1	3	7-Line
	B_2	28	
	B_3	4	
	B_4	29	
	B_5	27	
	B_6	2	
	B_7	26	
B Trig Analog	Analog B	30	Analog
Other	$\overline{RESET}$	10	Single Line
	$\overline{HOLD}$	35	
	$\overline{System\ Contrl}$	37	
	$\overline{External\ Gate}$	34	
	+5 Volts	8	
	GROUND	33	

operation of the front panel FUNCTION switch. Coding for each function is shown below.

Function	J113 Pin No. 20	45	44	19	BCD Weight
Check	0	0	0	0	0
Periodic	0	0	0	1	1
Periodic Avg	0	0	1	0	2
Frequency A	0	0	1	1	3
Frequency C	0	1	0	0	4
Total	0	1	0	1	5
Time Interval	0	1	1	0	6
A/B Ratio	0	1	1	1	7
Time Interval Avg	1	0	0	0	8

2.44 MULTIPLIER TIME BASE.

2.45 The remote selection of the multiplier time base is made by applying a binary code to the four time base command lines located on J113. The remote selection duplicates the operation of the front panel pushbuttons. Coding for each time base is shown below.

Timebase	J113 Pin No. 43	18	42	17	BCD Weight
1 + 100 ns	0	0	0	0	0
10 + 1 μs	0	0	0	1	1
10^2 + 10 μs	0	0	1	0	2
10^3 + 100 μs	0	0	1	1	3
10^4 + 1 ms	0	1	0	0	4
10^5 + 10 ms	0	1	0	1	5
10^6 + 100 ms	0	1	1	0	6
10^7 + 1 sec	0	1	1	1	7
10^8 + 10 sec	1	0	0	0	8
10^9 + 100 sec	1	0	0	1	9

Input code for all functions except TI on 8015B & 8035B

Timebase	J113 Pin No. 43	18	42	17	BCD Weight
100 ns	0	0	0	0	0
1 μs	0	0	0	1	1
10 μs	0	0	1	0	2
100 μs	0	0	1	1	3
1 ms	0	1	0	0	4
10 ms	0	1	0	1	5
100 ms	0	1	1	0	6
1 sec	0	1	1	1	7
10 sec	1	0	0	0	8
10 ns	1	0	0	1	9

Input code for TI on 8015B & 8035B only

2.46 INPUT CONTROLS.

2.47 The remote operation of input controls for channels A and B consists of both single line and binary coded inputs. Coding for the input controls is provided below.

	J113 Pin No.
Separate/Common	13
Separate	1
Common	0

Channel A Range	39	31	BCD Weight
X100	0	1	1
X10	1	0	2
X1	1	1	3

Channel A Slope	J113 Pin No. 24
+	1
–	0

Channel A AC/DC	J113 Pin No. 6
AC	1
DC	0

Channel A Trigger Level	J113 Pin No. 48*	49	23	47	22	46	21
	Codes provided in table 2.4						

*Most Significant Bit

Channel B Range	14	38	BCD Weight
X100	0	1	1
X10	1	0	2
X1	1	1	3

Channel B Slope	J113 Pin No. 7
+	1
–	0

Channel B AC/DC	J113 Pin No. 5
AC	1
DC	0

Channel B Trigger Level	J113 Pin No. 26*	2	27	29	4	28	3
	Codes provided in table 2.4						

*Most Significant Bit

2.48 HOLD.

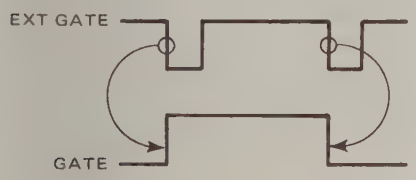
2.49 The Hold line, pin 35 of J113, corresponds to the full clockwise position of the DISPLAY TIME control on the front panel. When the Hold line is at logic 0, the counter takes one reading and holds the measurement until the Reset is activated.

2.50 RESET.

2.51 The reset corresponds to the front panel RESET switch. This is a single line control (pin 10 of J113) and is activated when set to logic 0. The line must be held at logic 0 for a minimum of 100 nanoseconds.

2.52 EXTERNAL GATE.

2.53 The external gate line (pin 34 of J113) is used in the Totalize mode to externally establish a gate time during which channel A signal is counted. The external gate command must be greater than 100 nanoseconds. Two commands are required per gate time or measurement. The gate is initiated in less than 50 nanoseconds after the following edge of the first command. The next command terminates the gate and holds the accumulated reading. The next external gate continues the count and so on. The count may be cleared by pulling the Reset line to logic 0.



2.54 TRIGGER LEVEL.

2.55 The trigger levels of channels A and B are capable of being independently set by external control with either an analog voltage level or a binary coded input.

2.56 Analog control of channel A is through pin 40 and control of channel B is through pin 30 of connector J113. Each 0.1 volt of input voltage adjusts the trigger level 1% of the selected range.

Example: A trigger level of −30 volts is desired.

1. The 100 range is selected.

2. The control voltage is equal to:

$$\left(\frac{\text{Desired trigger level}}{\text{Range}}\right) \times 10$$

3. Or: $\left(\frac{-30 \text{ volts}}{100}\right) \times 10$

4. Therefore the required control level is −3 volts.

The input impedance of the analog trigger level control inputs is 10 kilohms.

2.57 Digital control of the trigger levels for channels A and B requires the generation of digital command words for each channel. A separate command word is required for each level and 128 separate levels are available for each channel. Each command word consists of a 7-bit binary code. The available digitally programmable trigger levels along with the required 7-bit code is provided in table 2.4. Note that the available trigger levels listed in table 2.4 indicate the value of the analog signal generated within the instrument for each command word. To equate the available trigger level with the desired trigger level, the available trigger level value is multiplied by the range selected.

2.58 Also included in table 2.4 is the decimal representation for each trigger level. This value can be computed directly from the value of the trigger level by the relationship:

$$\text{Decimal Value} = 63 - 20\left(\frac{\text{Desired trigger level}}{\text{Range}}\right)$$

Example: A trigger level of +5 volts is desired.

1. Select the 10 volt range.

2. The decimal value is then equal to:

$$63 - 20\left(\frac{+5 \text{ Volts}}{10}\right)$$

3. The decimal value is 53.

4. From table 2.4, decimal value 53 is equal to +0.500 (available trigger level). +0.5 times the 10 range equals the desired +5 volts trigger level.

Table 2.4 - Trigger Level DAC Programming Information

Desired Trigger Level (VDC)	COMMAND WORD			
	Binary	Octal	Decimal	Hexidecimal
+3.150	0 000 000	000	000	00
+3.100	0 000 001	001	001	01
+3.050	0 000 010	002	002	02
+3.000	0 000 011	003	003	03
+2.950	0 000 100	004	004	04
+2.900	0 000 101	005	005	05
+2.850	0 000 110	006	006	06
+2.800	0 000 111	007	007	07
+2.750	0 001 000	010	008	08
+2.700	0 001 001	011	009	09
+2.650	0 001 010	012	010	0A
+2.600	0 001 011	013	011	0B
+2.550	0 001 100	014	012	0C
+2.500	0 001 101	015	013	0D
+2.450	0 001 110	016	014	0E
+2.400	0 001 111	017	015	0F
+2.350	0 010 000	020	016	10
+2.300	0 010 001	021	017	11
+2.250	0 010 010	022	018	12
+2.200	0 010 011	023	019	13
+2.150	0 010 100	024	020	14
+2.100	0 010 101	025	021	15
+2.050	0 010 110	026	022	16
+2.000	0 010 111	027	023	17
+1.950	0 011 000	030	024	18
+1.900	0 011 001	031	025	19
+1.850	0 011 010	032	026	1A
+1.800	0 011 011	033	027	1B
+1.750	0 011 100	034	028	1C
+1.700	0 011 101	035	029	1D
+1.650	0 011 110	036	030	1E
+1.600	0 011 111	037	031	1F
+1.550	0 100 000	040	032	20
+1.500	0 100 001	041	033	21

Table 2.4 - Trigger Level DAC Programming Information (continued)

Desired Trigger Level (VDC)	COMMAND WORD			
	Binary	Octal	Decimal	Hexidecimal
+1.450	0 100 010	042	034	22
+1.400	0 100 011	043	035	23
+1.350	0 100 100	044	036	24
+1.300	0 100 101	045	037	25
+1.250	0 100 110	046	038	26
+1.200	0 100 111	047	039	27
+1.150	0 101 000	050	040	28
+1.100	0 101 001	051	041	29
+1.050	0 101 010	052	042	2A
+1.000	0 101 011	053	043	2B
+0.950	0 101 100	054	044	2C
+0.900	0 101 101	055	045	2D
+0.850	0 101 110	056	046	2E
+0.800	0 101 111	057	047	2F
+0.750	0 110 000	060	048	30
+0.700	0 110 001	061	049	31
+0.650	0 110 010	062	050	32
+0.600	0 110 011	063	051	33
+0.550	0 110 100	064	052	34
+0.500	0 110 101	065	053	35
+0.450	0 110 110	066	054	36
+0.400	0 110 111	067	055	37
+0.350	0 111 000	070	056	38
+0.300	0 111 001	071	057	39
+0.250	0 111 010	072	058	3A
+0.200	0 111 011	073	059	3B
+0.150	0 111 100	074	060	3C
+0.100	0 111 101	075	061	3D
+0.050	0 111 110	076	062	3E
0.000	0 111 111	077	063	3F
–0.050	1 000 000	100	064	40
–0.100	1 000 001	101	065	41
–0.150	1 000 010	102	066	42
–0.200	1 000 011	103	067	43

Table 2.4 - Trigger Level DAC Programming Information (continued)

Desired Trigger Level (VDC)	COMMAND WORD			
	Binary	Octal	Decimal	Hexidecimal
-0.250	1 000 100	104	068	44
-0.300	1 000 101	105	069	45
-0.350	1 000 110	106	070	46
-0.400	1 000 111	107	071	47
0.450	1 001 000	110	072	48
0.500	1 001 001	111	073	49
-0.550	1 001 010	112	074	4A
-0.600	1 001 011	113	075	4B
-0.650	1 001 100	114	076	4C
0.700	1 001 101	115	077	4D
-0.750	1 001 110	116	078	4E
-0.800	1 001 111	117	079	4F
-0.850	1 010 000	120	080	50
0.900	1 010 001	121	081	51
-0.950	1 010 010	122	082	52
-1.000	1 010 011	123	083	53
-1.050	1 010 100	124	084	54
-1.100	1 010 101	125	085	55
-1.150	1 010 110	126	086	56
-1.200	1 010 111	127	087	57
-1.250	1 011 000	130	088	58
-1.300	1 011 001	131	089	59
-1.350	1 011 010	132	090	5A
-1.400	1 011 011	133	091	5B
-1 450	1 011 100	134	092	5C
-1.500	1 011 101	135	093	5D
-1.550	1 011 110	136	094	5E
-1.600	1 011 111	137	095	5F
-1.650	1 100 000	140	096	60
-1.700	1 100 001	141	097	61
-1.750	1 100 010	142	098	62
-1.800	1 100 011	143	099	63
-1.850	1 100 100	144	100	64
-1.900	1 100 101	145	101	65

Table 2.4 - Trigger Level DAC Programming Information (continued)

Desired Trigger Level (VDC)	COMMAND WORD			
	Binary	Octal	Decimal	Hexidecimal
−1.950	1 100 110	146	102	66
−2.000	1 100 111	147	103	67
−2.050	1 101 000	150	104	68
−2.100	1 101 001	151	105	69
−2.150	1 101 010	152	106	6A
−2.200	1 101 011	153	107	6B
−2.250	1 101 100	154	108	6C
−2.300	1 101 101	155	109	6D
−2.350	1 101 110	156	110	6E
−2.400	1 101 111	157	111	6F
−2.450	1 110 000	160	112	70
−2.500	1 110 001	161	113	71
−2.550	1 110 010	162	114	72
−2.600	1 110 011	163	115	73
−2.650	1 110 100	164	116	74
−2.700	1 110 101	165	117	75
−2.750	1 110 110	166	118	76
−2.800	1 110 111	167	119	77
−2.850	1 111 000	170	120	78
−2.900	1 111 001	171	121	79
−2.950	1 111 010	172	122	7A
−3.000	1 111 011	173	123	7B
−3.050	1 111 100	174	124	7C
−3.100	1 111 101	175	125	7D
−3.150	1 111 110	176	126	7E
−3.200	1 111 111	177	127	7F

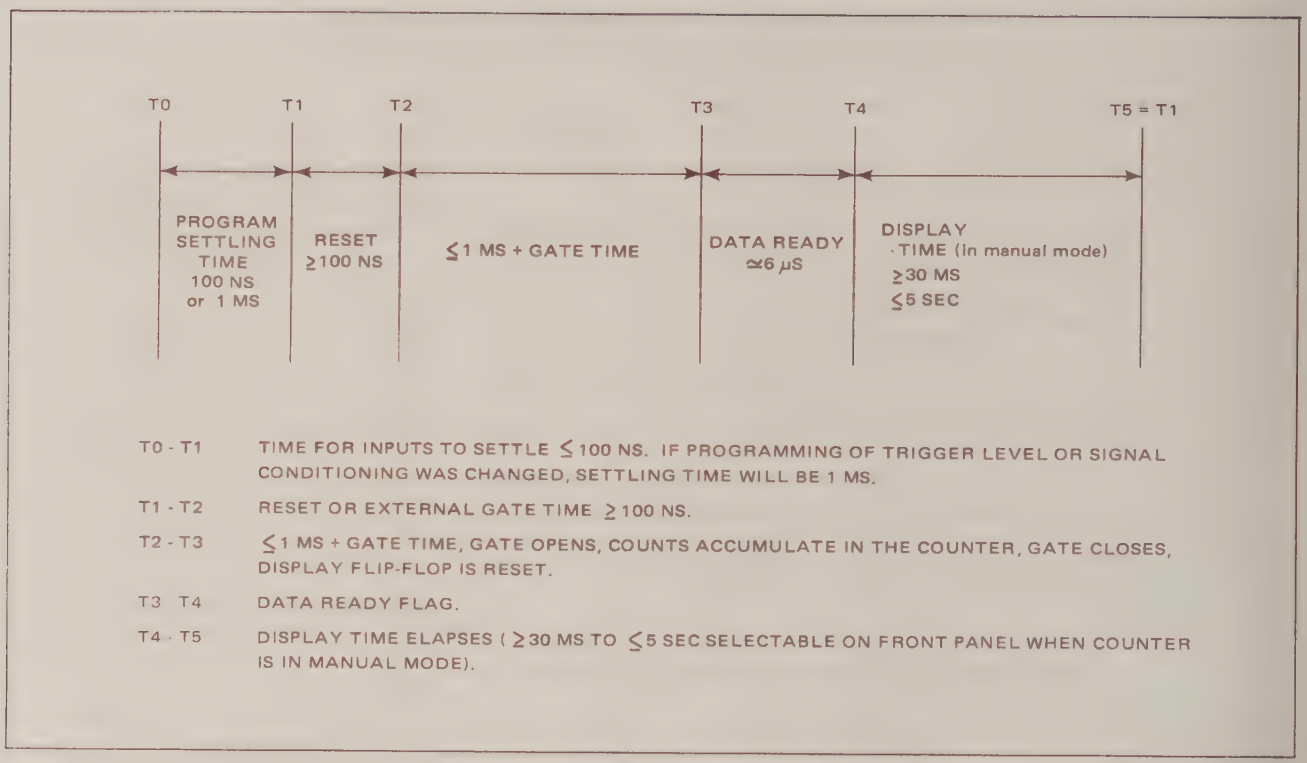

T0
T1
T2
T3
T4
T5 = T1
PROGRAM SETTLING TIME 100 NS or 1 MS
RESET ≥100 NS
≤1 MS + GATE TIME
DATA READY ≃6 μS
DISPLAY TIME (In manual mode) ≥30 MS ≤5 SEC
T0 - T1 TIME FOR INPUTS TO SETTLE ≤100 NS. IF PROGRAMMING OF TRIGGER LEVEL OR SIGNAL CONDITIONING WAS CHANGED, SETTLING TIME WILL BE 1 MS.
T1 - T2 RESET OR EXTERNAL GATE TIME ≥100 NS.
T2 - T3 ≤1 MS + GATE TIME, GATE OPENS, COUNTS ACCUMULATE IN THE COUNTER, GATE CLOSES, DISPLAY FLIP-FLOP IS RESET.
T3 T4 DATA READY FLAG.
T4 - T5 DISPLAY TIME ELAPSES (≥30 MS TO ≤5 SEC SELECTABLE ON FRONT PANEL WHEN COUNTER IS IN MANUAL MODE).

Figure 2.6 - Simplified Timing Diagram

2.59 Programming Sequence.

2.60 For computer-controlled operation the switch positions on the instrument front and rear panels should be set as indicated below.

Front Panel:

Function	REMOTE
Display Time	Any position
Time Base/Multiplier	Any position

Channel A and Channel B
Input Controls

Slope	Either position
AC/DC	Either position
Attenuators	Any position
Level	Any position
Sep/Com	Either position

Rear Panel:

Storage	ON
Ref	INT

2.61 TIMING.

2.62 Required information on timing for programming the instrument are provided in figure 2.6.

2.63 Local Control

2.64 When operating instruments equipped with the 009, option in local control, some remote lines are still capable of affecting instrument operation. These lines, shown below, should be allowed to float high while operating in local control to avoid interaction between the local and remote inputs.

J113 PIN	DESIGNATOR	J113 PIN	DESIGNATOR	NOTE
6	DCA	38	$\overline{\text{X10B}}$	All lines to remain floating when operating in local control
5	DCB	14	$\overline{\text{X100B}}$	
31	$\overline{\text{X10A}}$	34	$\overline{\text{External Gate}}$	
39	$\overline{\text{X100A}}$	10	$\overline{\text{RESET}}$	
13	Common	35	$\overline{\text{HOLD}}$	

SECTION 3 THEORY OF OPERATION

3.1 GENERAL.

3.2 The basic flow of information between the Series 8000B Counter and each of the interface options is shown in simplified form in figure 3.1. This figure and others in this section are provided as reference for the text and supplement the schematic drawings at the back of this manual and the Counter manual.

3.3 RECORDER.

3.4 The recorder output, in both options, is taken directly from the Readout Assembly. Physically, it consists of a cable from the readout to connectors J111 and J112 of the rear panel. Electrically, the output is taken from TTL integrated logic outputs. These outputs are also used to drive other logic on the Readout assembly. Typical Recorder drive circuits are shown in figure 3.2 and described in the following paragraphs.

3.5 Display.

3.6 The display output is supplied by eight sets of 4-line BCD output lines (or nine sets in instruments equipped with the 004 option). The lines are driven by the 7475 latches which also drive the BCD to 10-line converters.

3.7 Annunciators.

3.8 The annunciator data is carried on six individual lines, taken from inverter or logic gate outputs. These also control the annunciator drivers (Q5, Q6, Q7, Q8, Q9, and Q10).

3.9 Decimal.

3.10 The decimal output consists of eight single-line outputs taken from logic gate and inverter outputs that feed the decimal drivers of the display (Q15, Q17, Q18, Q19, Q20, Q21, Q22, and Q23).

3.11 Print.

3.12 The print line is picked up on the readout board at terminal E66 but the circuitry generating the signal is located on the switch board as shown in figure 3.3. The circuitry consists of a 6 microsecond one-shot generator. Normally, the output of the circuitry is at logic 0 with both inputs of NAND gate MC6 at logic 1. The falling edge of a positive 1 microsecond pulse, generated by the counter control logic, initiates the positive 6 microsecond print pulse. The 1 microsecond pulse is used by the counter to transfer new data into the display logic at the end of a measurement (update pulse); the print pulse indicates the data transfer is complete.

3.13 Zero Reference.

3.14 The zero reference is the logic 0 or common line. It is the zero reference line for all outputs of the RECORDER connectors J111 and J112.

3.15 One Reference.

3.16 The one reference is an internally generated reference of approximately +2.5 volts and is required by some types of printers. The circuit consists of two 2 Kilohm resistors in series, connected between zero reference and the +5 volt power supply line, with the one reference taken from the junction of the two resistors.

3.17 REMOTE OPERATION (008).

3.18 The option 008 offers remote programming of the function, multiplier/time base, and the slope and trigger level of the input control. Programming is through remote lines or remote circuitry that operate in parallel with existing instrument circuitry. Interaction of local controls by remote inputs is eliminated by switching the remote input lines to the REMOTE line (pin L); the remote inputs will not energize unless the REMOTE line is at logic 0 (when the front panel Function switch is set to REMOTE).

3.19 Remote Function.

3.20 A portion of the remote function control lines and the corresponding front panel function control lines are illustrated in figure 3.4. In all cases except the Remote position, diodes separate the remote input lines from the instrument control lines. The Function switch is shown in the remote position causing the $\overline{\text{REMOTE}}$ line to be at logic 0. Remote lines are energized when they are electrically tied to pin L of J110.

3.21 Remote Multiplier/Time Base.

3.22 Shown in figure 3.5 is a portion of the remote and local control of the multiplier/time base. To prevent front

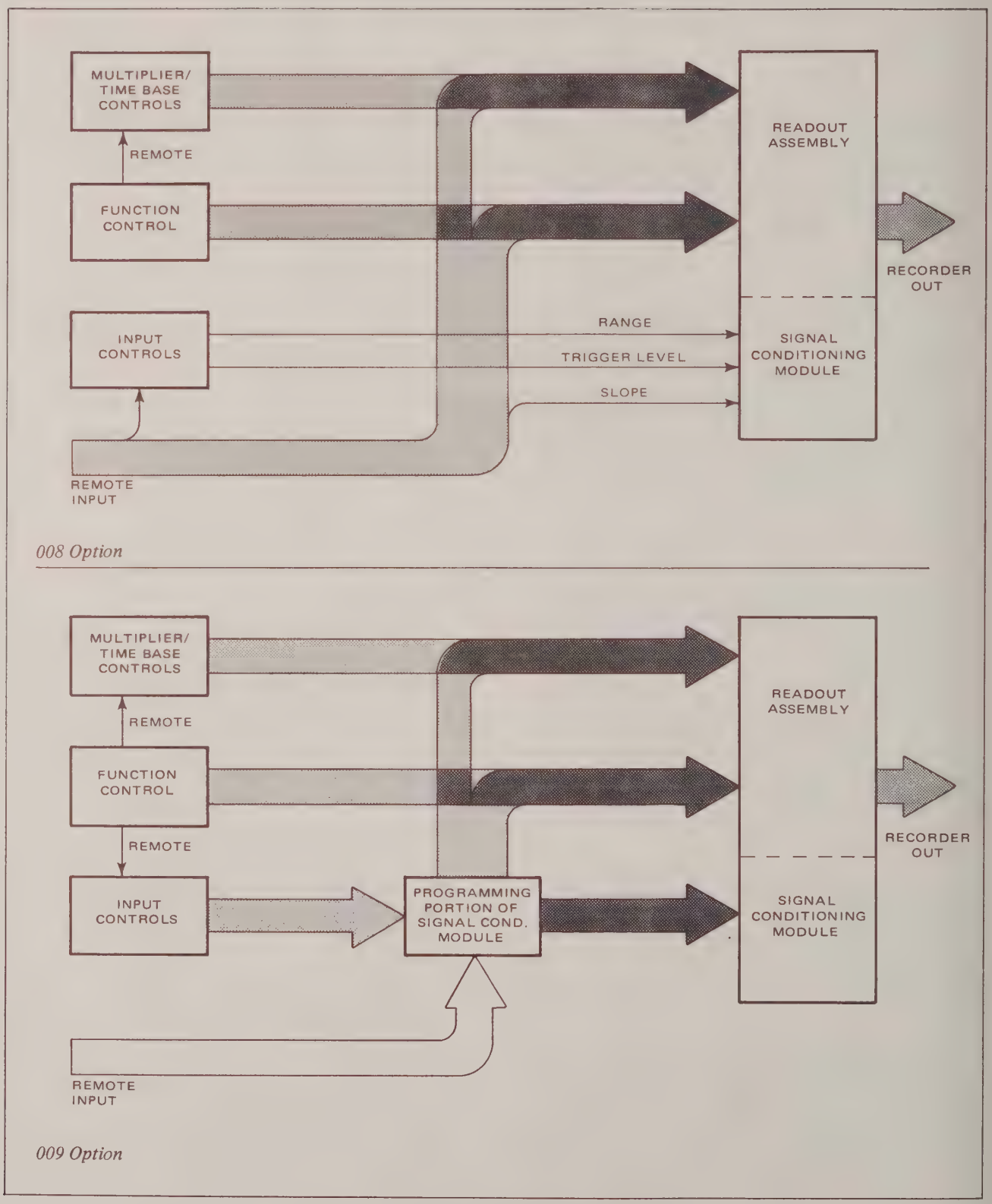


Figure 3.1 - 008/009 Programming, Block Diagram

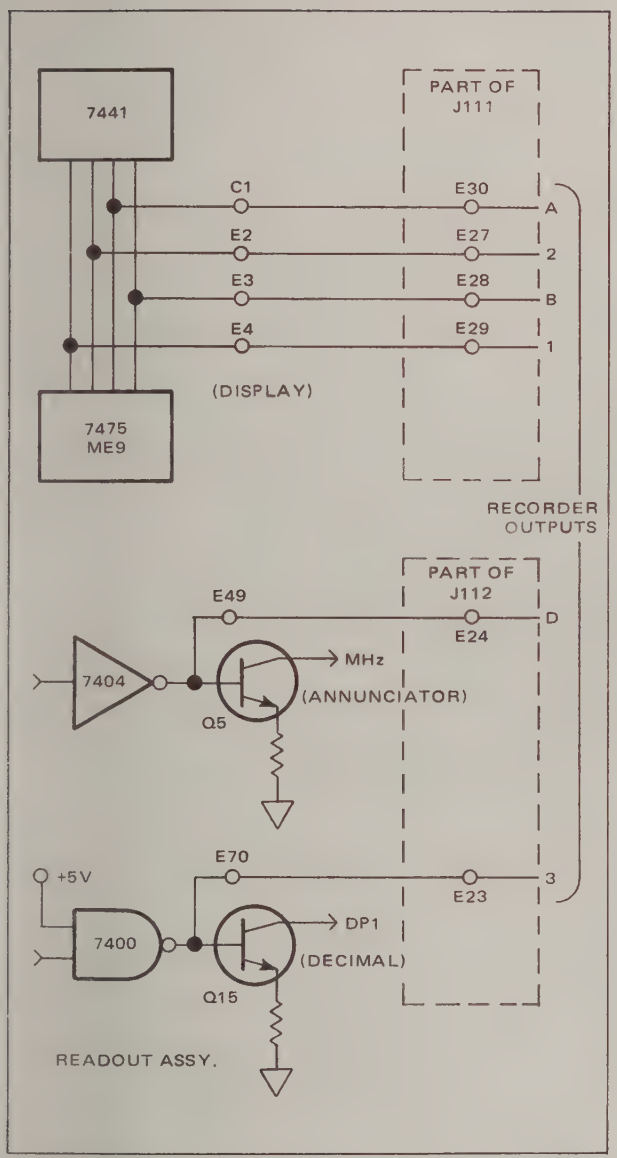


Figure 3.2 - Recorder Output Circuits

panel operation with Remote selected, inverter Q7 output is driven to logic 1, inhibiting the front panel pushbuttons from pulling any of the control lines down. Remote lines are energized when they are electrically tied to pin L of J110.

3.23 Remote Input.

3.24 The remote input (or inputs, depending on the counter model) selects the trigger level and slope of the input signal. The circuitry that controls these operations is part of the basic instrument. It is located on the signal conditioning module, and described in further detail in the 8000B Series manual; the remote programming portions of these circuits are described in the following paragraphs.

3.25 Remote Trigger Levels.

3.26 The remote trigger level circuitry, shown in figure 3.6, consists of a resistor (R27) tying the external control line (J110-S) to the trigger level circuitry. The front panel trigger level control consists of a potentiometer with a built-in switch that opens the circuit in the CCW position (PRESET). The control is placed in the PRESET position when the remote trigger level control is to be used. Because the remote trigger level control line is continuously in the circuit, it is recommended that it be externally opened when local control is used. Resistors R27 and R26 form a 10:1 voltage divider; a maximum input level of 30 volts, therefore, produces an input of 3 volts to the reference input of the amplifier.

3.27 Remote Slope Control.

3.28 The remote slope control is shown in figure 3.7. With remote selected, $\overline{\text{REMOTE}}$ is at logic 0. This causes transistor Q11 to be biased off and prevents the front panel SLOPE switch (S206) from pulling either of the two output lines down. Also, the emitter of transistor Q12 is held at logic 0. With J110-P open, Q12 is biased on through

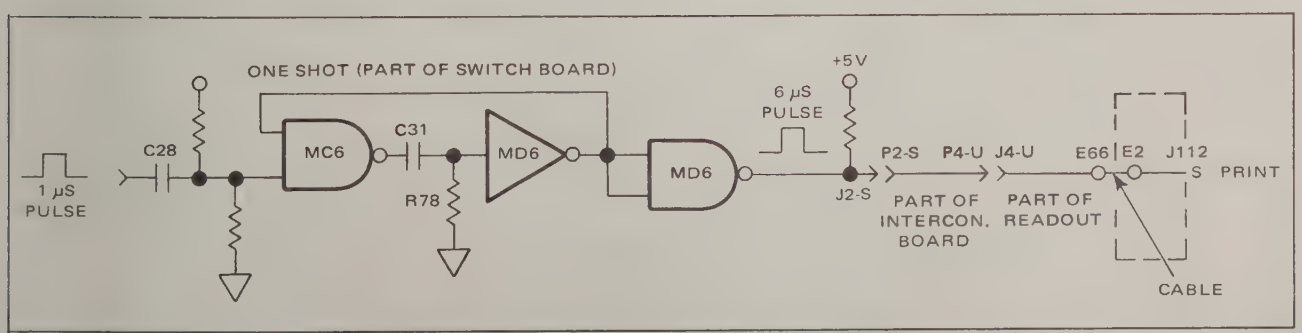


Figure 3.3 - Print Command Circuitry

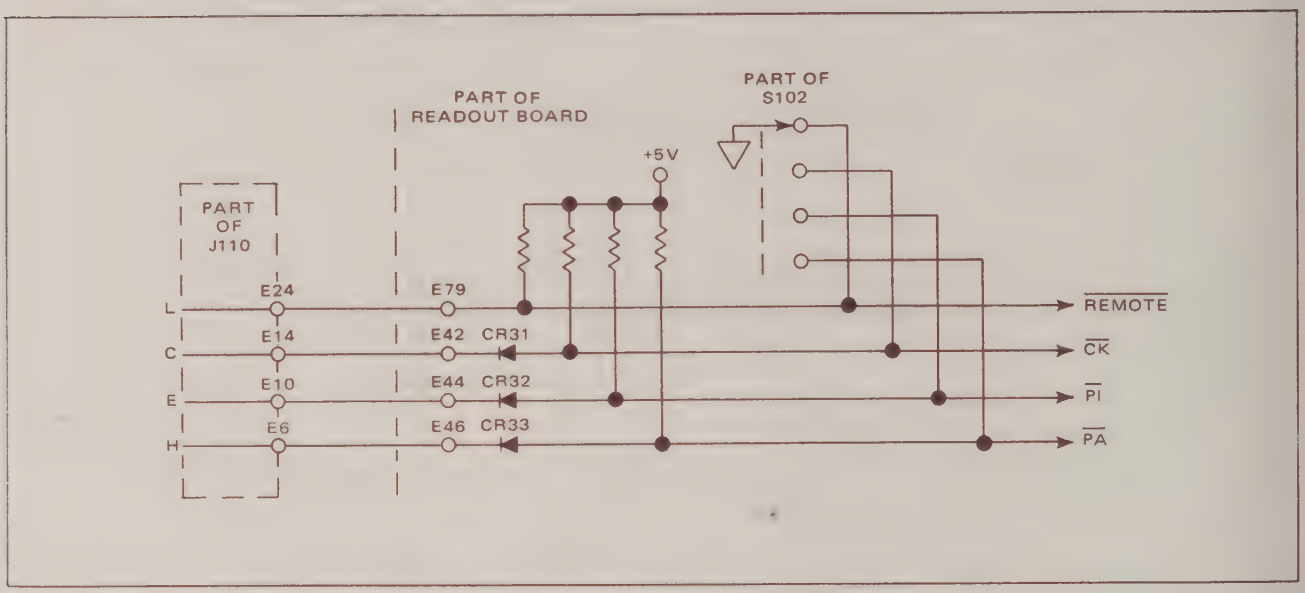


Figure 3.4 - Remote Function Select

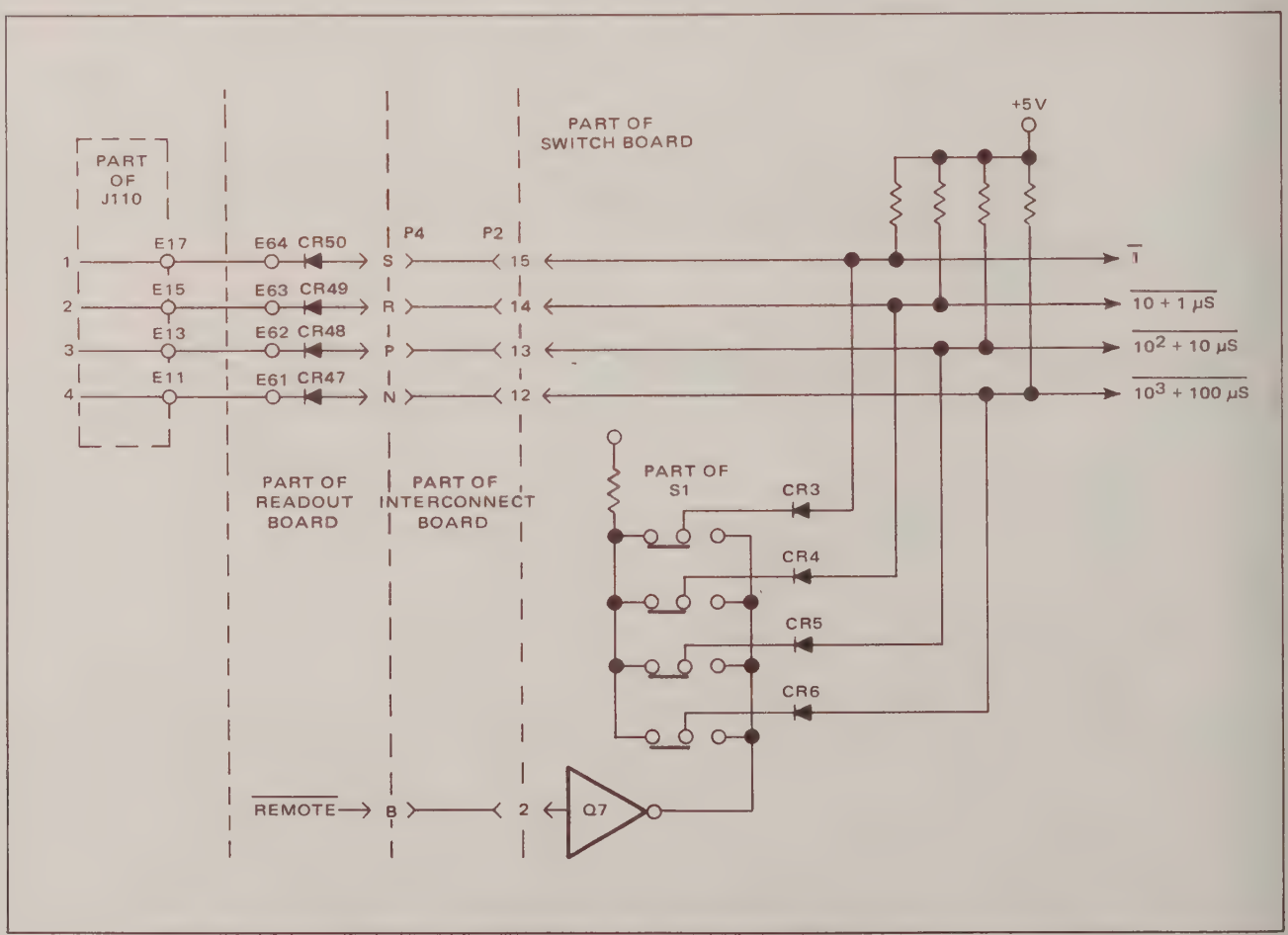


Figure 3.5 - Remote Multiplier/Time Base Select

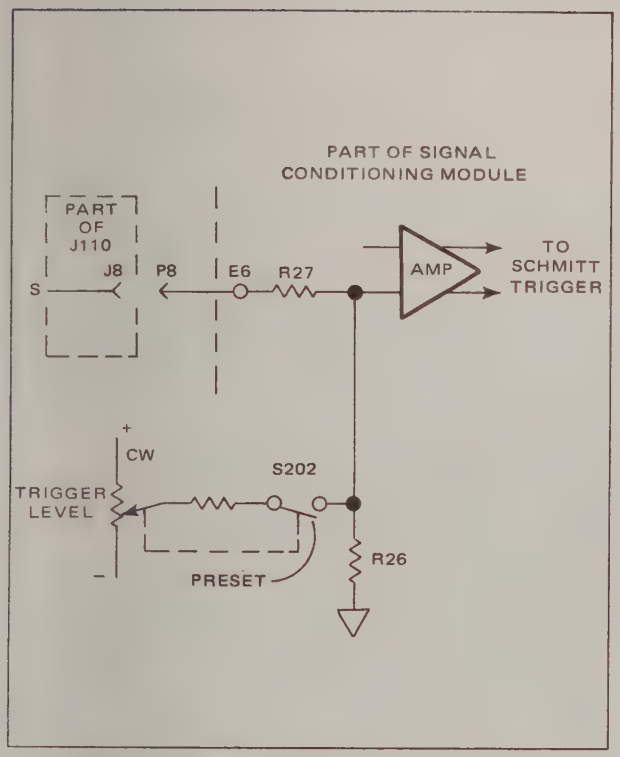


Figure 3.6 - Remote Trigger Level Control (008)

resistors R28, R37, and R32. Q12 thus pulls down the – slope line (inhibiting it) and allowing the signal on the + slope line to reach J6. When J110-P is pulled to logic 0, Q12 is biased off (allowing the – slope line to go positive) and the + slope line is pulled down through R37. The – slope signal is thus allowed to reach J6.

3.29 REMOTE OPERATION, 009.

3.30 The option 009 consists of a special signal conditioning module that replaces the standard conditioning module, a special rear panel that includes a fan, and certain changes in the standard circuitry that will be covered in the text.

3.31 The option offers remote programming of the function, multiplier/time base, and the slope and trigger level of the input control. In addition, it provides digital trigger level control, hysteresis compensation, range control and separate/common select. The option 009 is used on the 8010B, 8015B, 8030B, and the 8035B Series Counters.

3.32 Remote Function.

3.33 The functions are remotely selected by a 4-line, BCD, 1-2-4-8 code. The input lines are routed to a BCD-to-10 line converter located on the 009 Signal Conditioner

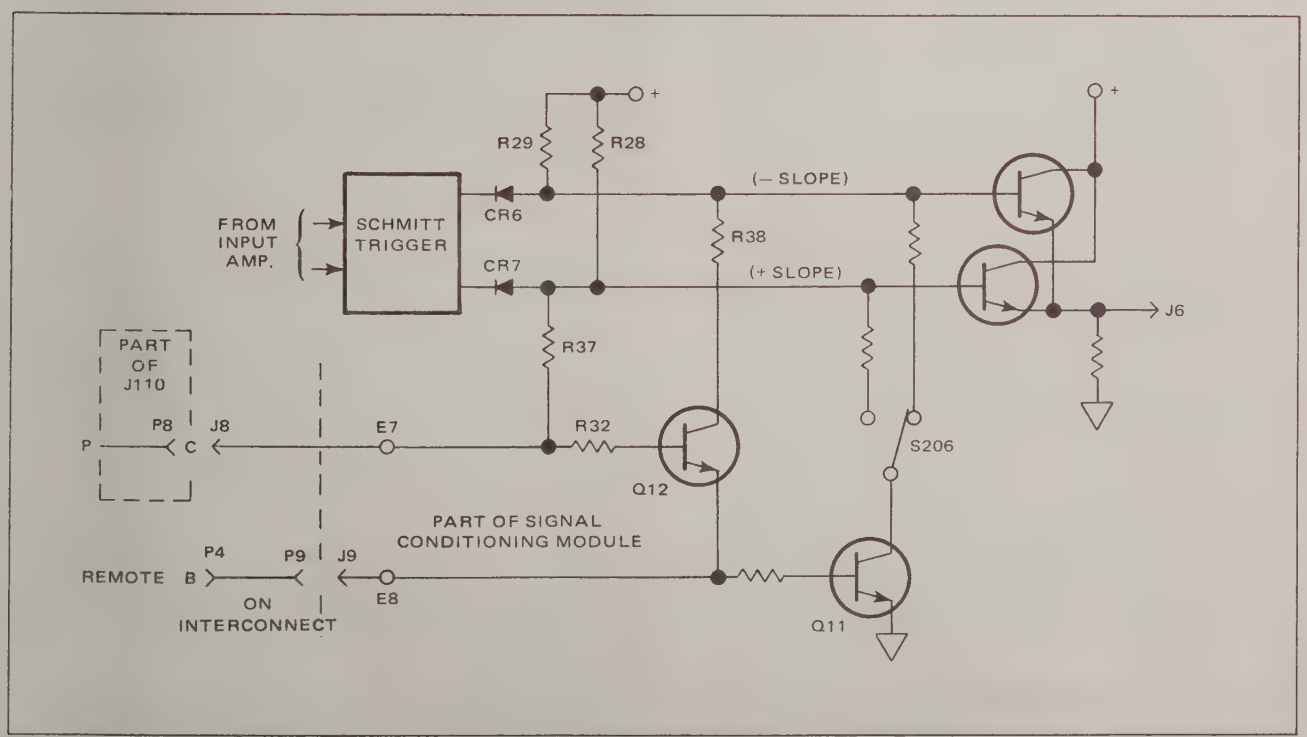


Figure 3.7 - Remote Slope Control (008)

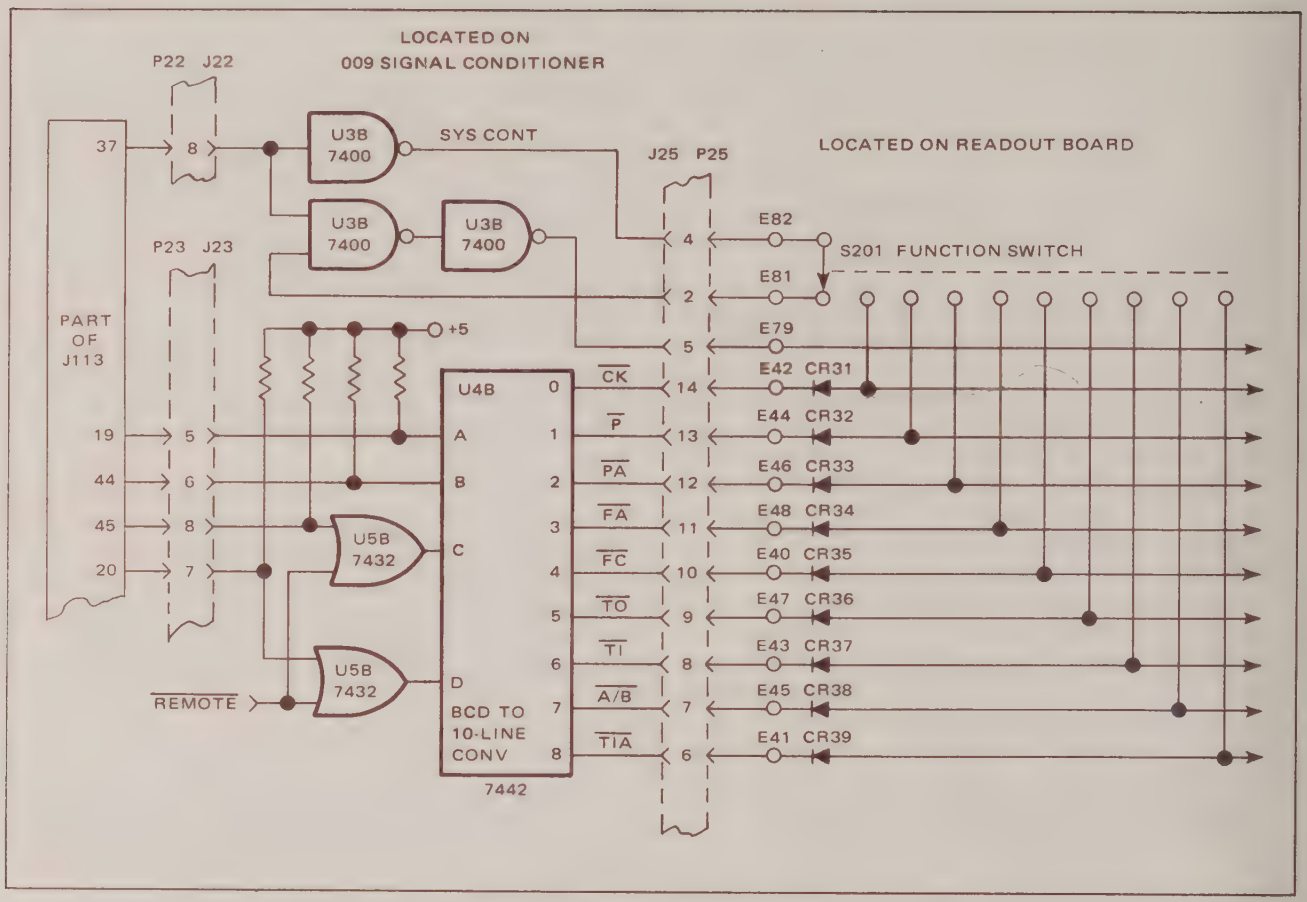


Figure 3.8 - Remote Function Decode

as shown in figure 3.8. With remote selected, the $\overline{\text{REMOTE}}$ signal appearing at the inputs of the two "OR" gates is at logic 0 and does not affect the operation of the converter. The coded function input is decoded to its numeric equivalent and appears as a logic 0 at the specified output terminal.

For Example: the input code for Time Interval (from Section 2) is 20 = 0, 45 = 1, 44 = 1, 19 = 0 for a BCD equivalent weight of 6. This input results in the $\overline{\text{TI}}$ output of the converter (which has a weight of 6) to be at logic 0 and all of the remaining outputs have an output of logic 1. The $\overline{\text{TI}}$ output selects the Time Interval function through diode CR37.

3.34 When Remote is not selected, the $\overline{\text{REMOTE}}$ line at the inputs of the "OR" gates is at logic 1 causing the C and D inputs of the converter to be at logic 1. This places the converter in an "impossible" code state and all output lines are held at logic 1 regardless of what BCD code is introduced at the input.

3.35 Remote Multiplier/Time Base.

3.36 The Multiplier/Time Base (M/TB) is remotely selected by 4-wire BCD 1-2-4-8 code and operates in much the same manner as the remote function selection. The operation of the circuitry as well as operating differences between counter models are described in the following paragraphs.

3.37 8010B, 8030B.

3.38 As shown in figure 3.9 the remote BCD input is converted to 10-line by U4A and routed to the switching board. With remote selected, the $\overline{\text{REMOTE}}$ line is at logic 0. The two 'OR' gates (7432) are not affected but switch S1 is disabled (the logic 0 of the $\overline{\text{REMOTE}}$ is inverted to logic 1 by Q7, and S1 can not pull down any of the control lines to logic 0). The BCD input is converted to its numeric equivalent and appears as a logic 0 at the specified output terminal.

For Example: the input code for 10 + 1 μs is 43 = 0, 18 = 0, 42 = 0, 17 = 1 for a BCD equivalent weight of 1. This input results in the 10 + 1 μs line to be at logic 0 and all the remaining outputs to be at logic 1. The 10 + 1 μs output is selected in the instrument through diode CR49.

3.39 When remote is not selected, the $\overline{\text{REMOTE}}$ line is at logic 1. Switch S1 is enabled and U4A, through the two 'OR' gates, is inhibited (see paragraph 3.34).

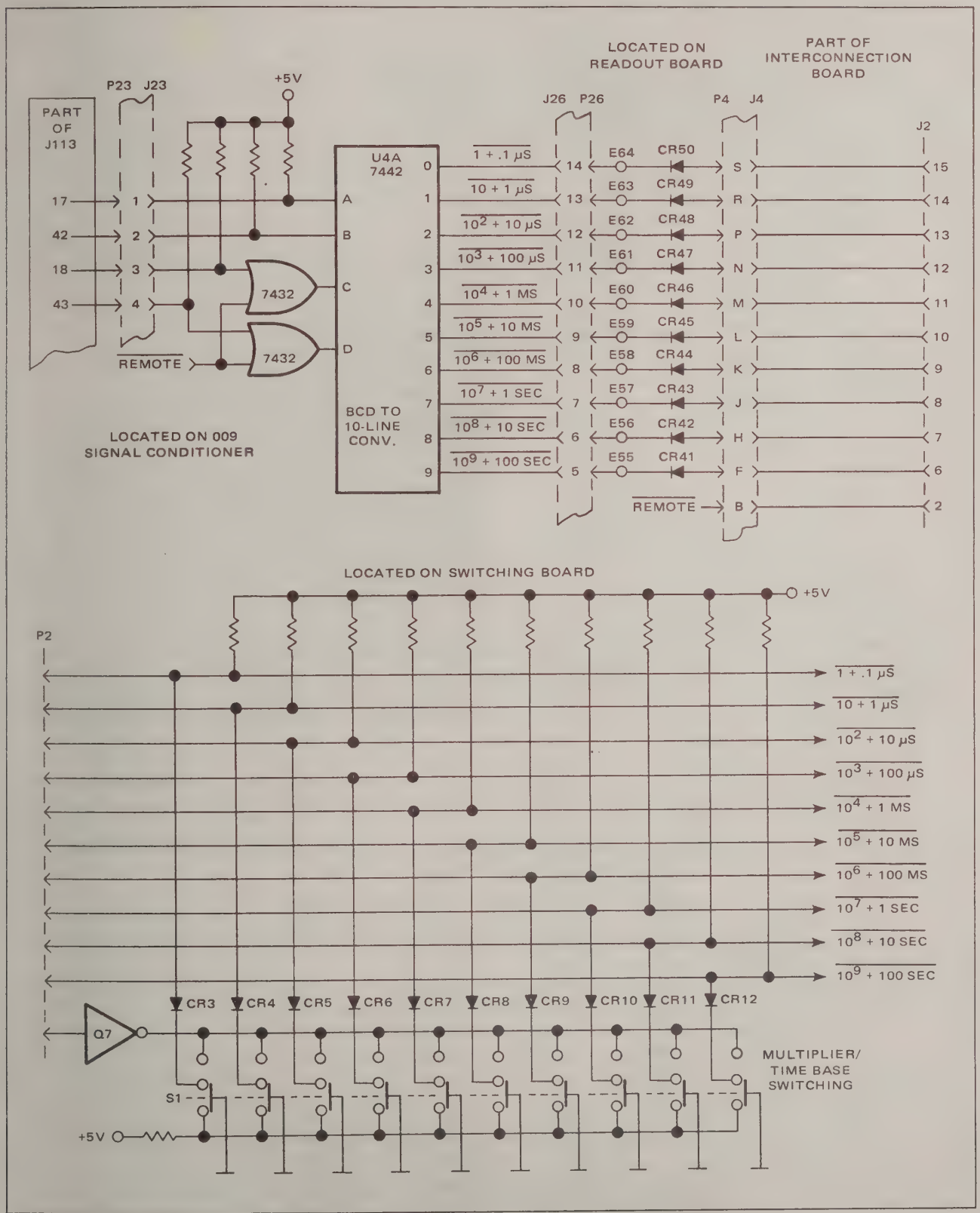


Figure 3.9 - Remote Multiplier/Time Base Decode (8010B, 8030B)

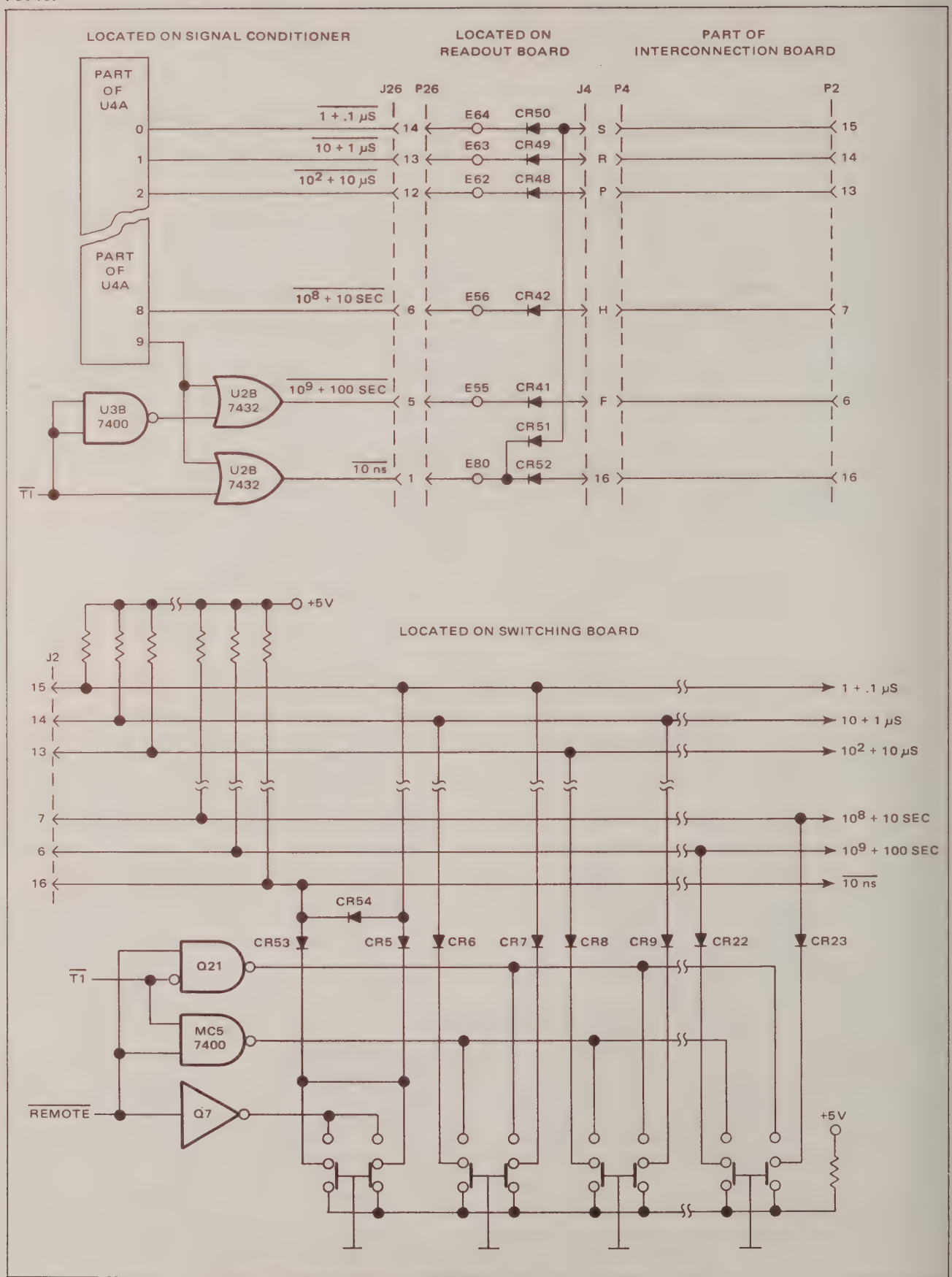


Figure 3.10 - 009 Remote Multiplexer/Time Base Decode (8015B, 8035B)

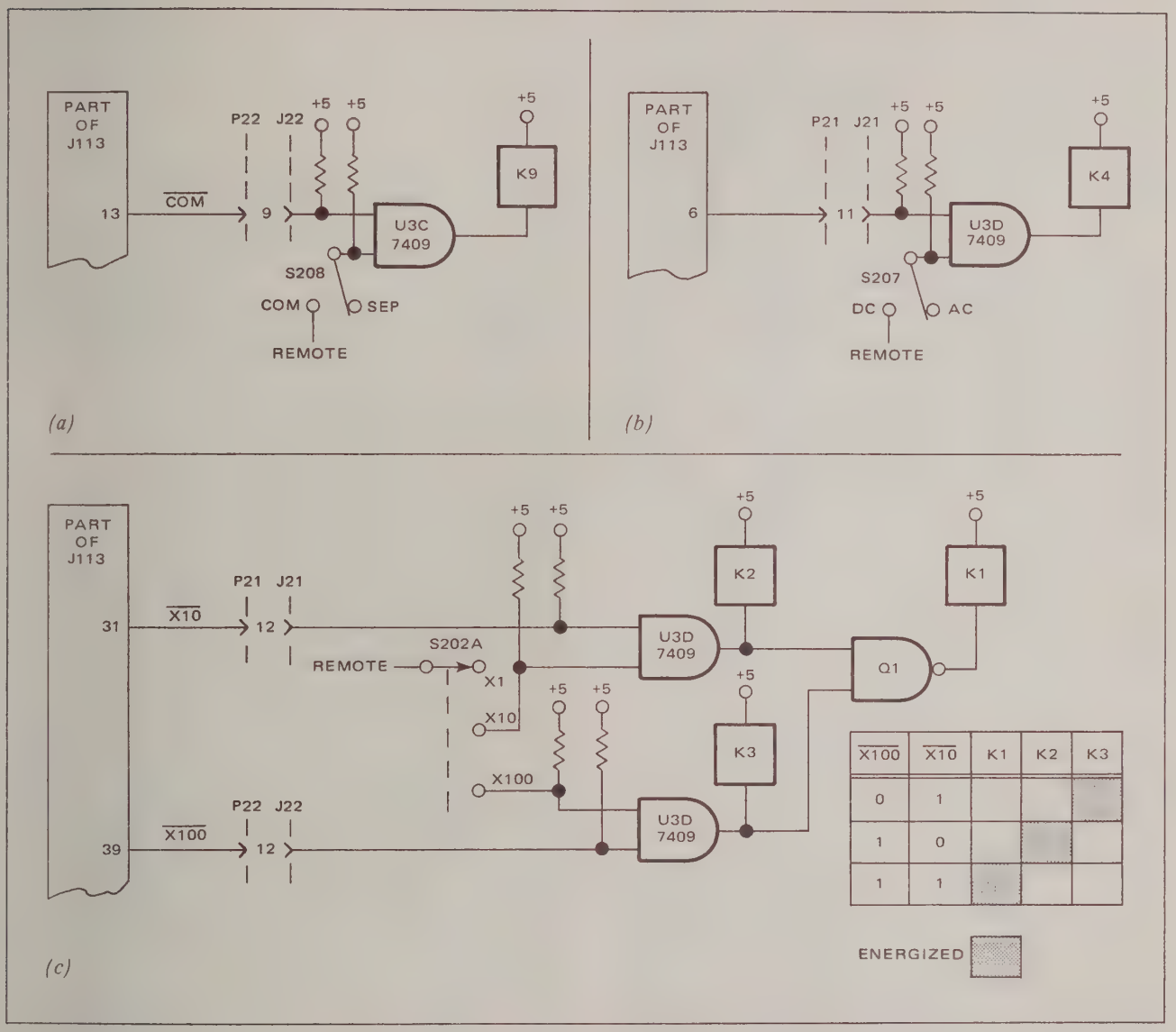


Figure 3.11 - Sep/Com, AC/DC Range Remote Inputs (009)

3.40 8015B, 8035B.

3.41 In all functions except Time Interval, the multiplier/time base of these instruments is programmed and operates in the same manner as the 8010B and 8030B counters. That is, the input BCD code is converted to 10-line by converter U4A and U4A is inhibited while the instrument is in local control. As shown in figure 3.10, additional logic is provided for the TI function and includes two 'OR' gates (U2B) and a NAND gate (U3B). In all but the TI function, the $\overline{TI}$ line (from the function converter, U4B) is logic 1, U3B output is logic 0, and the 9 output of U4A, when selected, appears at J26-5. In the TI function, $\overline{TI}$ is logic 0, the output of U3B is logic 1 and the 9 output of U4A, when selected, appears at J26-1 ($\overline{10}$ ns line). Also shown in figure 3.10 is the interconnection of the remote and local multiplier/time base circuitry.

3.42 Remote Input Operation.

3.43 The control of the input circuitry (or inputs) includes remote selection of separate/common, input range, and AC/DC. The signal conditioning module of the 009 option uses relays in place of the standard instrument switches to permit remote operation. The circuitry is described in the following paragraphs.

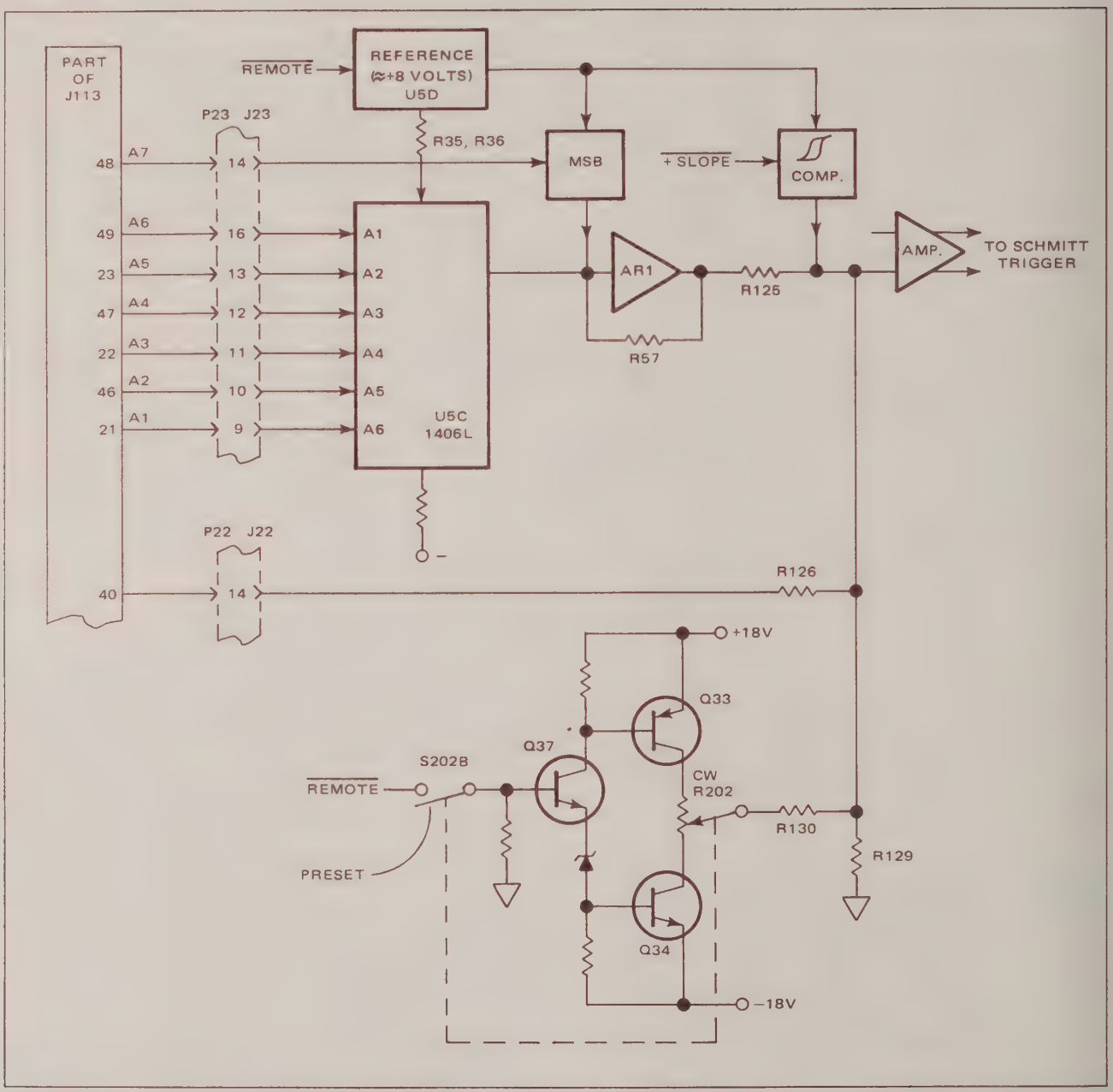


Figure 3.12 - Remote Trigger Level Control (009)

3.44 SEPARATE/COMMON.

3.45 This circuit, shown in figure 3.11(a) uses an AND gate driving a relay (K9). With remote not selected REMOTE is at logic 0 and the remote COM line is at logic 1. When S208 is in the (SEP) position, the output of the AND gate is at logic 1 and the relay is not energized; when S208 is in the (COM) position the output of the gate is at logic 0 and the relay is energized. In remote operation, the REMOTE line is at logic 1 and the switch S208 is inhibited. A logic 0 on the remote $\overline{\text{COM}}$ line (J113-13) causes the relay to energize.

3.46 AC/DC.

3.47 This circuit shown in figure 3.11(b) operates in the same manner as the Separate/Common circuit (paragraph 3.44). The circuit is remotely energized by a logic 0 on J113-6.

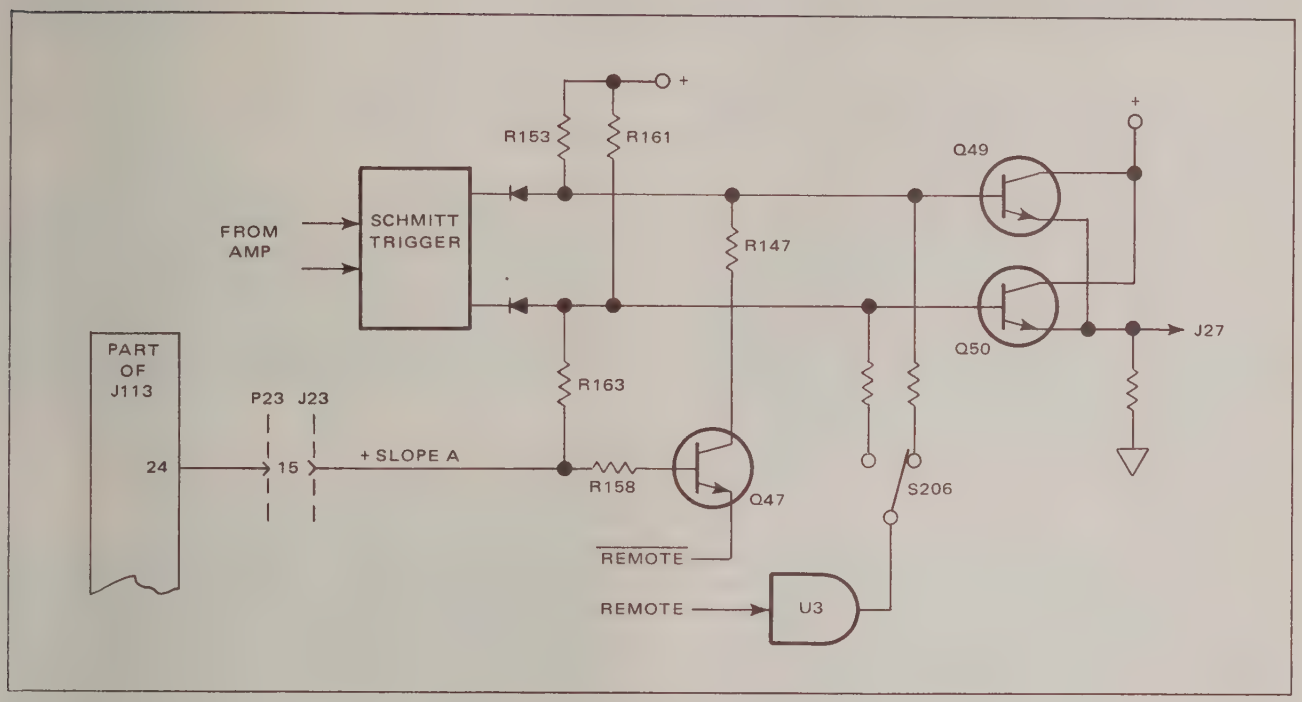


Figure 3.13 - Remote Slope Control (009)

3.48 RANGE.

3.49 The range control circuitry, figure 3.11(c), consists of two AND gates (U3D), a NAND gate and three relays. In local operation, the REMOTE line is logic 0 and S202 is capable of pulling the X10 and X100 lines down. In remote operation S202A is inhibited and selection is through the remote lines J113-31 and J113-39. The input code for selecting each of the three relays is provided in the table.

3.50 TRIGGER LEVEL CONTROL.

3.51 The circuitry shown in figure 3.12 illustrates the methods used to provide the three separate means of setting the input signal trigger level. The three methods are: Front panel control, analog input, and digital input control. All the circuitry shown is located on the 009 Signal Conditioning Module.

3.52 The front panel control circuitry basically consists of potentiometer R202 and resistor R130 working in conjunction with resistors R125 and R129 to generate a positive or negative control level. The control level is applied to the reference side of the amplifier and determines the trigger level of the Schmitt trigger. The remainder of the circuitry is used to switch the potentiometer 'in' and 'out' of the circuit. This 'pot' is in the circuit when the instrument is in local control and R202 is not in the PRESET position. In this instance, $\overline{\text{REMOTE}}$ is at logic 1 and through Q37 and CR28, biases Q34 ON. The collector current of Q37 also biases Q33 ON. This electrically connects the CW end of R202 to the +18 volt line and the CCW end of R202 to the −18 volt line. The pot is switched out of the circuit when R202 is placed in the extreme CCW position (PRESET), causing S202B to open, or when remote is selected, causing $\overline{\text{REMOTE}}$ to be at logic 0.

3.53 The analog input operates precisely as it does in the 008 option. The input (pin 40 of J113) feeds current into the circuitry through R126 and provides ±300% of the trigger range. It is used with R202 in the PRESET position or in Remote Programming.

3.54 The digital trigger level control is used only in remote operation. The circuit shown in simplified form in figure 3.12 provides 128 separate, digitally-selected, trigger levels through seven control lines. The circuitry consists of a 6-bit Digital-to-Analog converter (U5C) a seventh discrete-component bit (MSB), an 8-volt reference source (U5D), an operational amplifier (AR1), and a hysteresis compensation circuit.

3.55 The Digital-to-Analog converter generates 64 discrete output current levels from 0 to −2 milliamps. The output is fed to operational amplifier AR1 where it is

converted at the output to a voltage level of zero to +6.3 volts. The voltage is fed through resistor R125 to the input of the amplifier. A full scale output results in a trigger level of +3.150 volts.

3.56 The MSB (most-significant bit) circuit consists of a positive current source that can be switched in or out of the circuit and supplies slightly more than +2 milliamps. This current is converted to a voltage by the operational amplifier and fed through R125 to the amplifier. Its output results in a trigger level of –3.200 volts. The 6 bit Digital-to-Analog integrated logic circuit and the discrete component MSB circuit operate in conjunction to produce all of the available digitally selected trigger levels. These are shown in table 2.4.

3.57 The eight volt reference source supplies a fixed stable voltage level for the MSB and hysteresis compensation circuits and also provide a required +5 milliamp reference via R35, R36 to U5C. The reference is on only in remote operation and, by this fact, inhibits all the digital trigger level select circuitry when the instrument is in local control. The reference circuit itself consists of an integrated 5-transistor matrix (U5D) with three of the transistors used as diodes, one as an emitter follower, and one (reversed biased) as a zener diode. The output is a very stable voltage of approximately +8 volts.

3.58 The hysteresis compensation circuit provides a correcting supply of positive current to the input of the amplifier to compensate for an inherent voltage shift that occurs in the Schmitt trigger for changes in input signal polarity. This correction is necessary to enable the accurate selection of a trigger level of either + or – slope. The circuit is energized by a logic 1 signal generated by Q47, the remote + slope select transistor.

3.59 SLOPE CONTROL.

3.60 Shown in figure 3.13 is the circuitry used in the selection of the trigger slope. With remote selected, the front panel slope switch S206 is inhibited and remote + slope select transistor Q47 emitter is at logic 0. With + slope selected at J113-24 (logic 1), transistor Q47 is biased on through R158, R163, and R161, inhibiting the – slope line. With J113 at logic 0, transistor Q47 is biased off and the + slope line is biased off.

SECTION 4 CALIBRATION & MAINTENANCE

4.1 CALIBRATION.

4.2 The option 008 requires no calibration; the calibration of the 009 option is performed following the normal calibration of the 8000B Series Counter. The equipment required is listed in table 4.1 and with the exception of an optional jumper assembly is a portion of the equipment used for calibrating the Model 8000B. Calibration points are provided in figures 4.2 and 4.3.

4.3 Jumper.

4.4 The jumper assembly consists of a mating connector (Dana P/N 600047) for programming connector J113 having the required pins hard-wired together for the various calibration steps. This same operation can be performed with individual clip leads but with considerably more difficulty. The wiring of the jumper assembly is shown in figure 4.1.

4.5 Calibration Procedure.

a. Set the FUNCTION switch to REMOTE. Allow all programming lines to remain open.

b. On the Programmable Signal Conditioner assembly, monitor R125 (channel A) and adjust potentiometer R47 for a reading of −2.88 volts DC; monitor R127 (channel B) and adjust potentiometer R50 for a reading of −2.88 volts DC. (Reference measurements to E29.)

c. Connect jumper strings #1 and #2 as shown in figure 4.1 to pin 33 (GRD) of J113. Monitor R125 (channel A) and adjust potentiometer R35 for a reading of +2.84 volts DC; monitor R127 (channel B) and adjust potentiometer R37 for a reading of +2.84 volts.

d. Remove jumper string #1 from J113-33 (GRD) and attach jumper string #3 to J113-33 (GRD).

e. Connect a signal generator output to both the INPUT A of the counter and the vertical input of the oscilloscope (channel 1, 2V/cm). Connect the rear panel MARKER output of the counter to the Z AXIS input of the oscilloscope.

f. Adjust the signal generator for an output of 100 Hz, 4V P-P sinewave. With channel 2 of the oscilloscope (DC coupled, .5V/cm) monitor MD1-12 and MD2-8 on the SWITCH board assembly (reference to E1). Adjust potentiometer R113 for equal logic levels at MD1-12 and MD2-8.

g1. (Models 8010B, 8030B.) Monitor ME0-6 and MC1-8 on the Switch board and adjust potentiometer R114 for equal logic levels.

g2. (Models 8015B, 8035B.) Monitor ME1-1 and ME1-2 on the Switch board and adjust potentiometer R114 for equal logic levels.

h. Decrease the output level of the signal generator to 1 volt P-P and set the oscilloscope channel 1 gain to 20 mV/cm. Adjust potentiometer R102 so that marker initiation is within 10 mV of zero; adjust potentiometer R103 so that marker termination is within 10 mV of zero.

Table 4.1 - Required Calibration Equipment

Instrument Type	Required Specification	Recommended Equipment
Oscilloscope	100 Hz BW, 20 mV/cm	TEK 454
Voltmeter	10V, 4 digit accuracy	Dana 4300
Sinewave Generator	100 Hz @ 4V P.P.	Dana 7010
Jumper Assembly – see figure 4.1		

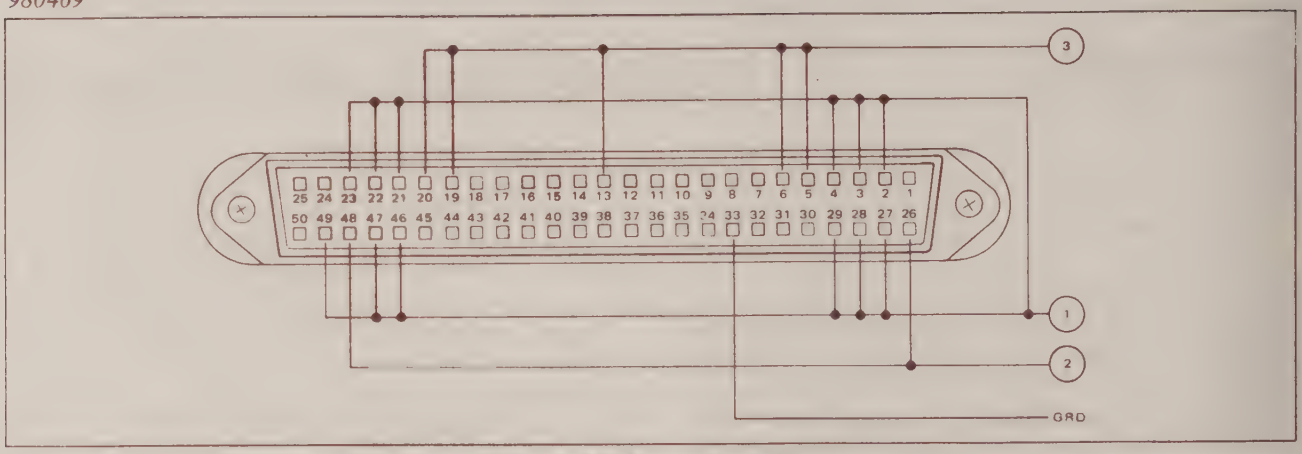


Figure 4.1 - Jumper Assembly

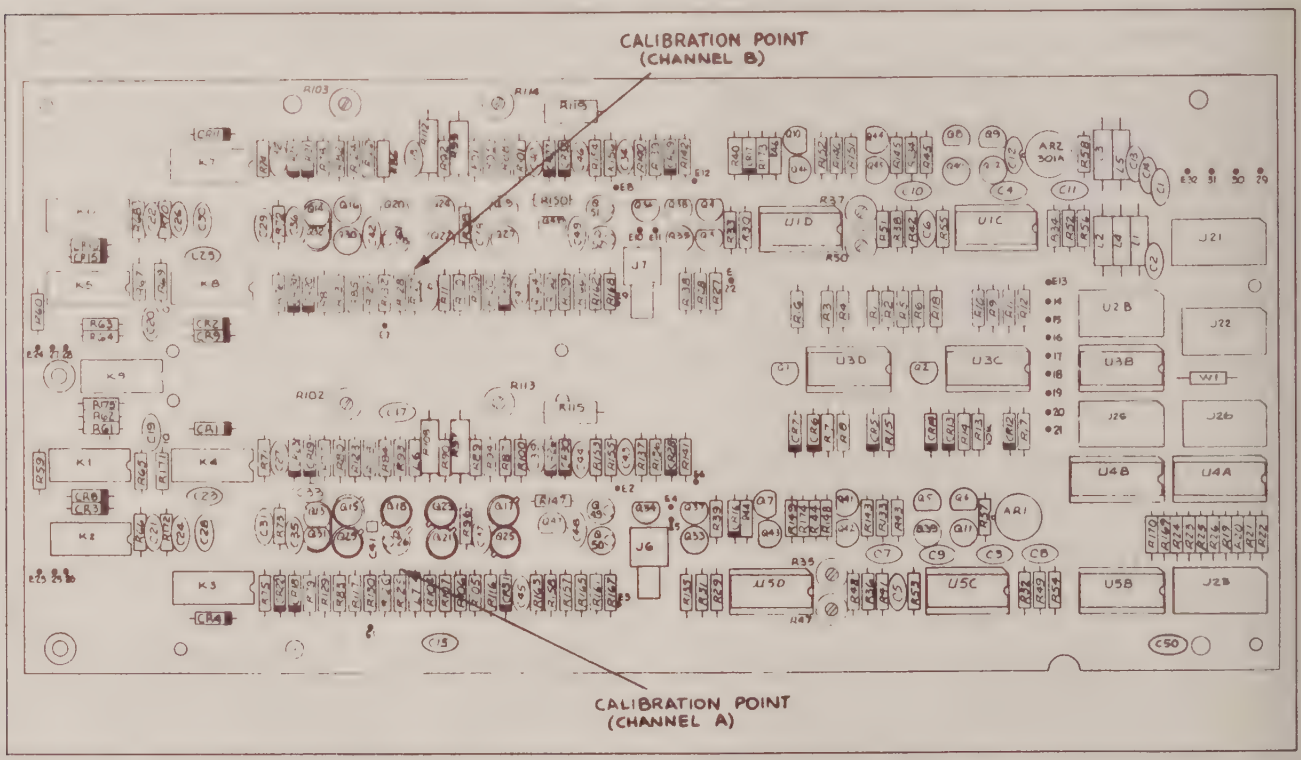


Figure 4.2 - Programmable Signal Conditioner Calibration Points

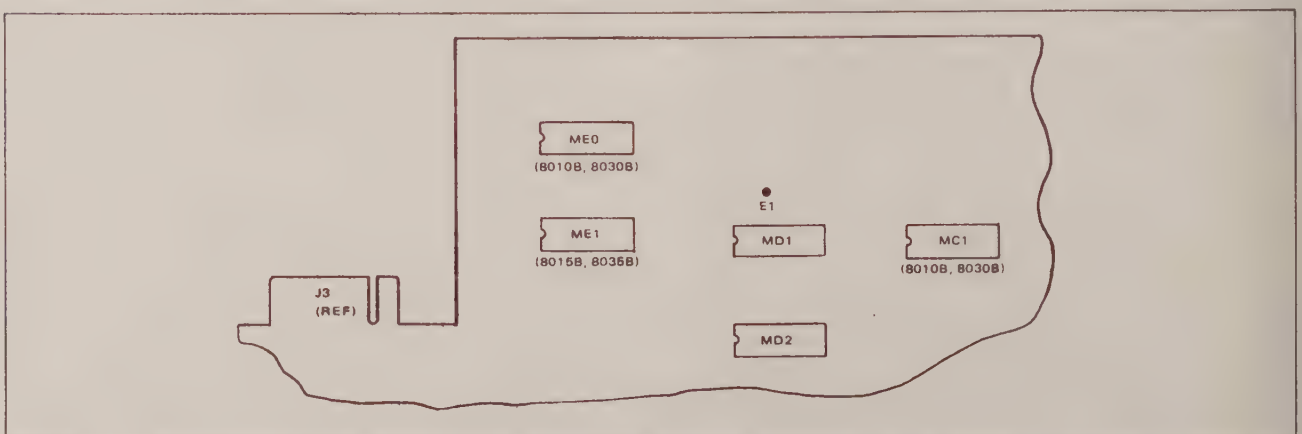


Figure 4.3 - Switch Board Calibration Points

4.6 MAINTENANCE.

4.7 The fan on the rear panel assembly, Dana P/N 406732, used with the 009 option requires oil periodically. The location of the oil pad is indicated in figure 4.4.

4.8 Use premium grade SAE20 or 30 oil at 2 to 6 month intervals, depending on frequency of use.

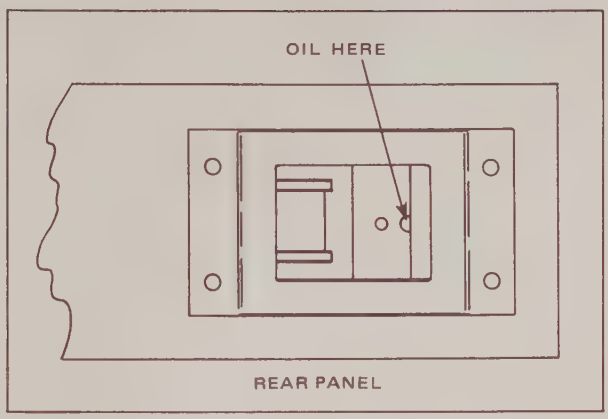
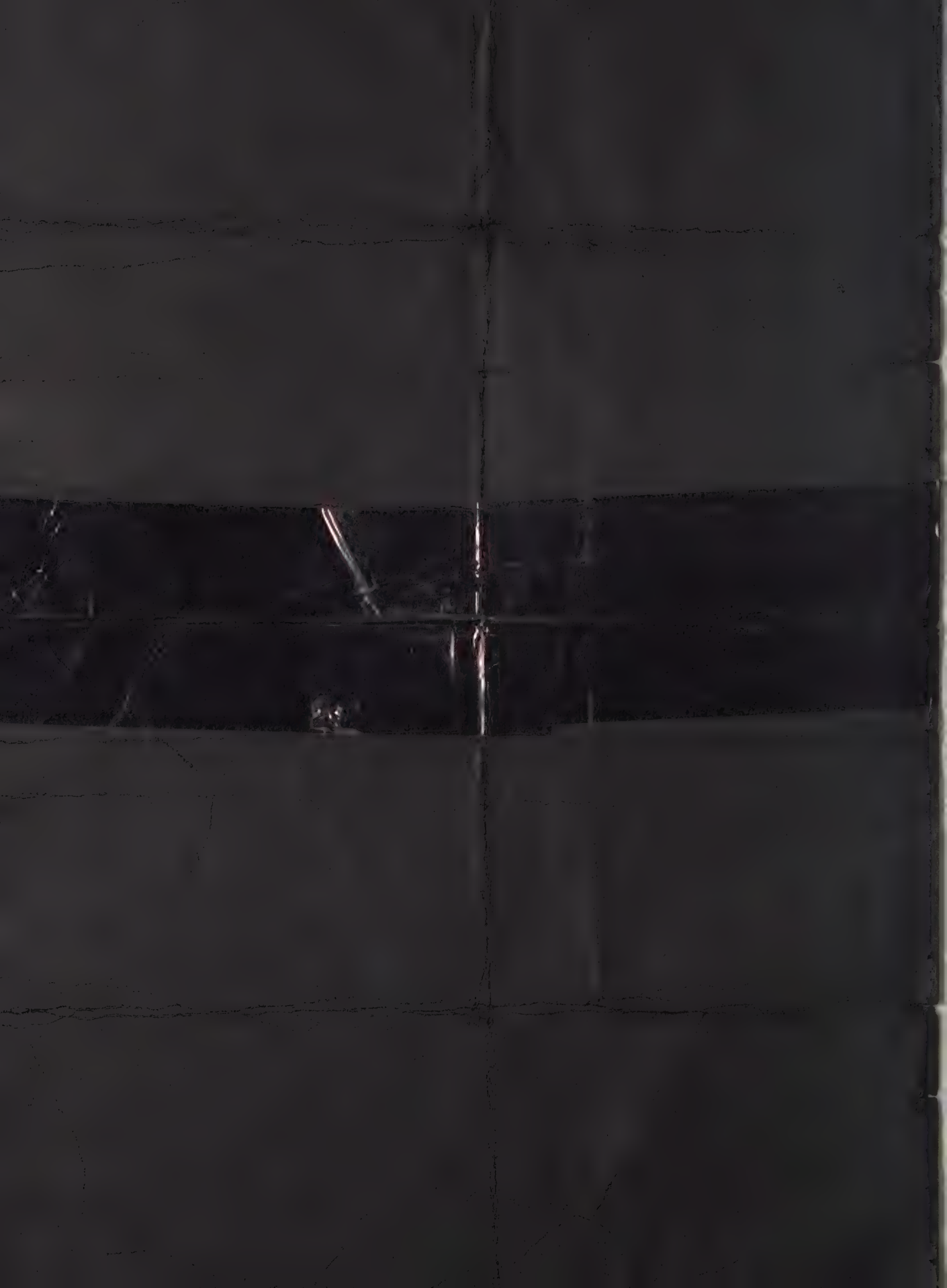


Figure 4.4 - Oil Pad Location

SECTION 5 DRAWINGS

Figure	Title	Page
Option 009		
5.1	Assembly, Full Systems Interface (406737)	5-2
5.2	Layout, Rear Panel (406732)	5-4
5.3	Layout, Interconnect (406128)	5-6
5.4	Assembly, Programmable Signal Conditioner Module (406738)	5-7
5.5	Layout, Programmable Signal Conditioner (406741)	5-8
5.6	Schematic, Programmable Signal Conditioner	5-9
5.7	Assembly, Remote Programming Cable (600762)	5-10
5.8	Assembly, Interface Harness (406756)	5-11
5.9	Assembly, Remote and Recorder Harness (406733)	5-12
Option 008		
5.10	Layout, Systems Interface (406664)	5-14
5.11	Assembly, Remote & Recorder Harness (406563)	5-15



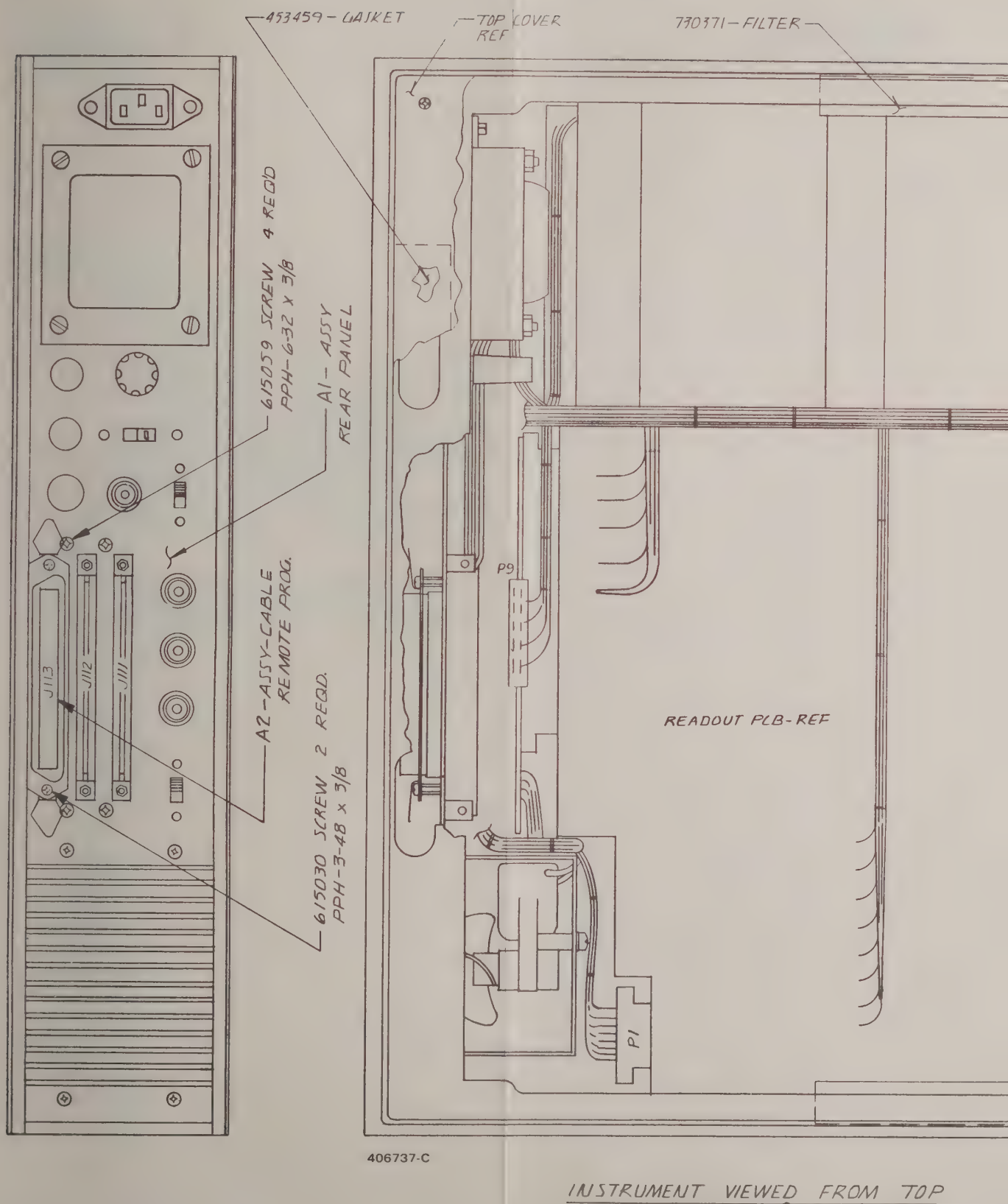
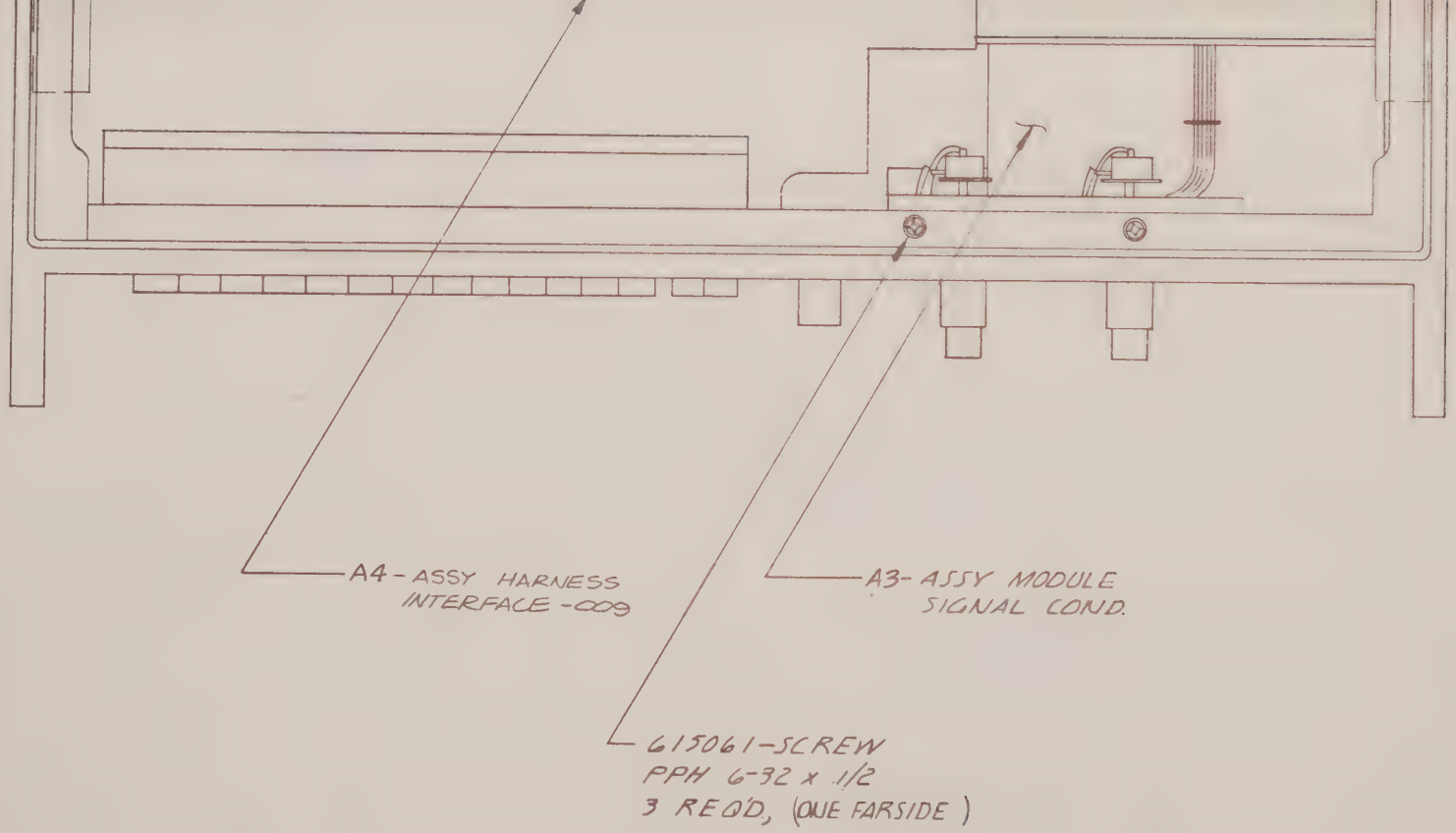
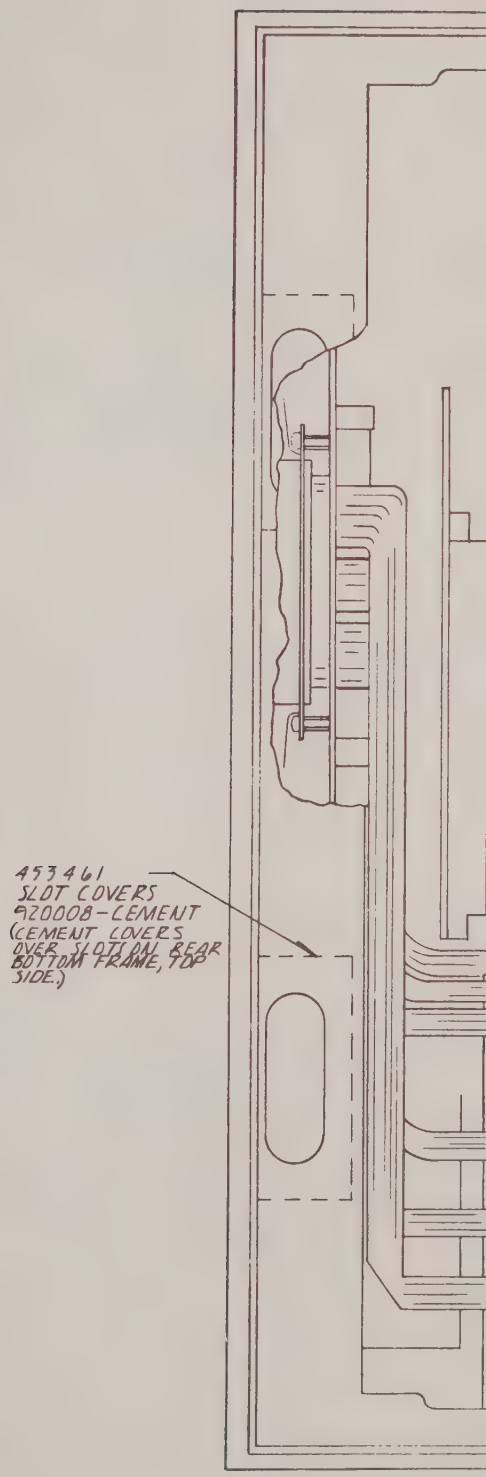


Figure 5.1 - Assembly, Full Systems Interface (406737)


730370 - FILTER
730372 - RETAINER - 4 PLCS
(2 EA FILTER
SIDE PANELS)
A4 - ASSY HARNESS
INTERFACE - 009
A3 - ASSY MODULE
SIGNAL COND.
615061 - SCREW
PPH 6-32 x 1/2
3 REQ'D, (ONE FARSIDE)


453461
SLOT COVERS
920008-CEMENT
(CEMENT COVERS
OVER SLOTS ON REAR
BOTTOM FRAME, TOP
SIDE.)

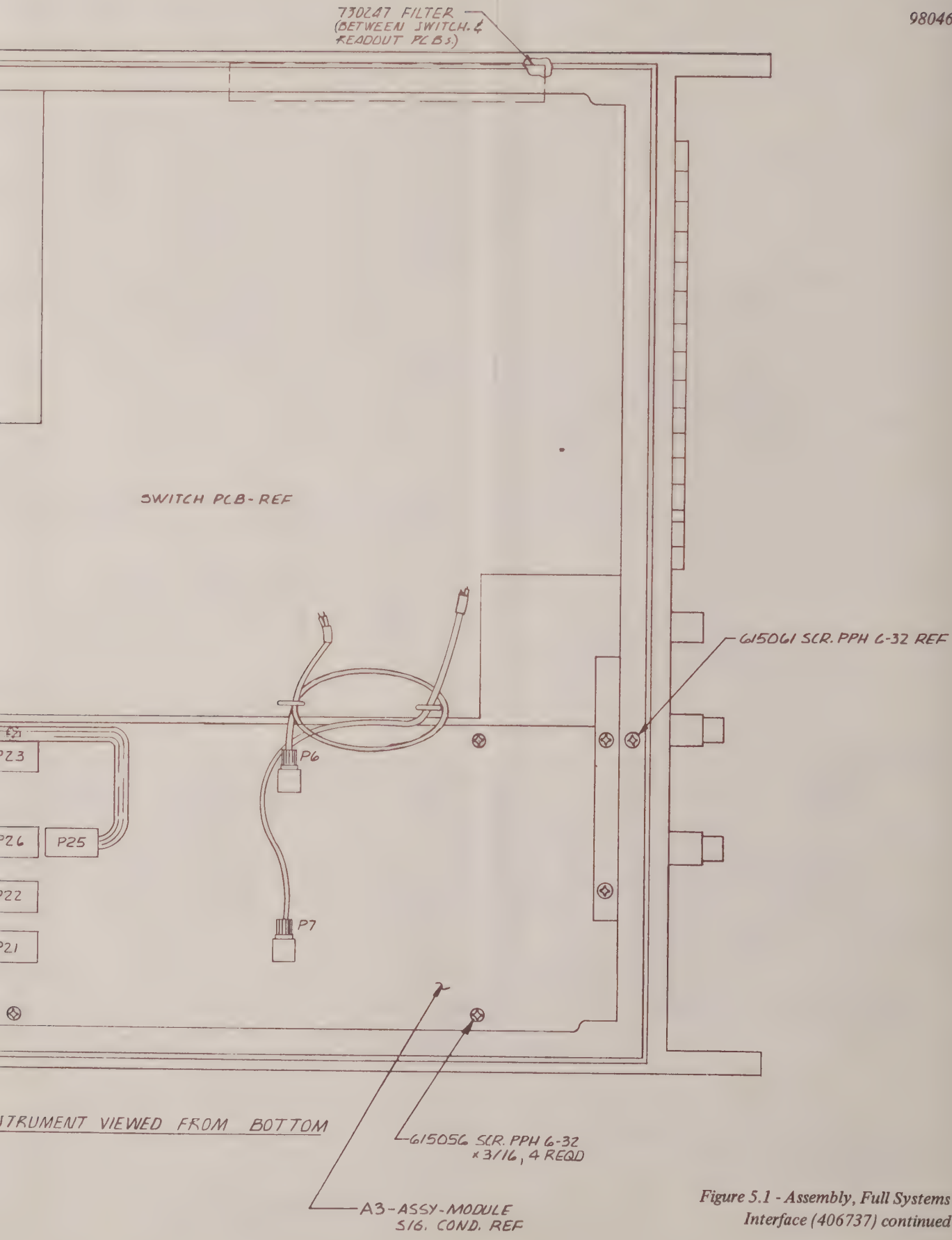
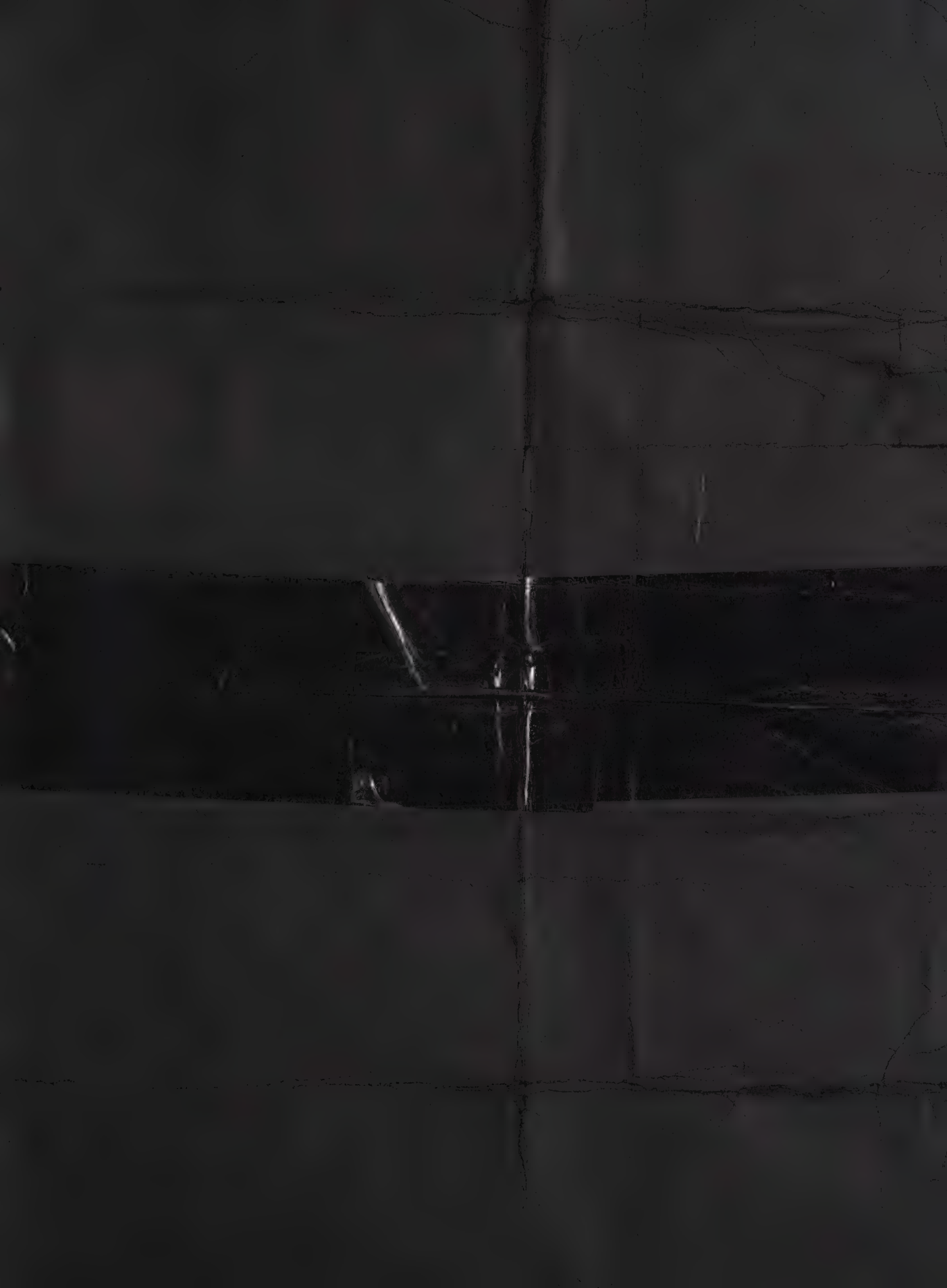
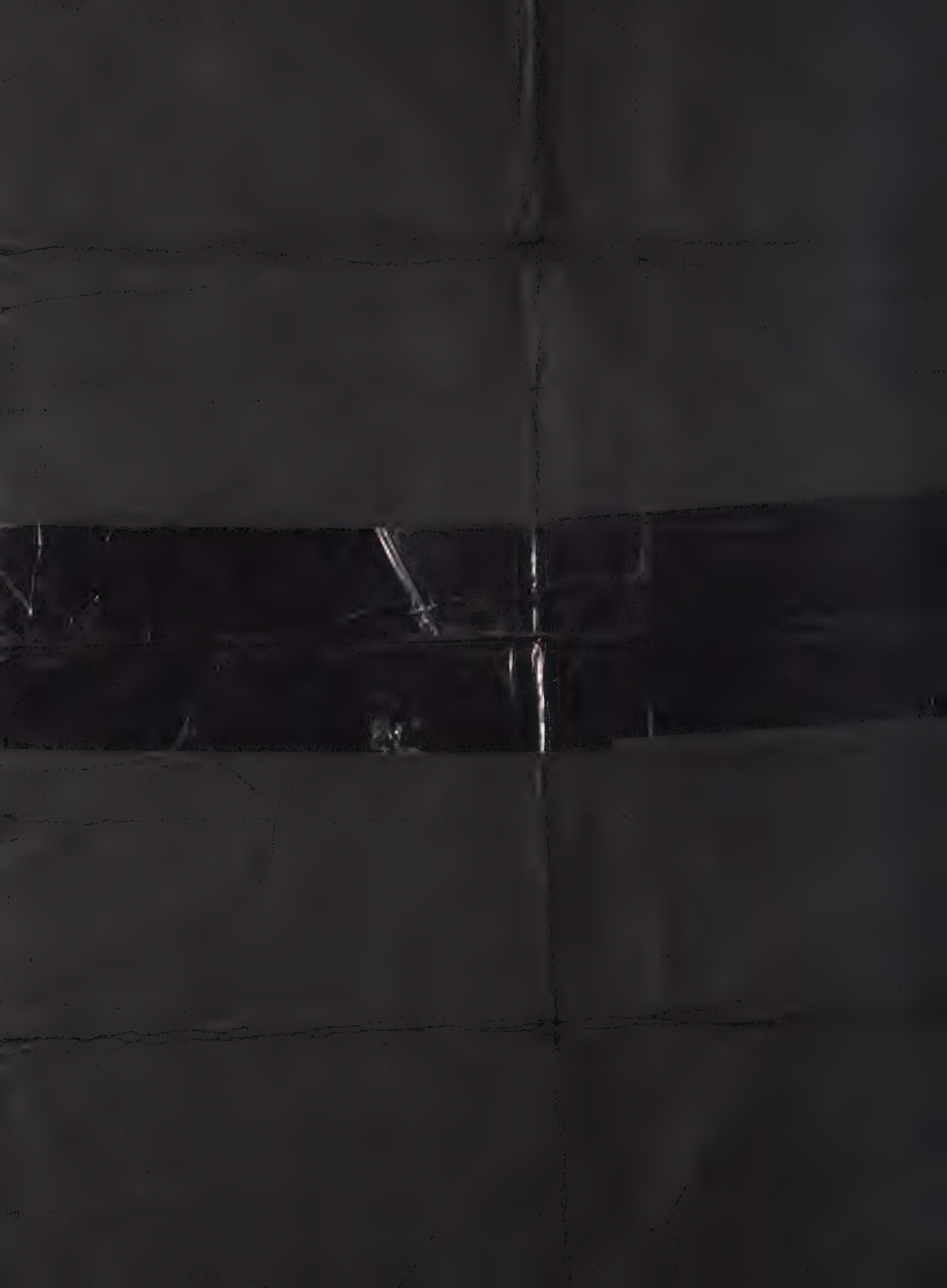
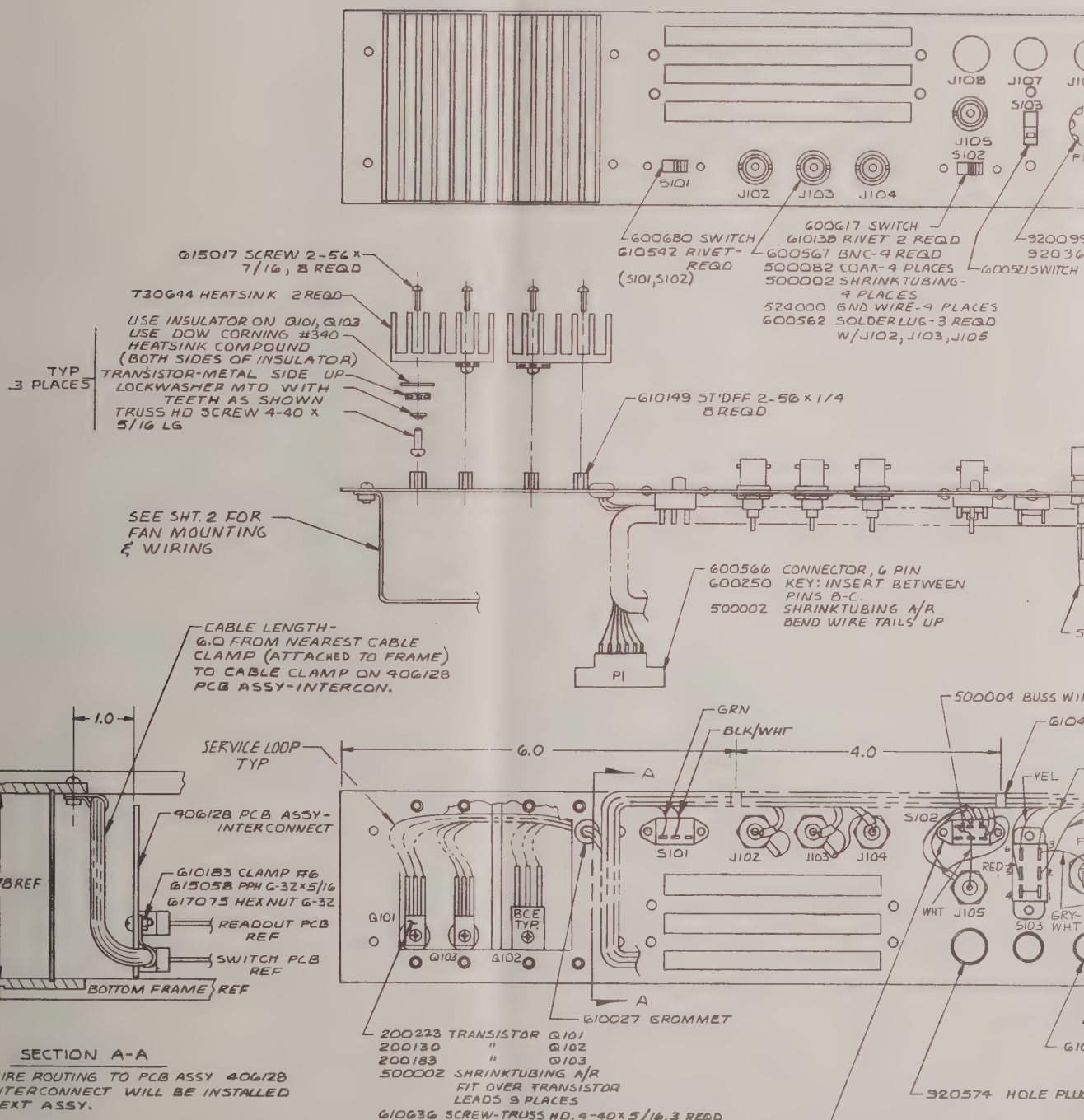


Figure 5.1 - Assembly, Full Systems Interface (406737) continued





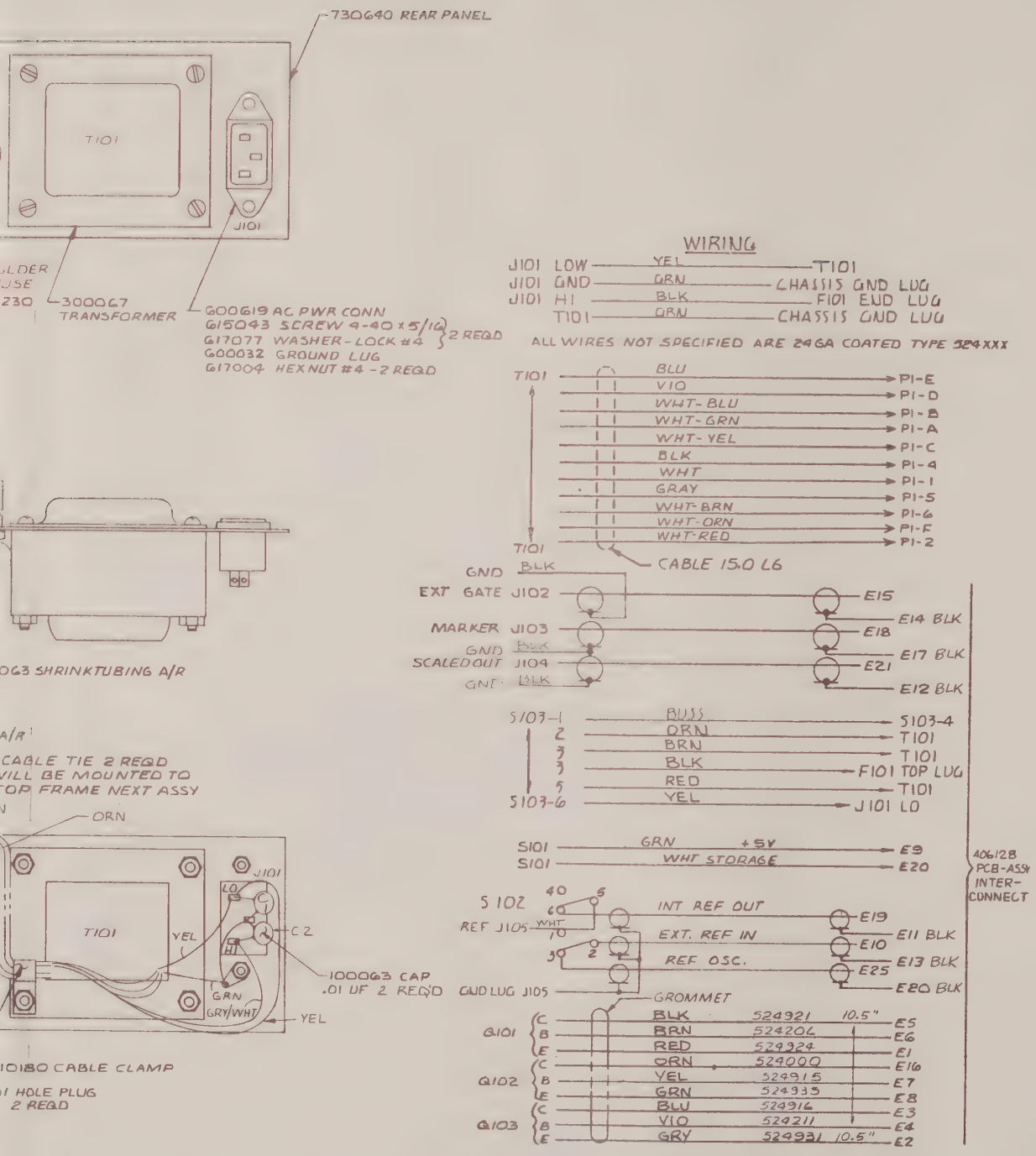


SECTION A-A

WIRE ROUTING TO PCB ASSY 406128 INTERCONNECT WILL BE INSTALLED NEXT ASSY.

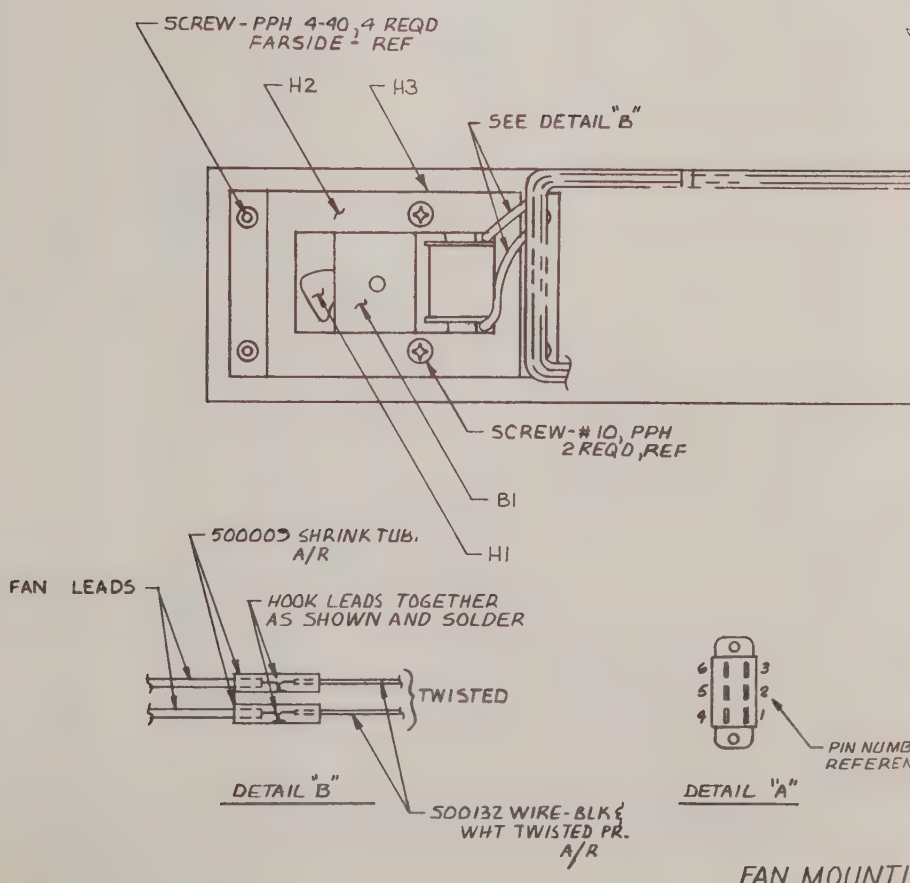
2. ASSY PROCESSES & PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS.
1. REF DESIGNATORS SHOWN FOR IDENTIFICATION PURPOSES ONLY.

NOTES: UNLESS OTHERWISE SPECIFIED

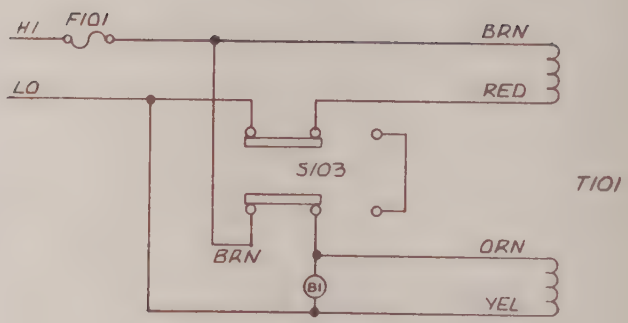


406732-D

Figure 5.2 - Layout, Rear Panel (406732)

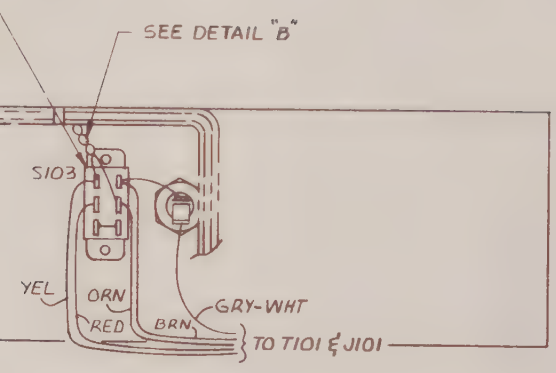

SCREW - PPH 4-40, 4 REQD
FARSIDE - REF
H2
H3
SEE DETAIL "B"
SCREW - #10, PPH
2 REQD, REF
B1
H1
500003 SHRINK TUB.
A/R
FAN LEADS
HOOK LEADS TOGETHER
AS SHOWN AND SOLDER
TWISTED
DETAIL "B"
500132 WIRE - BLK &
WHT TWISTED PR.
A/R
6
5
4
3
2
1
DETAIL "A"
PIN NUMB
REFEREN

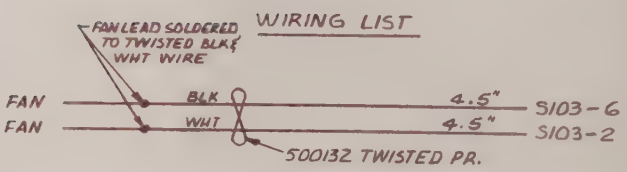
FAN MOUNTI



WIRING DIAGRAM FOR FAN & P5

SEE DETAIL "A"

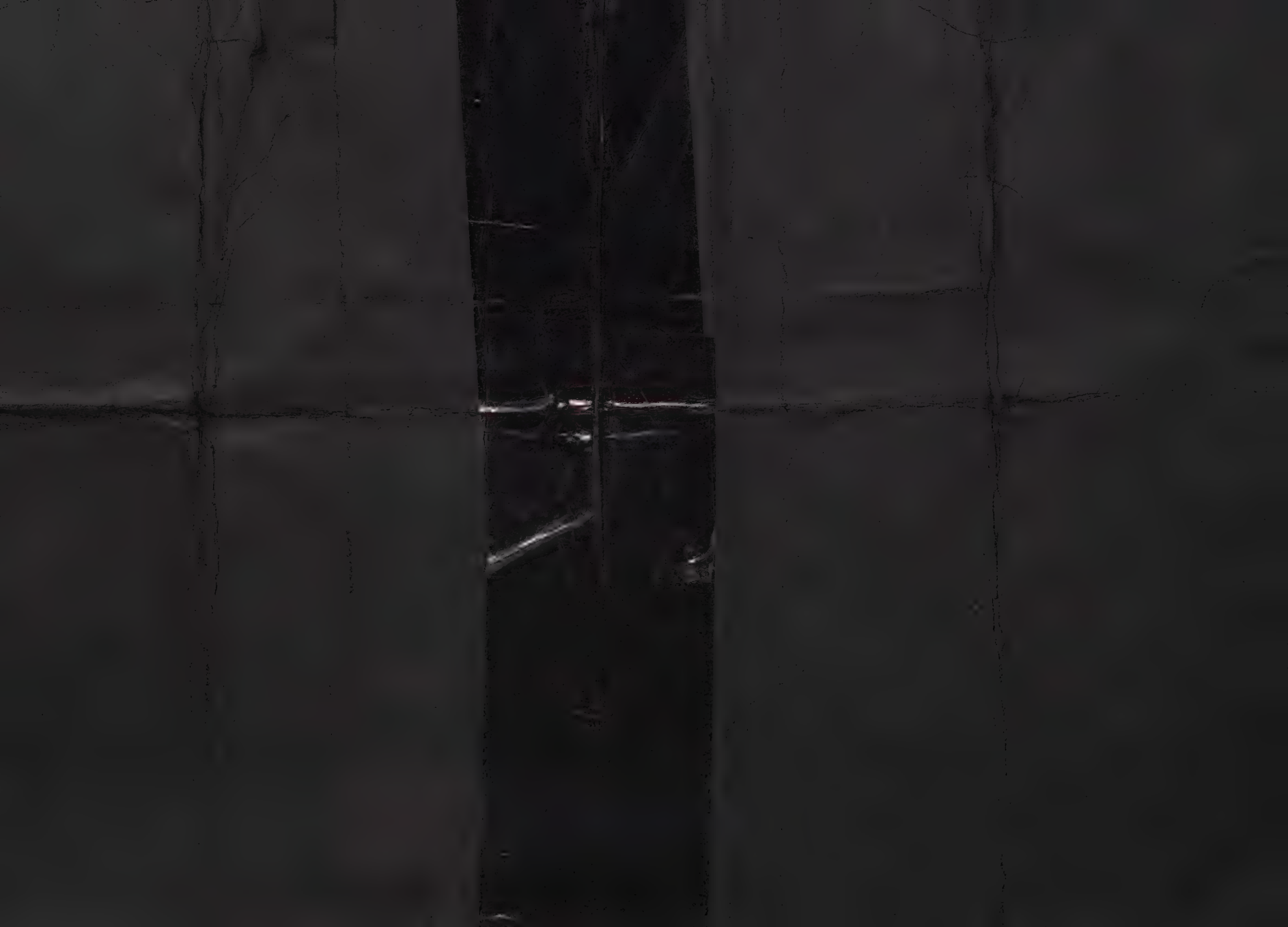


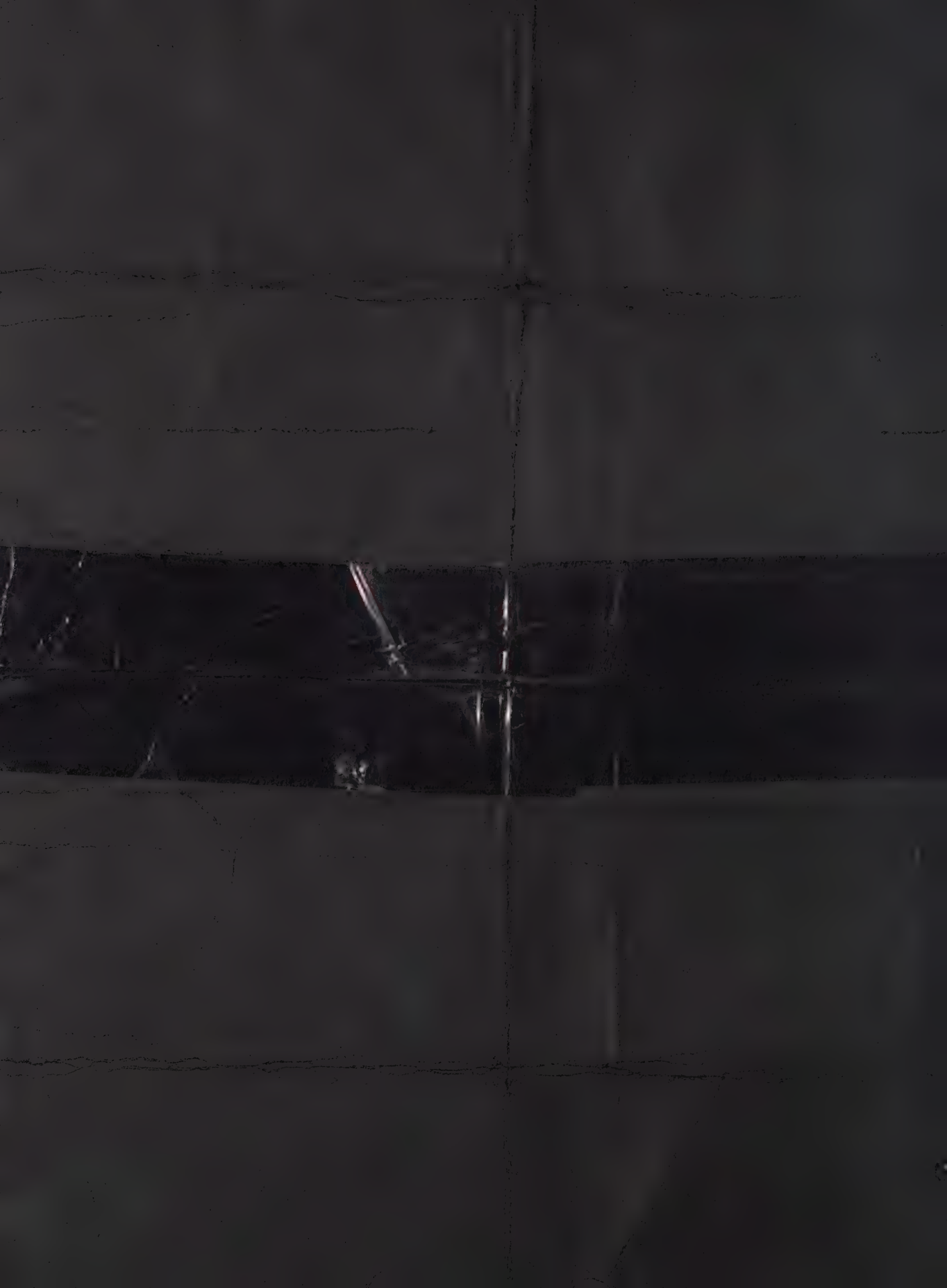


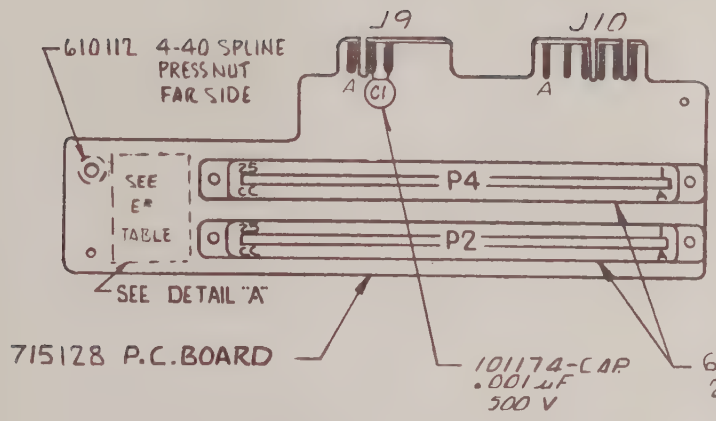
S FOR
E ONLY

G DETAIL

Figure 5.2 - Layout, Rear Panel (406732) continued

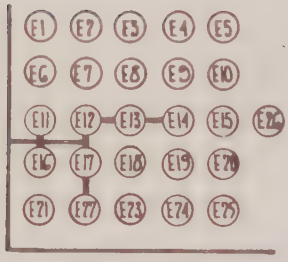






P2 PIN ASSIGNMENTS (SWITCH)

PIN #		E #	PIN #		E #
1	REF OSC		A	$\overline{P_0}$	
2	$\overline{\text{REMOTE}}$		B	$\overline{P_1}$	
3	$\overline{CR}$		C	$\overline{A/B}$	
4	GATE	E18	D	$\overline{T_0}$	
5	$\overline{F_a}$		E	$\overline{TIA}$	
6	$\overline{10^9 + 100S}$		F	$\overline{TI}$	
7	$\overline{10^8 + 10S}$		H	Dic	
8	$\overline{10^7 + 1S}$		J	Did	
9	$\overline{10^6 + 100mS}$		K	Dia	
10	$\overline{10^5 + 10\,mS}$		L	Dib	
11	$\overline{10^4 + 1\,mS}$		M	$f_a/10$	
12	$\overline{10^3 + 100\,\mu S}$		N	$\overline{\text{UPDATE}}$	
13	$\overline{10^2 + 10\,\mu S}$		P	$\overline{T_2\ \text{CLEAR}}$	
14	$\overline{10 + 1\,\mu S}$		R	$\overline{\text{REMOTE HOLD}}$	
15	$\overline{T}$		S	PRINT	
16	$\overline{T'}$		T	ARM	
17	$\overline{\text{EXT GATE}}$		U	$\overline{\text{REMOTE RESET}}$	
18	———		V	$\overline{F_2}$	
19	+18VDC		W	−18VDC	
20	+28VDC		X	+5VDC ———	E9
21	GND. —E11-E14,E16,E17		Y	GND. —E11-E14,E16,E17	
22	10 MHz		Z	MARKER OUT	E15
23	———		AA	REF OUT	E19
24	———		BB	———	E20
25	EXT REF IN	E10	CC	f/n (SCALED OUT)	E21



DETAIL "A"

VIEWED FROM COMPONENT SIDE

CONNECTOR

E # ASSIGNMENTS TO REAR PNL.	
E #	FUNCTION
E1	Q101 EMITTER
E2	Q103 EMITTER
E3	Q103 COLLECTOR
E4	Q103 BASE
E5	Q101 COLLECTOR
E6	Q101 BASE
E7	Q102 BASE
E8	Q102 EMITTER
E9	+5
E10	EXT REF IN
E11	GND SHD FROM COAX AT E19
E12	GND SHD FROM COAX AT E21
E13	GND SHD FROM COAX AT E10
E14	GND SHD FROM COAX AT E18
E15	MARKER
E16	Q102 COLLECTOR
E17	GND SHD FROM COAX AT E15
E18	GATE
E19	REF OUT
E20	STORAGE
E21	SCALED OUT
E22	GND SHD FROM COAX AT E25
E23	CHAN A REMOTE LEVEL
E24	+28VDC
E25	REF.OSC.
E26	CHAN B REMOTE LEVEL

P4 PIN ASSIGNMENTS (READOUT)					
	E#	PIN #			E#
$\overline{PA}$		A	TCXO (REF OSC)		
$\overline{PI}$		B	$\overline{REMOTE}$		
$\overline{A/B}$		C	$\overline{ZR}$		
$\overline{To}$		D	GATE		
$\overline{TIA}$		E	$\overline{Fa}$		
$\overline{TI}$		F	$\overline{10^9 + 100S}$		
D1C		H	$\overline{10^8 + 10S}$		
D1D		J	$\overline{10^7 + 1S}$		
D1A		K	$\overline{10^6 + 100mS}$		
D1B		L	$\overline{10^5 + 10mS}$		
Fa/10		M	$\overline{10^4 + 1mS}$		
$\overline{UPDATE}$		N	$\overline{10^3 + 100\mu S}$		
$\overline{T_2 CLEAR}$		P	$\overline{10^2 + 10\mu S}$		
HARMONIC COUNT		R	$\overline{10 + 1\mu S}$		
$\overline{\quad\quad}$		S	$\overline{T}$		
$\overline{T'}$		T	$\overline{REMOTE\ HOLD}$		
$\overline{EXT\ GATE}$		U	PRINT		
$\overline{Fc}$		V	$\overline{REMOTE\ RESET}$		
-18V		W	+18V		
+5V	E9	X	+28V		
GROUND	E11-E14, E16, E17	Y	Q102	E11-E14, E16, E17	
Q101	E1	Z	Q101	E5	
Q103	E2	AA	Q101	E6	
Q103	E3	BB	Q102	E7	
Q103	E4	CC	Q102	E8	

J10 PIN ASSIGNMENTS (R-F BOARD)	
PIN #	
A ∤ 1	$\overline{\quad\quad}$
B ∤ 2	$\overline{Fc}$
C ∤ 3	$\overline{\quad\quad}$
D ∤ 4	+5V
E ∤ 5	-18V
F ∤ 6	+18V

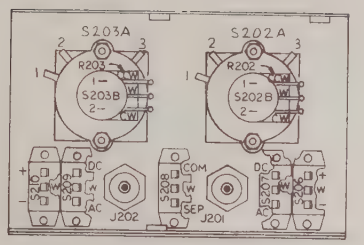
J9 PIN ASSIGNMENTS (SIGNAL COND)	
PIN #	
A ∤ 1	REMOTE LEVEL 'A'
B ∤ 2	REMOTE LEVEL 'B'
C ∤ 3	GND
D ∤ 4	$\overline{REMOTE}$
E ∤ 5	-18V
F ∤ 6	+18V

406128-F

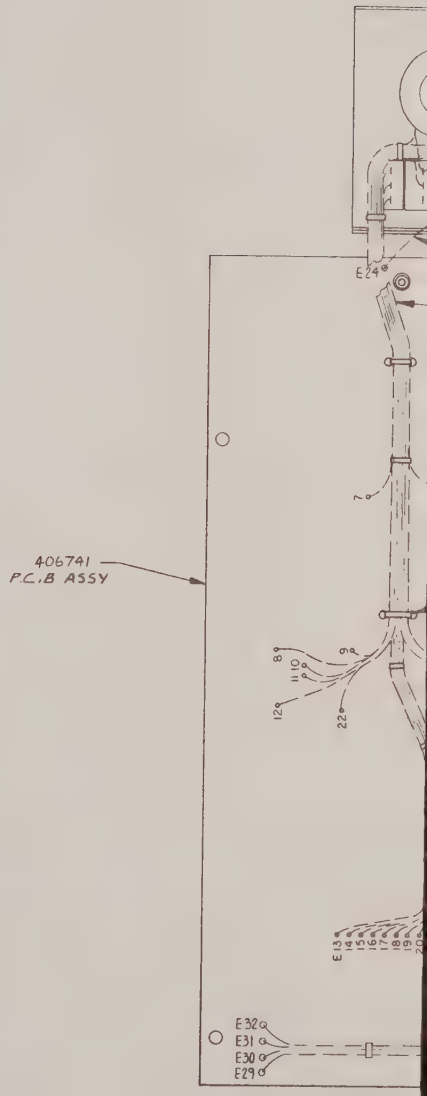
Figure 5.3 - Layout, Interconnect (406128)

Signal Conditioning Module Wire List

TO	FROM	WIRE COLOR
S202A-1	E-21	BRN
S202A-2	E-15	GRN
R202-CCW	E-4	YEL
R202-W	E-1	BRN
R202-CW	E-5	GRN
S203A-1	E-20	BLK
S203A-2	E-19	WHT
R203-CCW	E-11	BRN
R203-W	E-7	VIO
R203-CW	E-10	BLK
S202B-1	E-6	BLU
S203B-1	E-12	RED
S202B-2	S203B-2	WHT
S203B-2	E-22	WHT/RED
S206 +	E-2	RED
S206 –	E-3	ORG
S207-W	E-14	YEL
S208-W	E-18	GRY
S209-W	E-13	ORG
S210 +	E-8	GRY
S210 –	E-9	WHT
S206-W	S210-W	BLU
S210-W	E-16	BLU
S207-DC	S202A-3	WHT/BLK
S202A-3	S207-COM	WHT/BLK
S208-COM	S203A-3	WHT/BLK
S203A-3	S209-DC	WHT/BLK
S209-DC	E-17	WHT/BLK
J201	E-23	WHT
J202	E-24	WHT
E-29	P9-3	BLK
E-30	P9-0	GRN
E-31	P9-5	BLU
E-32	P9-6	RED



REFERENCE VIEW
FOR WIRING POINT IDENTIFICATION



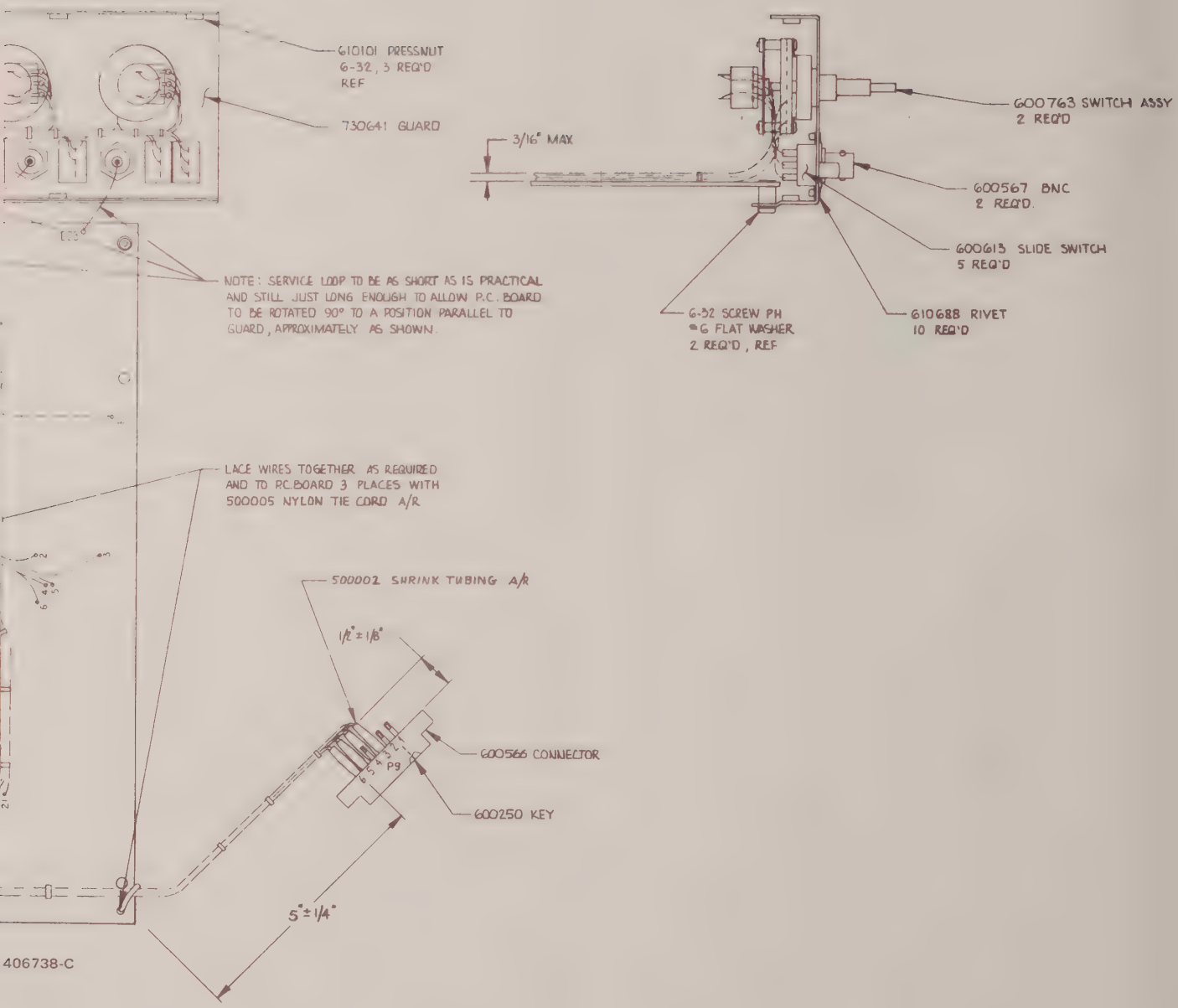
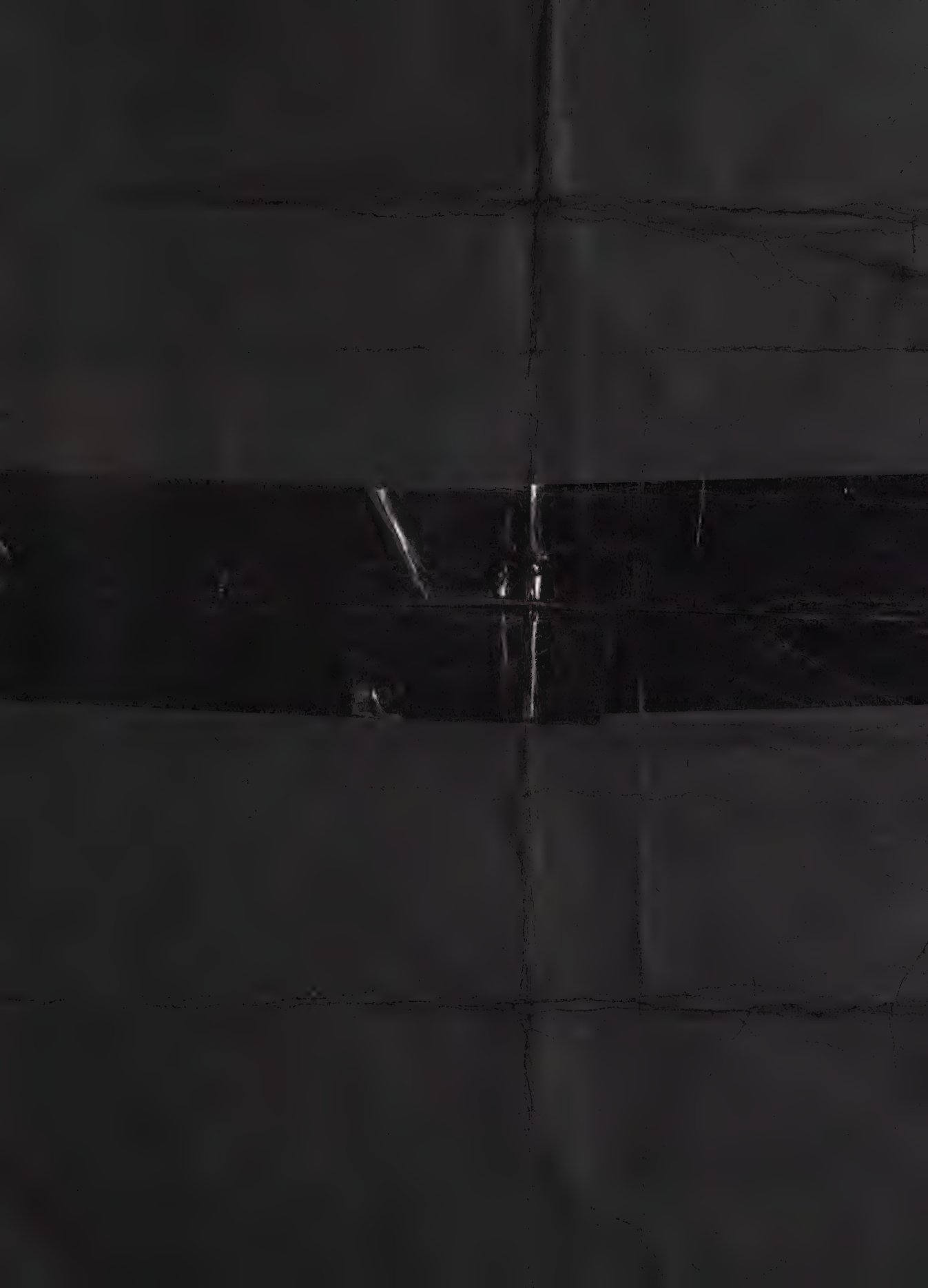

610101 PRESSNUT
6-32, 3 REQ'D
REF
730641 GUARD
3/16" MAX
600763 SWITCH ASSY
2 REQ'D
600567 BNC
2 REQ'D.
600613 SLIDE SWITCH
5 REQ'D
610688 RIVET
10 REQ'D
6-32 SCREW PH
#6 FLAT WASHER
2 REQ'D, REF
NOTE: SERVICE LOOP TO BE AS SHORT AS IS PRACTICAL AND STILL JUST LONG ENOUGH TO ALLOW P.C. BOARD TO BE ROTATED 90° TO A POSITION PARALLEL TO GUARD, APPROXIMATELY AS SHOWN.
LACE WIRES TOGETHER AS REQUIRED AND TO P.C.BOARD 3 PLACES WITH 500005 NYLON TIE CORD A/R
500002 SHRINK TUBING A/R
1/2" ± 1/8"
600566 CONNECTOR
P9
600250 KEY
5" ± 1/4"
406738-C

Figure 5.4 - Assembly, Programmable Signal Conditioner Module (406738)



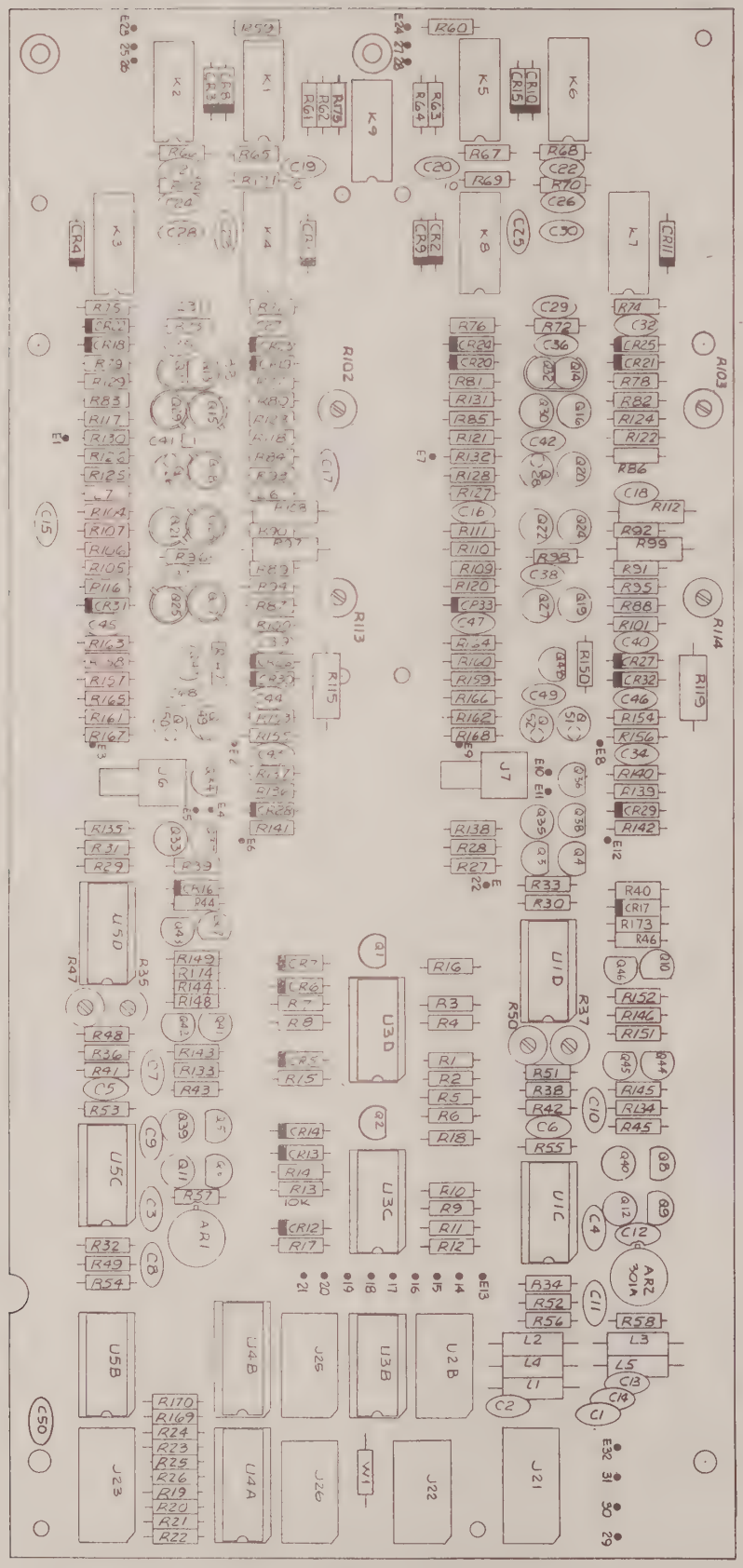
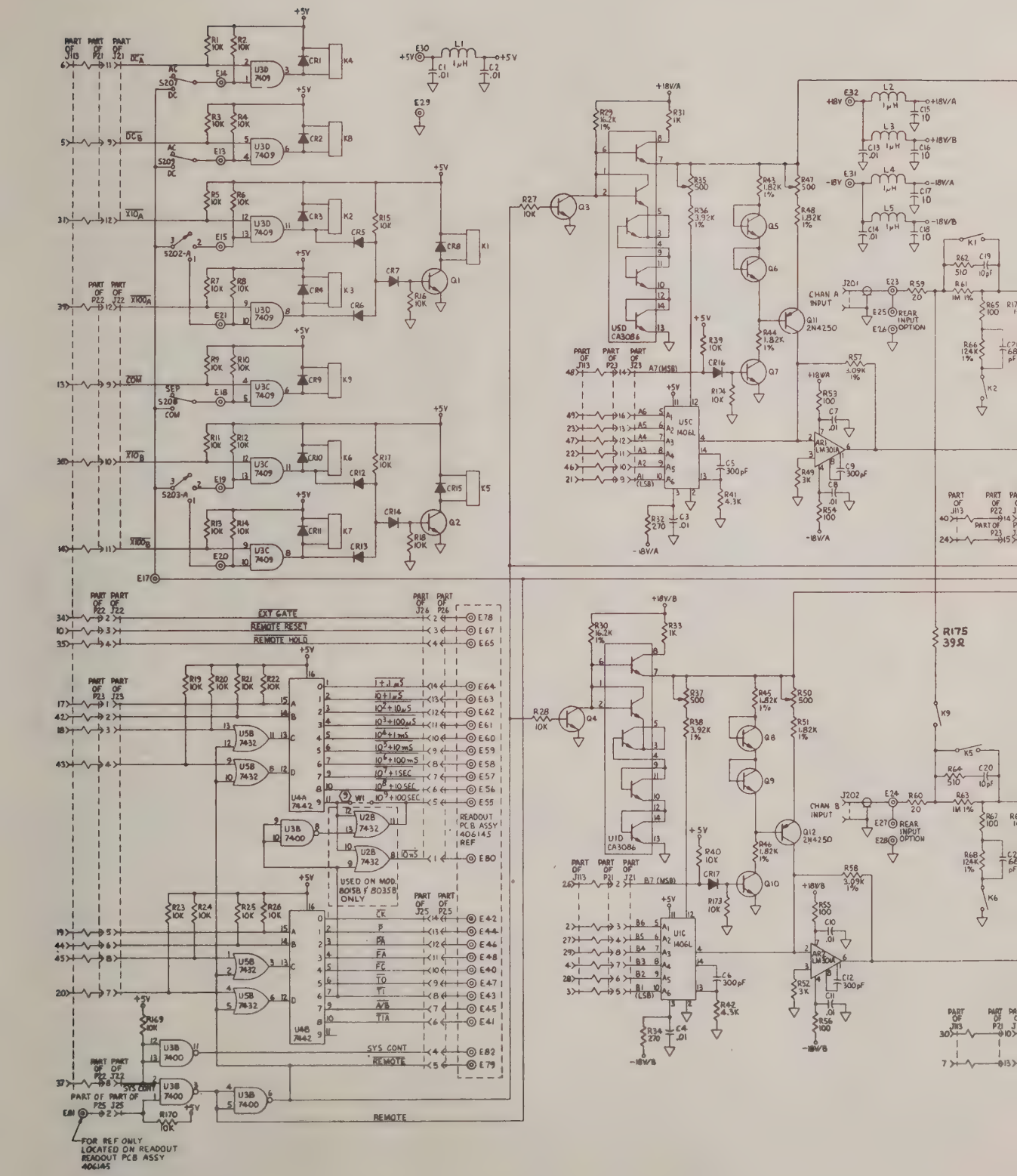
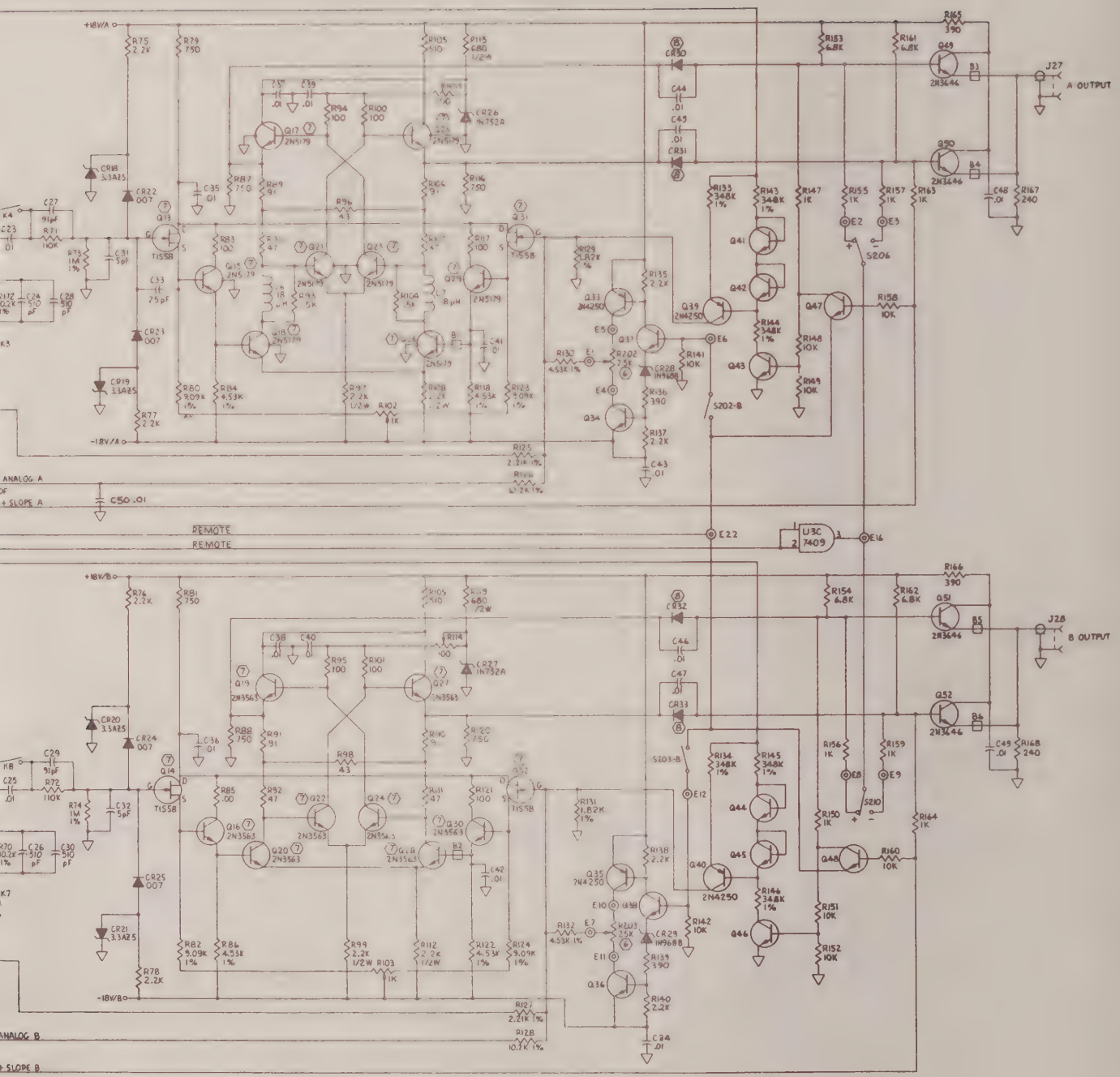


Figure 5.5 - Layout, Programmable Signal Conditioner (406741)


+5V
L1
C1 1μH
C2 .01
E30
E29
R1 10K
R2 10K
R3 10K
R4 10K
R5 10K
R6 10K
R7 10K
R8 10K
R9 10K
R10 10K
R11 10K
R12 10K
R13 10K
R14 10K
R15 10K
R16 10K
R17 10K
R18 10K
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR10
CR11
CR12
CR13
CR14
CR15
K1
K2
K3
K4
K5
K6
K7
K8
K9
Q1
Q2
U3D 7409
U3C 7409
S201
S202-A
S203-A
S204
AC
DC
SEP
COM
E14
E15
E16
E18
E19
E20
E21
E17
PART OF J113
PART OF P21
PART OF J21
PART OF P22
PART OF J22
DC_A
DC_B
X10_A
X100_A
COM
X10_B
X100_B
+18V/A
+18V/B
-18V/A
-18V/B
R27 10K
R28 10K
R29 16.2K 1%
R30 16.2K 1%
R31 1K
R33 1K
R35 500
R36 3.92K 1%
R37 500
R38 3.92K 1%
R39 10K
R40 10K
R41 4.3K
R42 4.3K
R43 1.82K 1%
R44 1.82K 1%
R45 1.82K 1%
R46 1.82K 1%
R47 500
R48 1.82K 1%
R50 500
R51 1.82K 1%
R52 3K
R53 100
R54 100
R55 100
R56 100
R57 3.09K 1%
R58 3.09K 1%
R59 20
R60 20
R61 1M 1%
R62 510
R63 1M 1%
R64 510
R65 100
R66 124K 1%
R67 100
R68 124K 1%
R169 10K
R170 10K
R173 10K
R174 10K
R175 39Ω
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11 2N4250
Q12 2N4250
U5D CA3086
U1D CA3086
U5C 1406L
U1C 1406L
AR1 LM301A
C3 .01
C4 .01
C5 300pF
C6 300pF
C7 .01
C8 .01
C9 300pF
C10 .01
C11 .01
C12 300pF
C13 1μH .01
C14 1μH .01
C15 10
C16 10
C17 10
C18 10
C19 10pF
C20 10pF
L2 1μH
L3 1μH
L4 1μH
L5 1μH
J201
J202
CHAN A INPUT
CHAN B INPUT
E23
E24
E25 REAR INPUT OPTION
E26
E27 REAR INPUT OPTION
E28
E31
E32
A7(MSB)
B7(MSB)
(LSB)
EXT GATE
REMOTE RESET
REMOTE HOLD
PART OF J26
PART OF P26
E78
E67
E65
U4A 7442
U4B 7442
U5B 7432
U3B 7400
U2B 7432
1 μS
10 μS
100 μS
1 mS
10 mS
100 mS
1 SEC
10 SEC
100 SEC
W1
READOUT PCB ASSY 406145 REF
USED ON MOD. B035B & B035B ONLY
PART OF J123
PART OF J23
PART OF J25
PART OF P25
E64
E63
E62
E61
E60
E59
E58
E57
E56
E55
E80
E42
E44
E46
E48
E40
E47
E43
E45
E41
SYS CONT
REMOTE
E82
E79
PART OF P23
PART OF J123
PART OF P22
PART OF J22
PART OF P25 J25
E81
FOR REF ONLY LOCATED ON READOUT READOUT PCB ASSY 406145



(9) W1 IS REMOVED WHEN U2B IS INSTALLED

(8) CR30 / CR31, CR32 / CR33 ARE MATCHED PAIRS

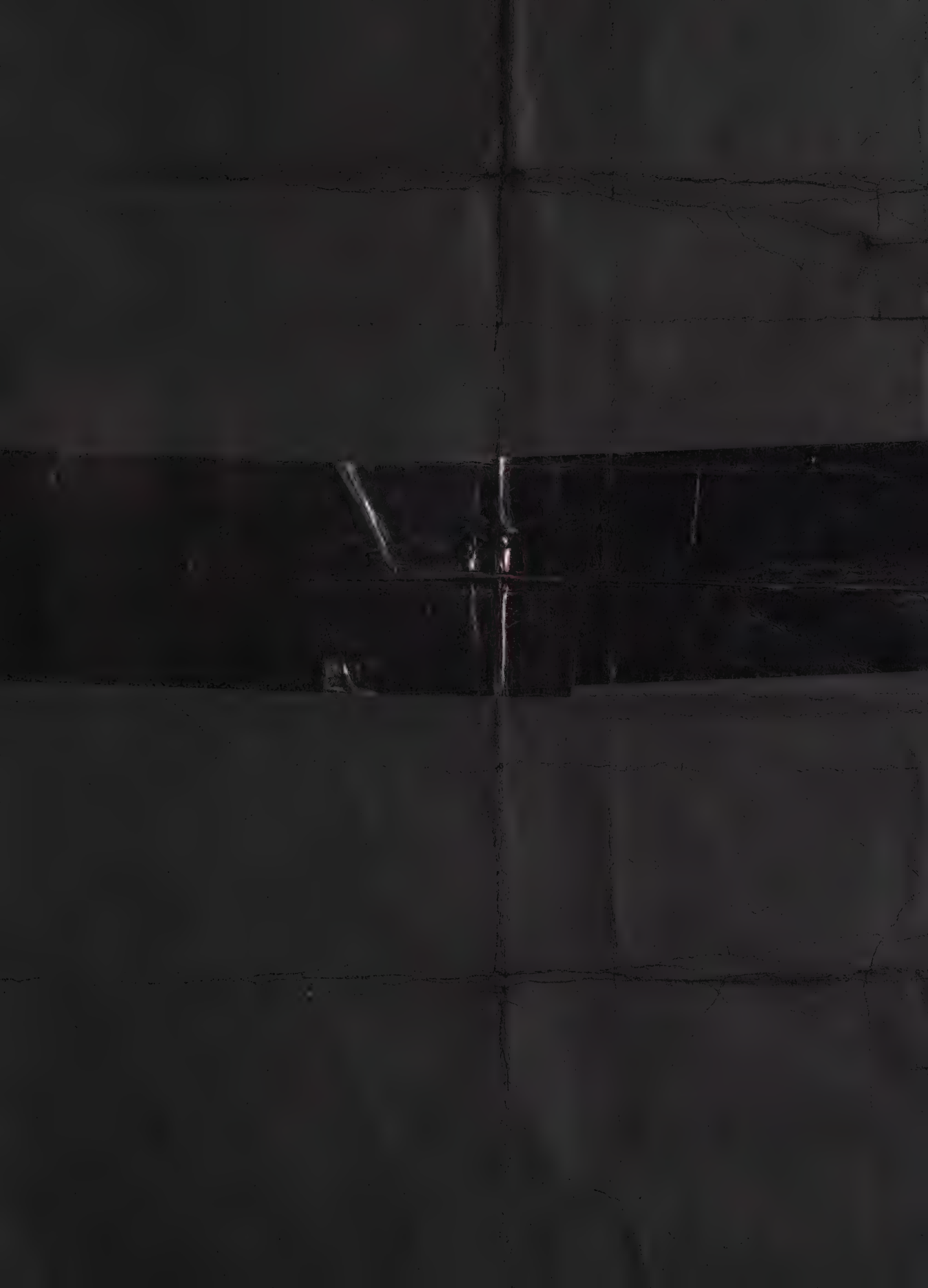
(7) Q13 / Q31, Q14 / Q32, Q15 / Q29, Q16 / Q30, Q17 / Q25, Q18 / Q26, Q19 / Q27, Q20 / Q28, Q21 / Q23, Q22 / Q24 ARE MATCHED PAIRS

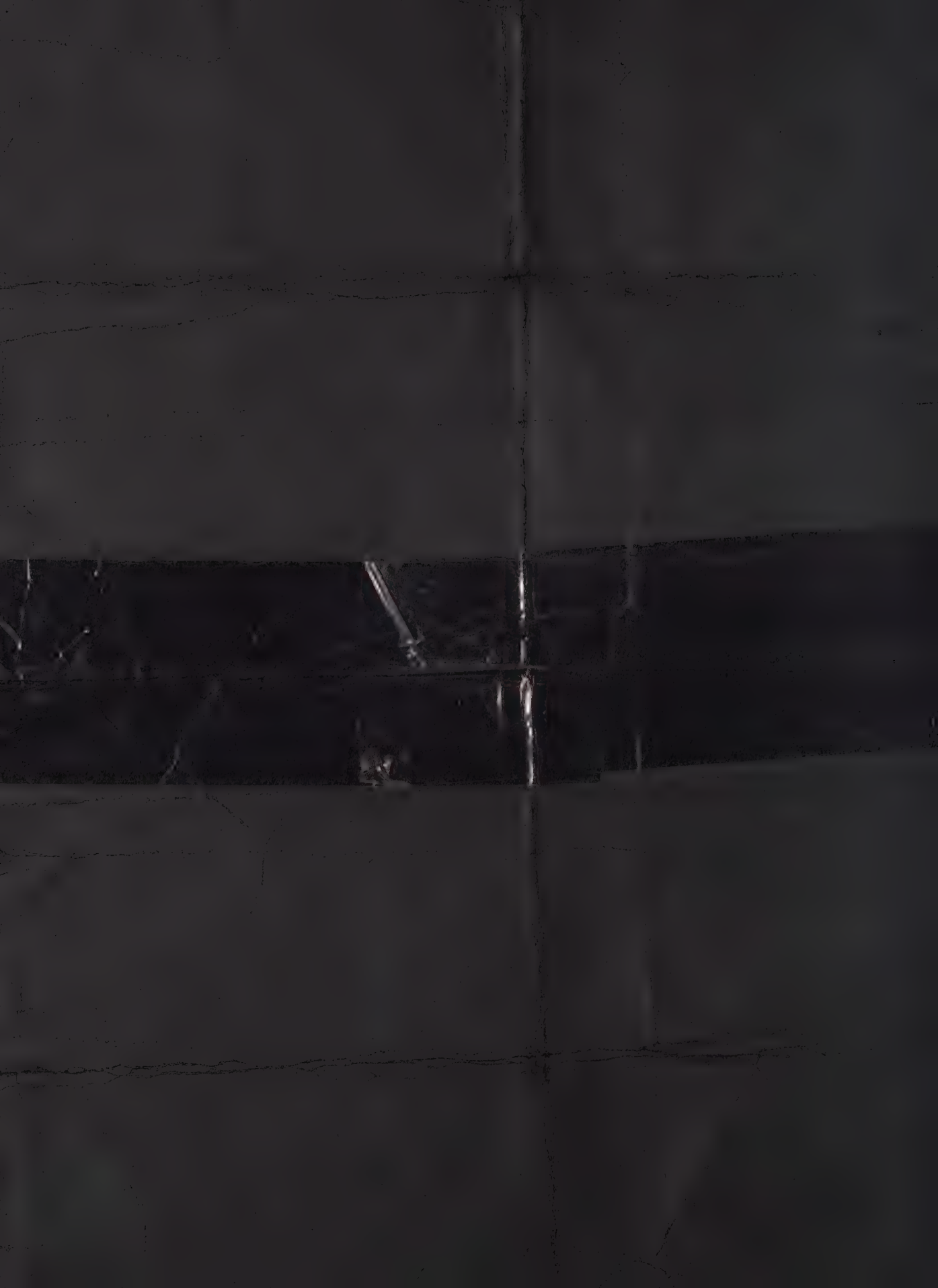
(6) R202 & R203 LOCATED ON FRT PAN WITH S202 / S203

5. RELAYS ARE 310123
4. TRANSISTORS ARE 200200
3. DIODES ARE 018
2. CAPACITORS ARE IN MFD
1. RESISTORS ARE IN OHMS ±5%, 1/4 W.

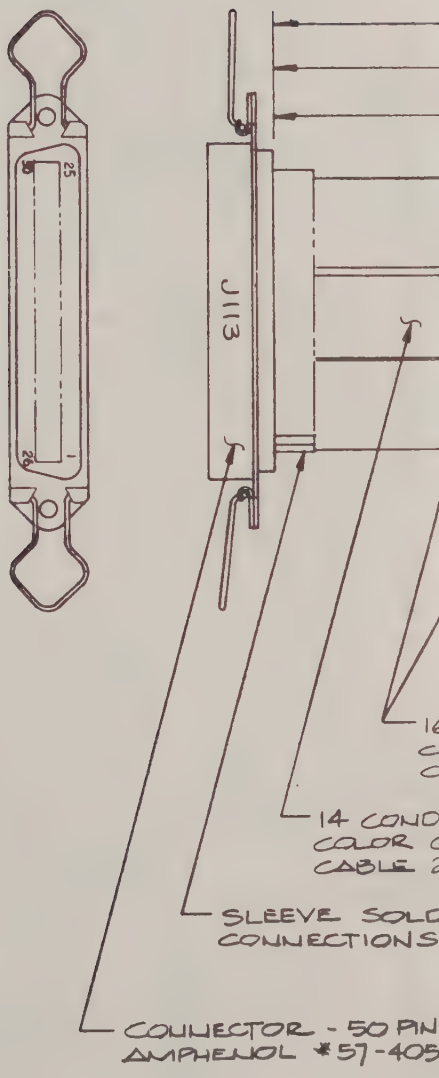
NOTE: UNLESS OTHERWISE SPECIFIED

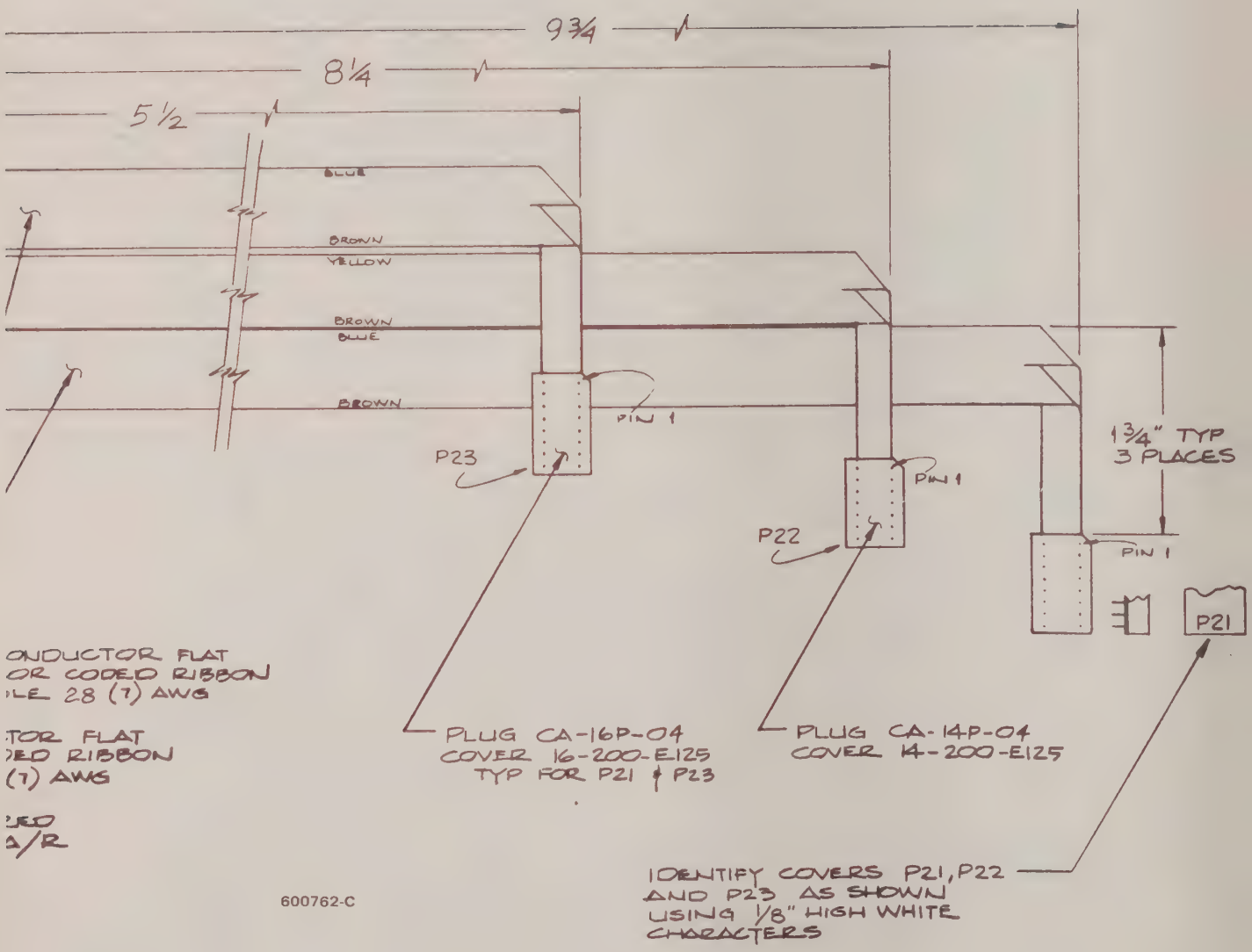
Figure 5.6 - Schematic, Programmable Signal Conditioner





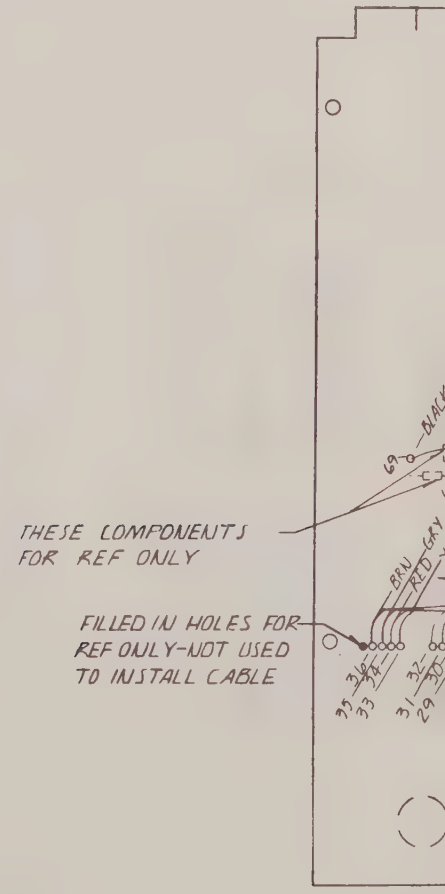
WIRE LIST		
FROM	TO	WIRE COLOR
J21-1	J113-1	BRN
2	26	RED
3	2	ORG
4	27	YEL
5	3	GRN
6	28	BLU
7	4	VIO
8	29	GRY
9	5	WHT
10	30	BLK
11	6	BRN
12	31	RED
13	7	ORG
14	32	YEL
15	8	GRN
J21-16	J113-33	BLU
J22-1	J113-9	BRN
2	34	RED
3	10	ORG
4	35	YEL
5	11	GRN
6	36	BLU
7	12	VIO
8	37	GRY
9	13	WHT
10	38	BLK
11	14	BRN
12	39	RED
13	15	ORG
J22-14	J113-40	YEL
J23-1	J113-17	BRN
2	42	RED
3	18	ORG
4	43	YEL
5	19	GRN
6	44	BLU
7	20	VIO
8	45	GRY
9	21	WHT
10	46	BLK
11	22	BRN
12	47	RED
13	23	ORG
14	48	YEL
15	24	GRN
J23-16	J113-49	BLU





TOLERANCE NOTE:
FRACTION – ± 1/4

Figure 5.7 - Assembly, Remote Programming Cable (600762)


THESE COMPONENTS
FOR REF ONLY
FILLED IN HOLES FOR
REF ONLY-NOT USED
TO INSTALL CABLE
69
BRN
RED
GRY
35
33
31
29

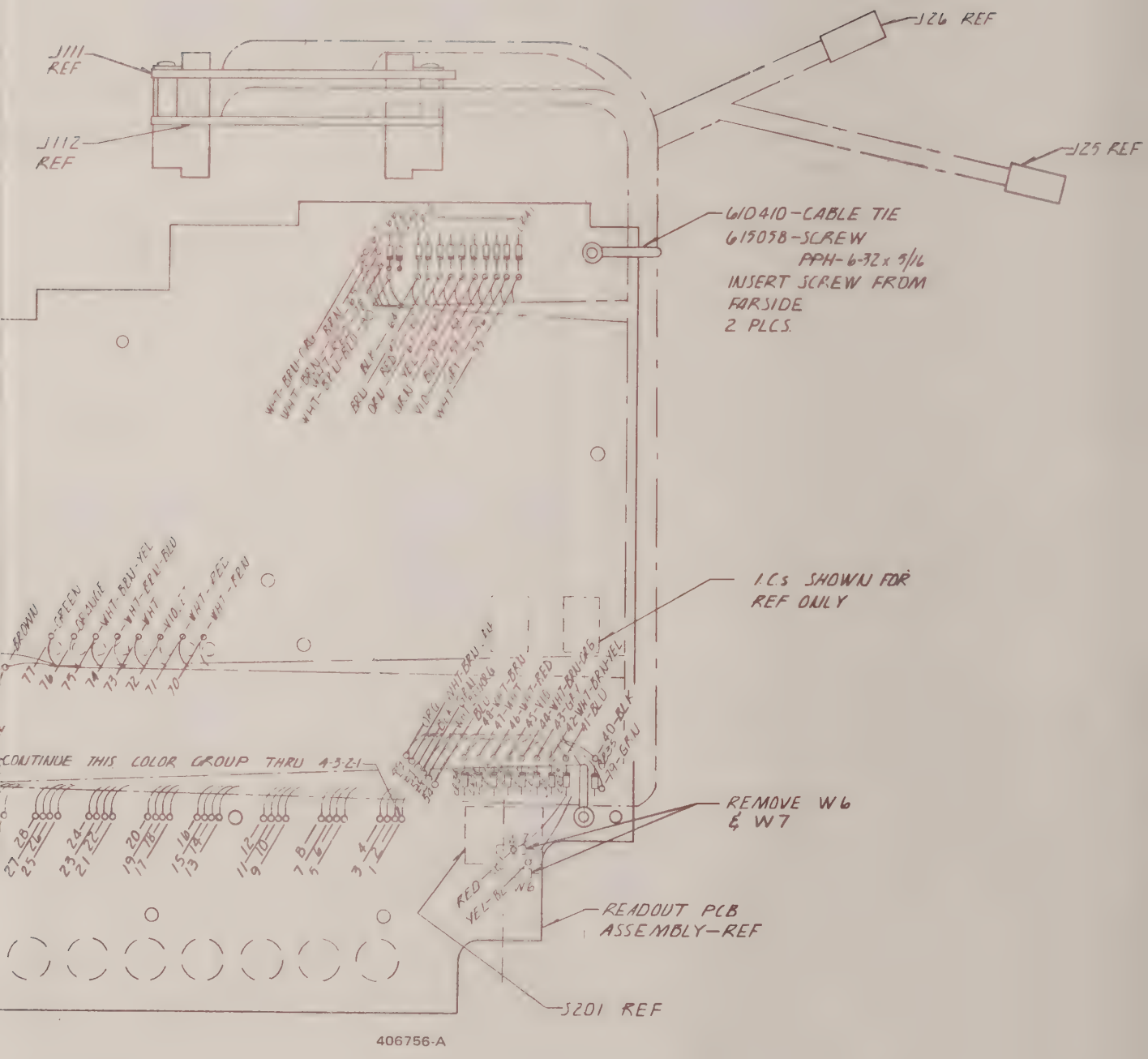
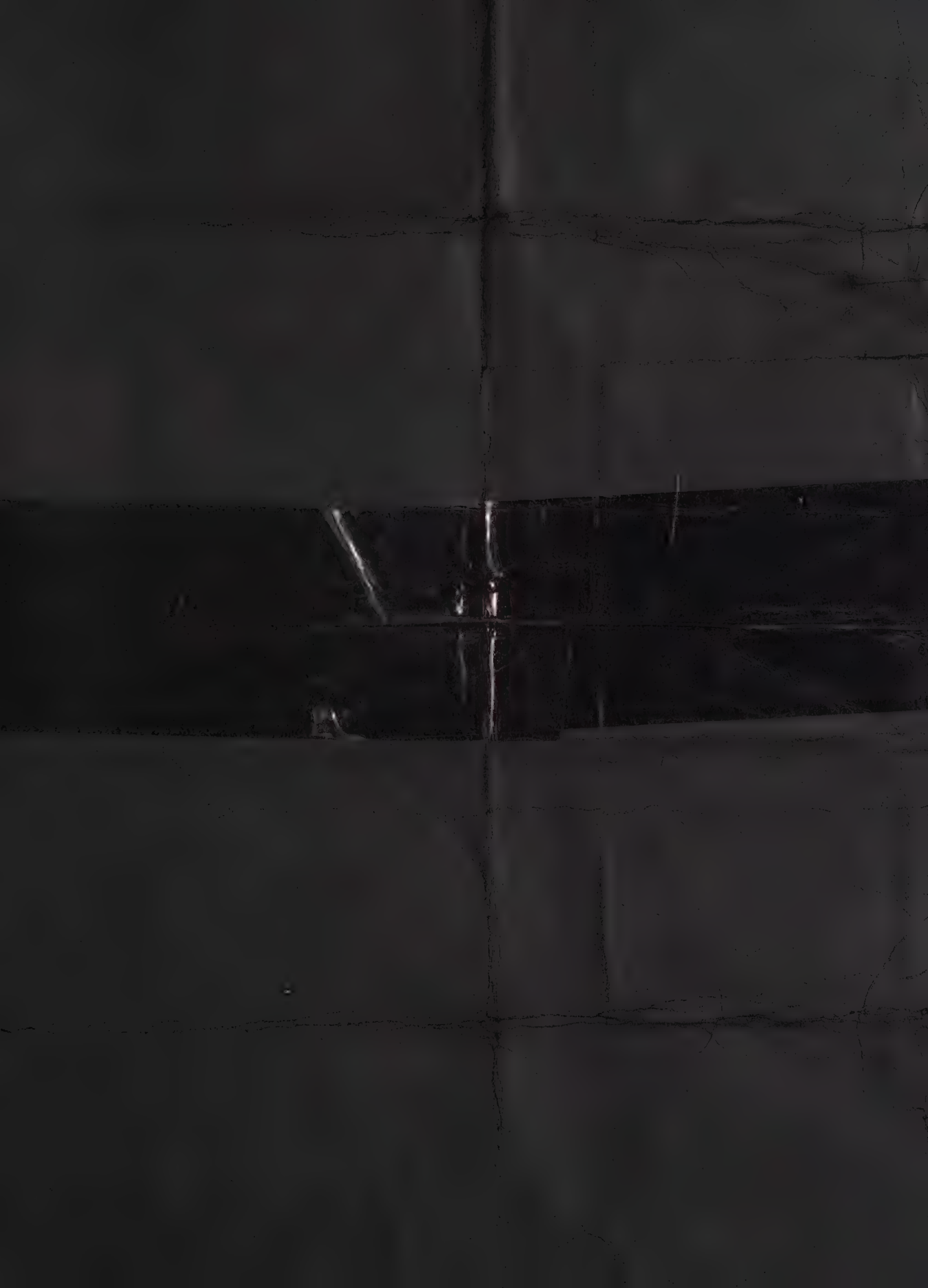
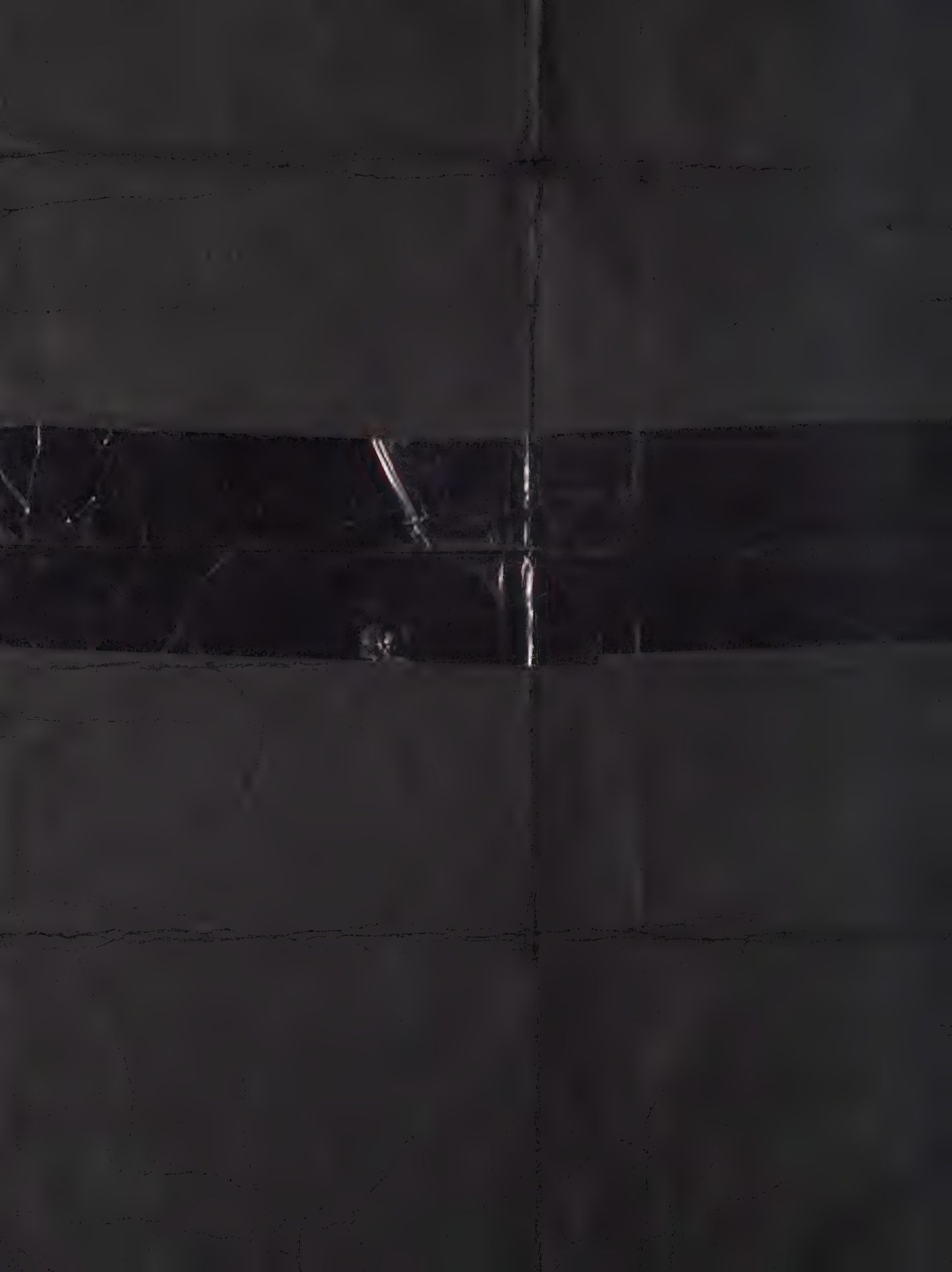
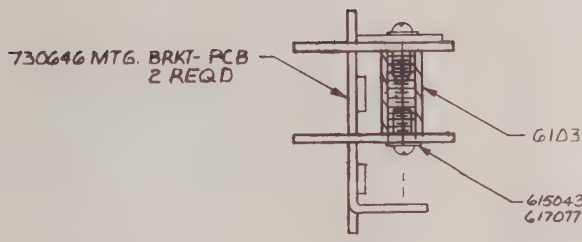


Figure 5.8 - Assembly, Interface Harness (406756)

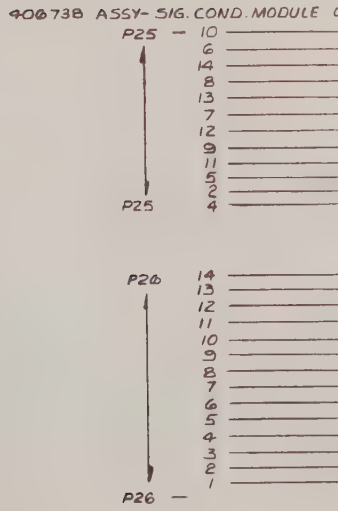






WIRING

ALL WIRES 24 GA,

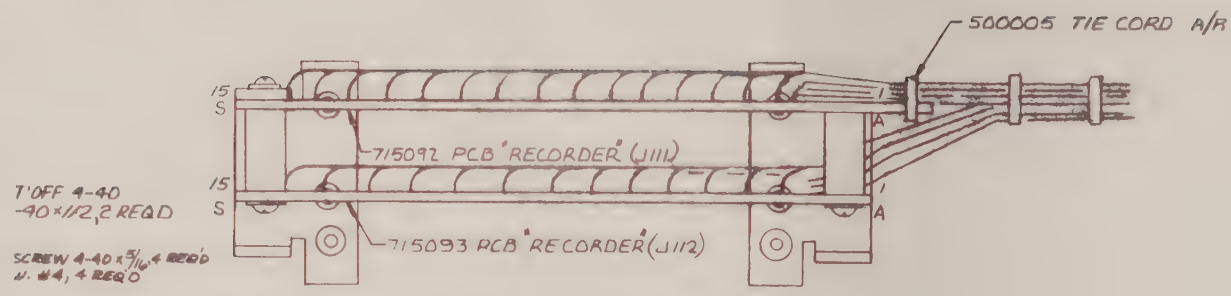


3. REMOVE JUMPERS W6 & W7 ON READOUT ASSEMBL

2. HARNESS ROUTING DWG. IS SHEET 2 OF THIS DWG

⚠6 WILL BE HARD WIRED NEXT ASSEMBLY.

NOTES: UNLESS OTHERWISE SPECIFIED



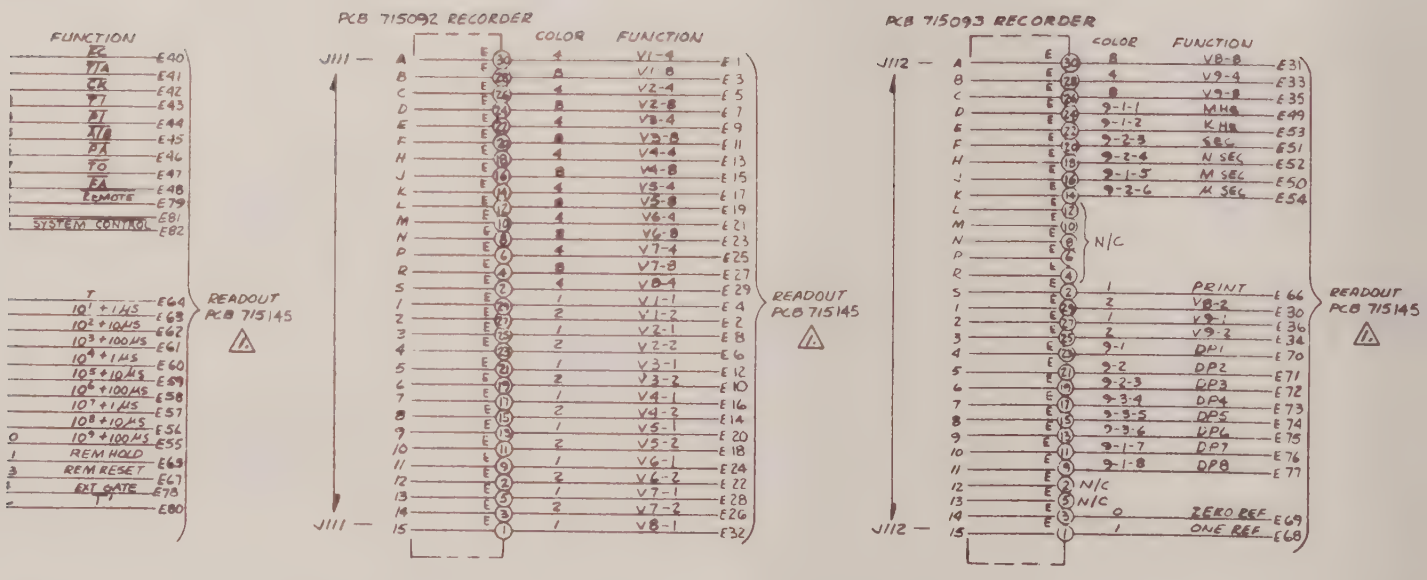


Figure 5.9 - Assembly, Remote and Recorder Harness (406733)

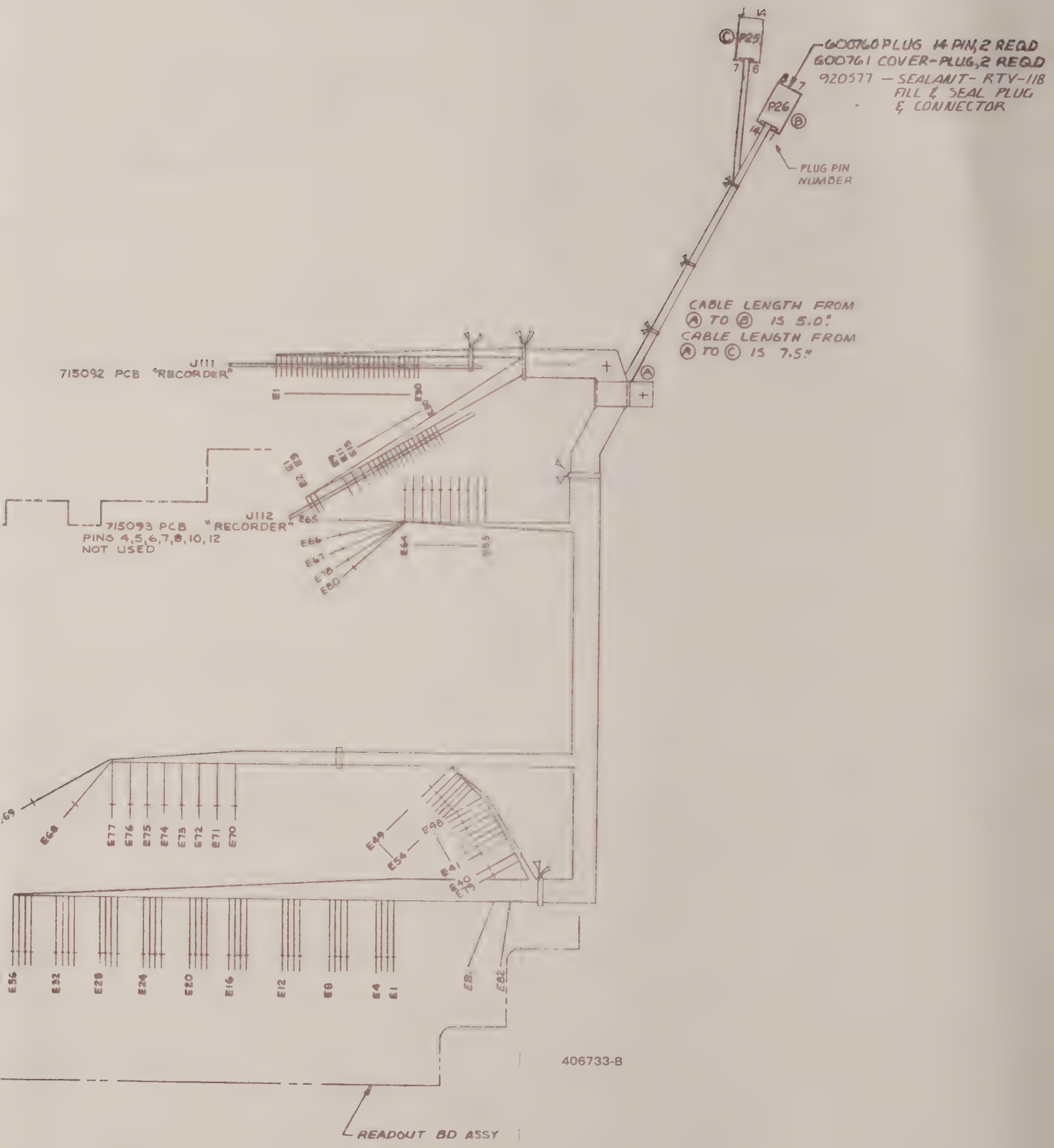
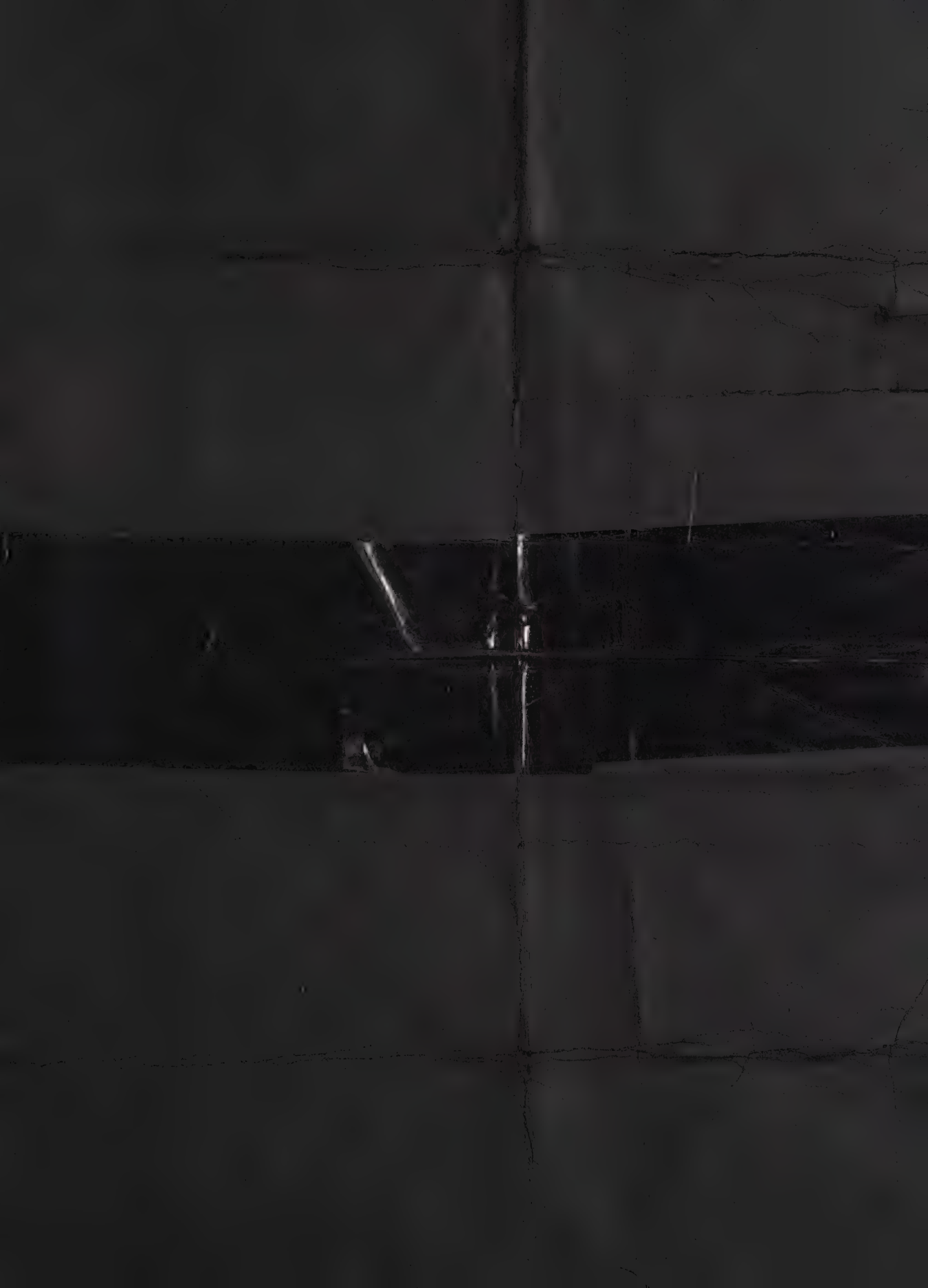
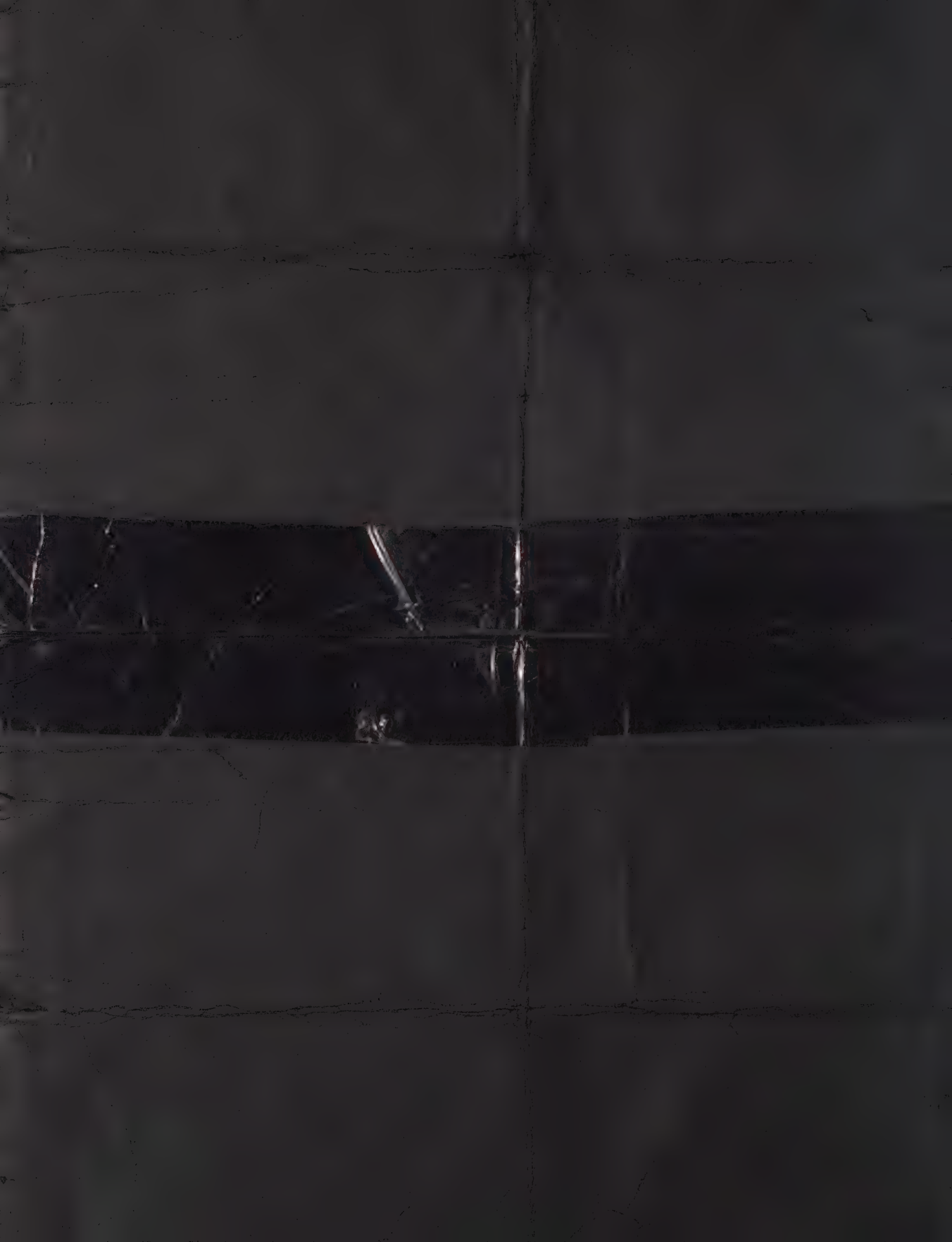
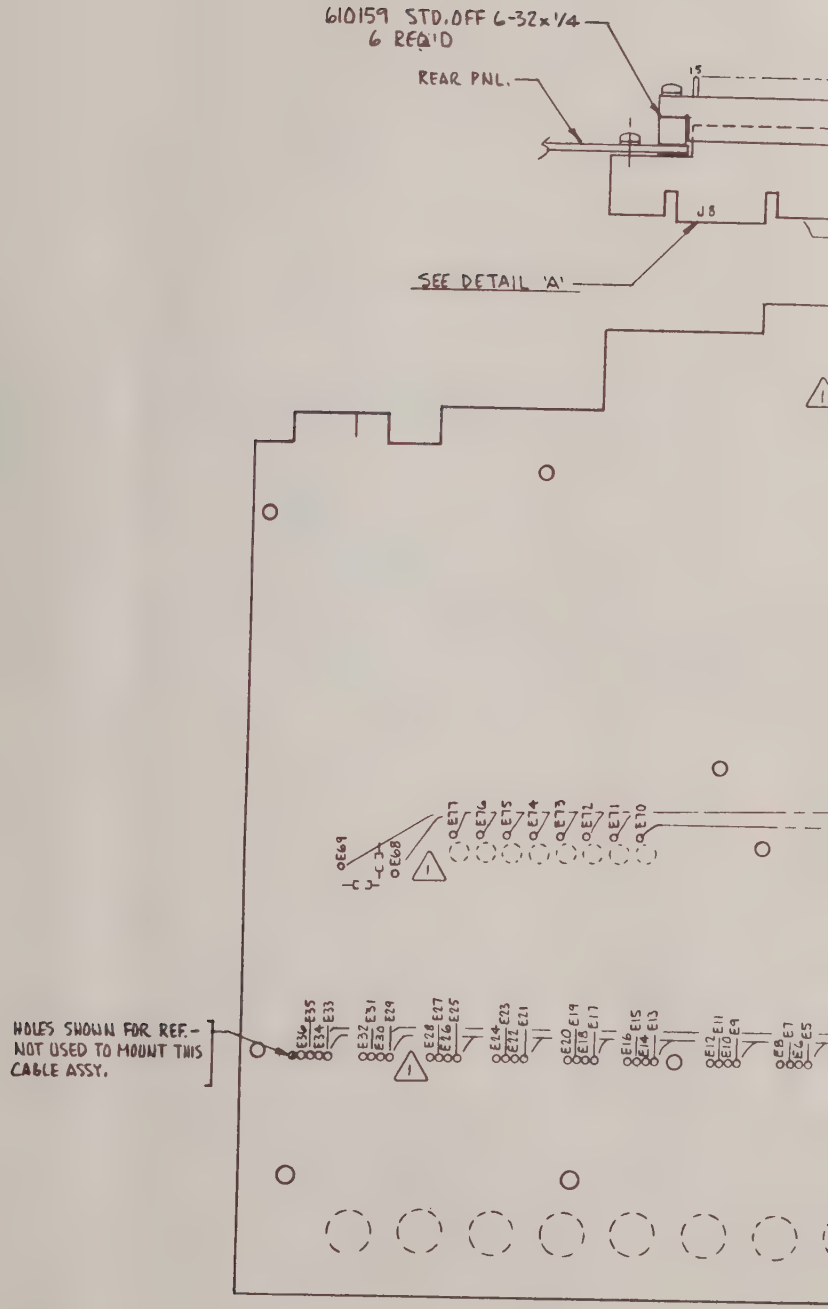


Figure 5.9 - Assembly, Remote and Recorder Harness (406733) continued






610159 STD.OFF 6-32x1/4
6 REQ'D
REAR PNL.
J8
SEE DETAIL 'A'
HOLES SHOWN FOR REF.-
NOT USED TO MOUNT THIS
CABLE ASSY.

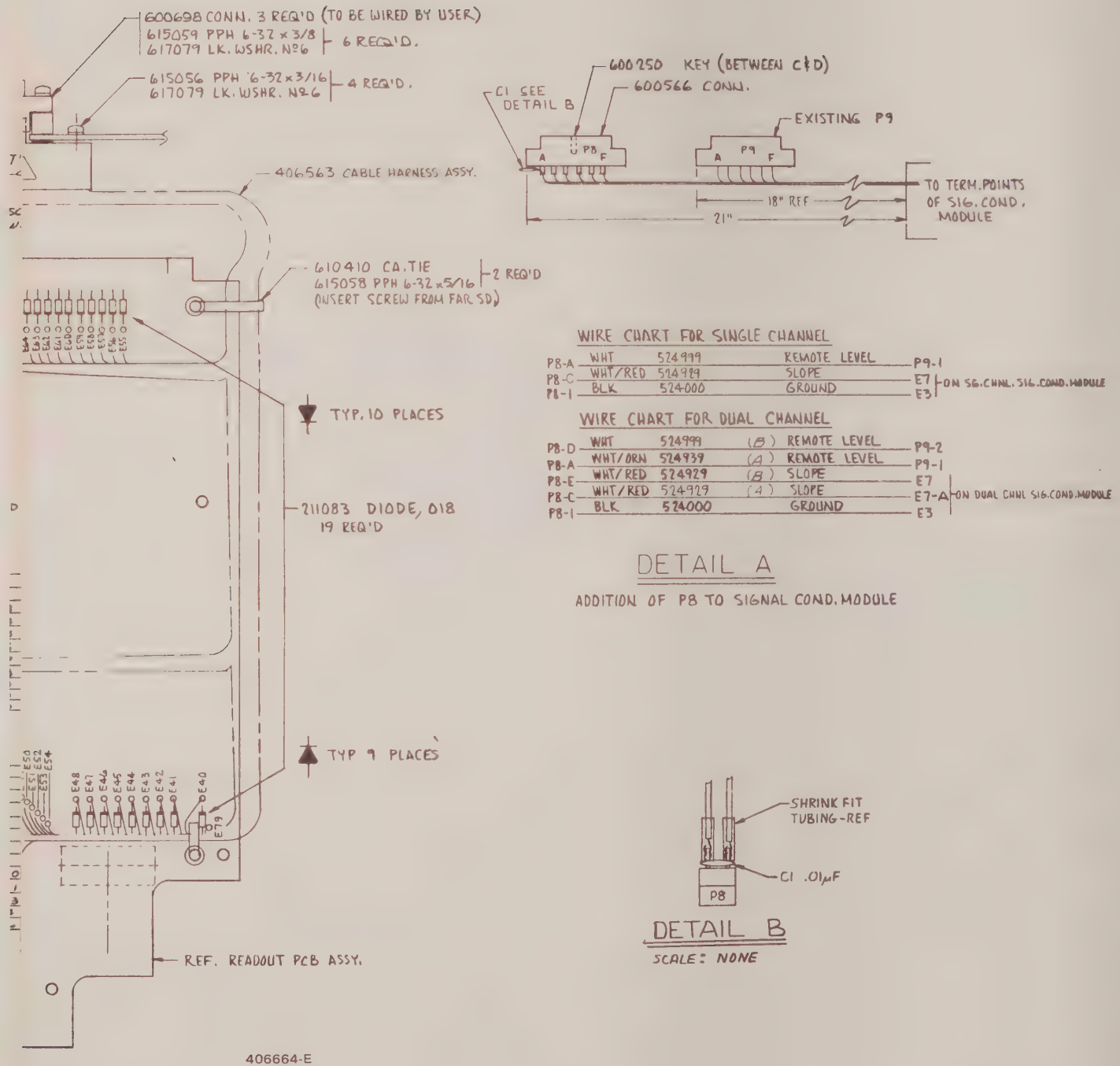
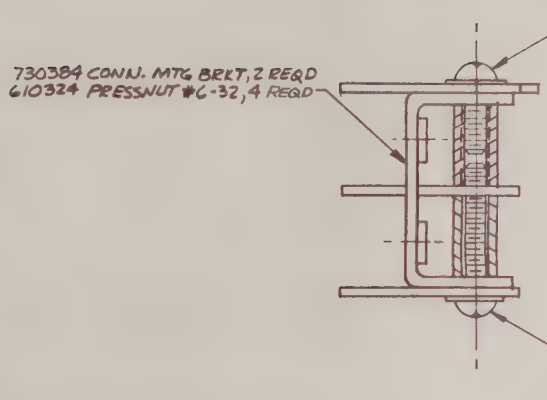


Figure 5.10 - Layout, Systems Interface (406664)

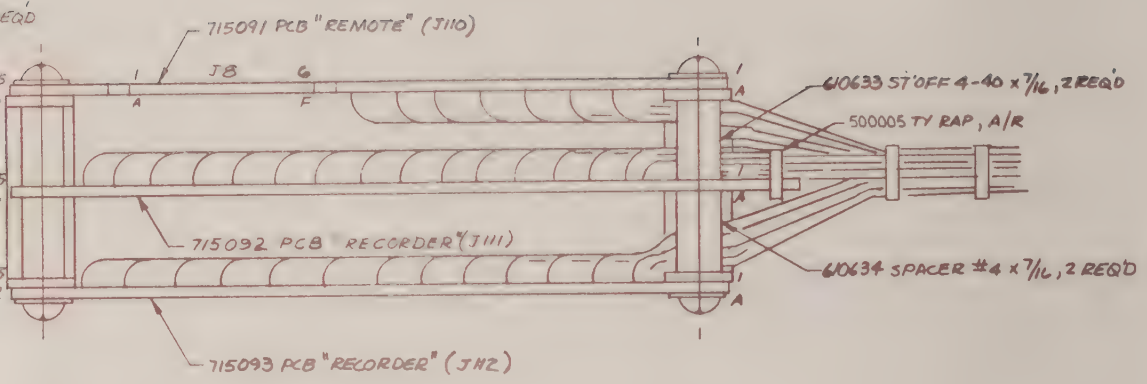

615044 PPH SCREW 4-40 x 3/8, 2
617077 LOCKW. #4, 2 REQD
730384 CONN. MTG BRKT, 2 REQD
610324 PRESSNUT #6-32, 4 REQD
J110
J111
J112
615048 PPH SCREW 4-40 x 3/4, 2 REQ
617077 LOCKW. #4, 2 REQ'D

WIRING

ALL WIRES 24 GA, COATED

PCB 715091 REMOTE

			COLOR	FUNCTION	
J110 —	A	E 18	9-0	$\overline{EC}$	E40
	B	E 16	9-1	$\overline{T/A}$	E41
	C	E 14	9-2	$\overline{CK}$	E42
	D	E 12	9-2-3	$\overline{T1}$	E43
	E	E 10	9-3-4	$\overline{P1}$	E44
	F	E 8	9-3-5	$\overline{A/B}$	E45
	H	E 6	9-3-6	$\overline{PA}$	E46
	J	L 4	9-1-7	$\overline{TO}$	E47
	K	E 2	9-1-8	$\overline{EA}$	E48
	L	E 24	9-1-4	REMOTE	E79
	M	J8-E			
	N	J8-D			
	P	J8-C			
	R	J8-B			
	S	J8-A			
	1	E 17	0	T	E64
	2	E 15	1	$10^1+1\,\mu S$	E63
	3	E 13	2	$10^2+10\,\mu S$	E62
	4	E 11	3	$10^3+100\,\mu S$	E61
	5	E 9	4	$10^4+1\,mS$	E60
	6	E 7	5	$10^5+10\,mS$	E59
	7	E 5	6	$10^6+100\,mS$	E58
	8	E 3	7	$10^7+1\,S$	E57
	9	E 1	8	$10^8+10\,S$	E56
	10	E 20	9-2-0	$10^9+100\,S$	E55
	11	E 22	9-2-1	REM HOLD	E69
	12	E 19	9-1-3	REM RESET	E67
	13	E 21	9-2-4	EXT GATE	E78
	14	E 23	9-1-6	T1	E80
J110 —	15	J8-1			


715091 PCB "REMOTE" (J110)
J8
610633 ST'OFF 4-40 x 7/16, 2 REQ'D
500005 TY RAP, A/R
715092 PCB "RECORDER" (J111)
610634 SPACER #4 x 7/16, 2 REQ'D
715093 PCB "RECORDER" (J112)

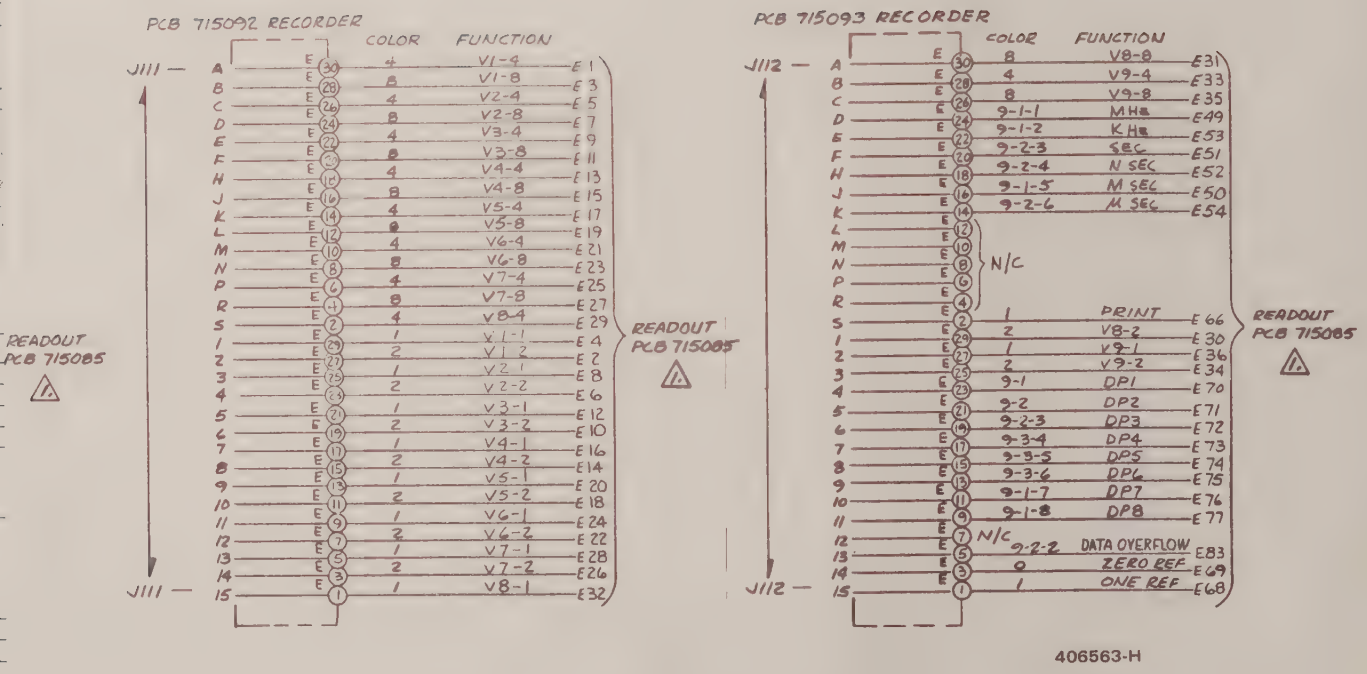
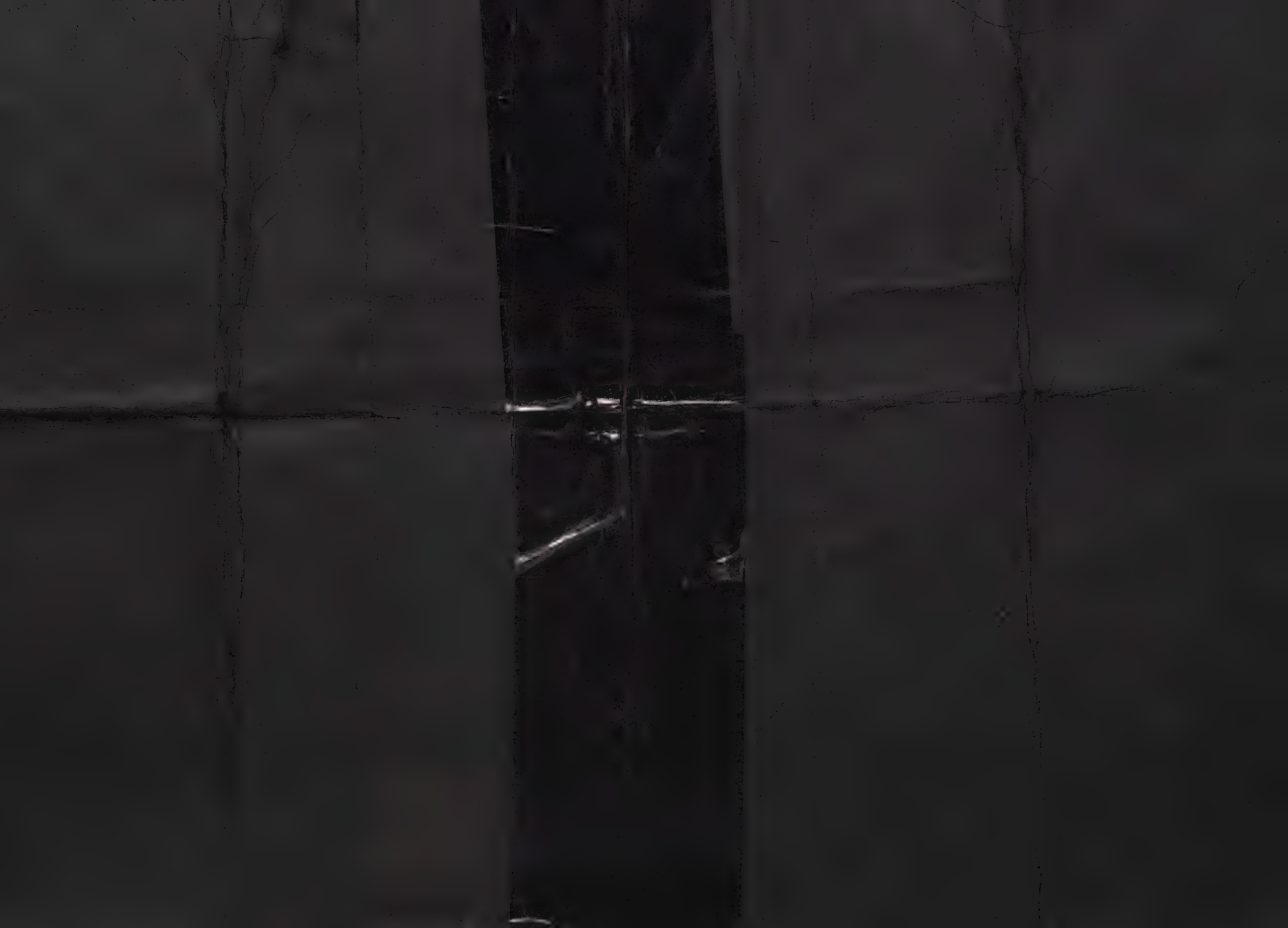


Figure 5.11 - Assembly, Remote & Recorder Harness (406563)



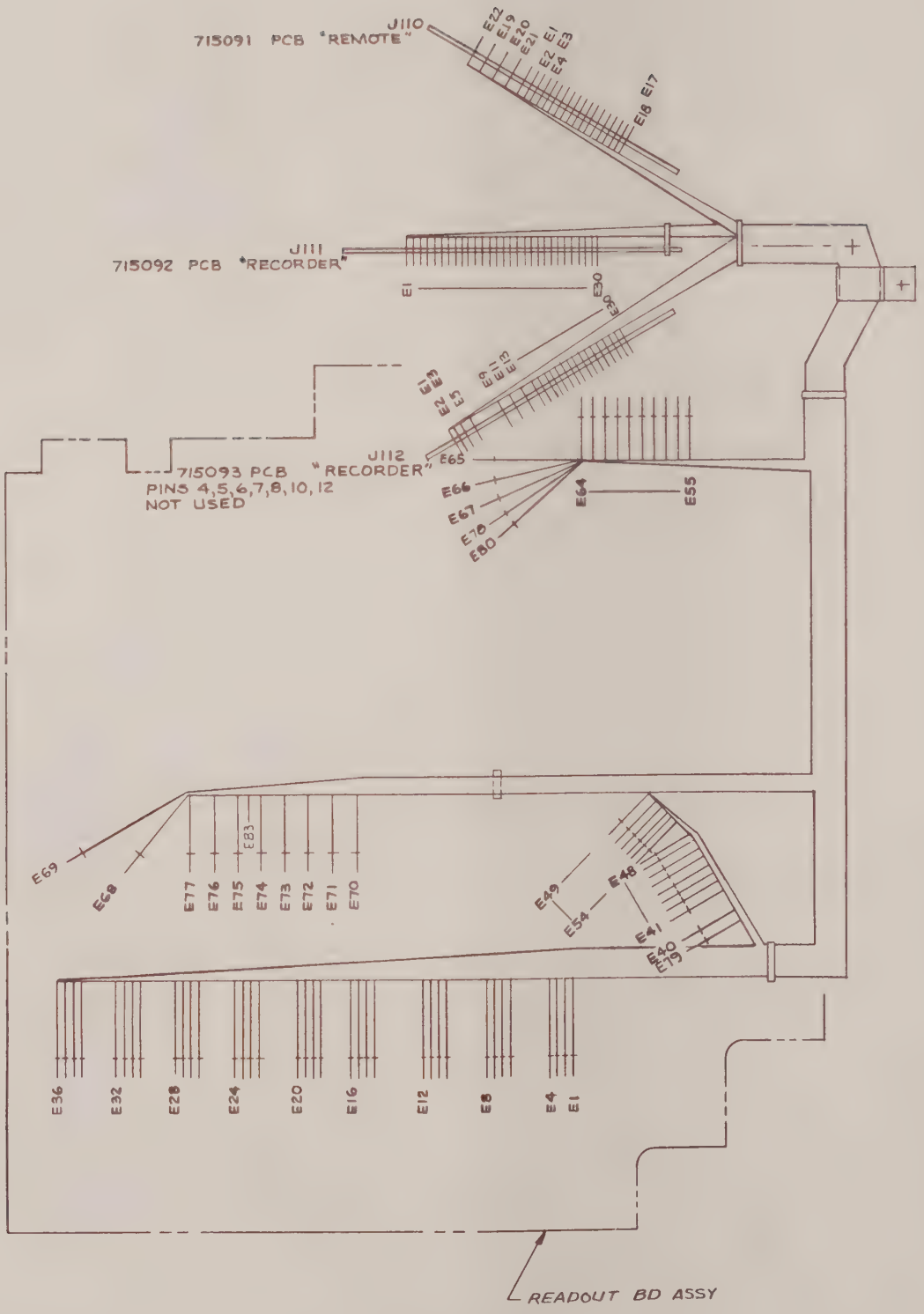


Figure 5.11 - Assembly, Remote & Recorder Harness (406563) continued

6.1 This section contains lists of replaceable parts arranged in the order of the following subassemblies:

Option 009	Page
Full Systems Interface	6-3
Rear Panel	6-4
Interconnect	6-5
Programmable Signal Conditioner Module	6-6
Programmable Signal Conditioner PCB	6-7
Interface Harness	6-16
Remote and Recorder Harness	6-17
Option 008	
Systems Interface	6-18
Remote and Recorder Harness	6-19

6.2 Manufacturers are identified by FSC numbers listed in table 6.2, "List of Suppliers". The code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1, H4-2, and their supplements.

6.3 Certain parts having 21793 (Dana) listed in the "FSC" column are specially-selected semiconductors. For some of these, standard commercial parts will serve as satisfactory replacements. These Dana parts are identified in table 6.1 along with the commercial equivalent.

Table 6.1

Semiconductor Type:	Equivalent:
007 Diode	Fairchild FD300
018 Diode	Texas Instruments 1N4448

Table 6.2 - List of Suppliers

FSC	NAME	FSC	NAME
02114	FERROXCUBE CORPORATION SAUGERTIES, NEW YORK	05397	UNION CARBIDE CORP. (Materials Systems Division) CLEVELAND, OHIO
02660	AMPHENOL CORPORATION BROADVIEW, ILLINOIS	05624	BARBER & COLMAN CO. ROCKFORD, ILLINOIS
04713	MOTOROLA, INC. (Semiconductor Products Division) PHOENIX, ARIZONA	07263	FAIRCHILD SEMICONDUCTOR (Division of Fairchild Camera & Instrument Corp.) MOUNTAIN VIEW, CALIFORNIA

Table 6.2 - List of Suppliers continued

FSC	NAME
11237	CTS KEENE, INC. PASO ROBLES, CALIFORNIA
15636	ELEC-TROL, INC. SAUGUS, CALIFORNIA
21793	DANA LABORATORIES, INC. IRVINE, CALIFORNIA
23095	AZTEC ELECTRONICS, INC. ANAHEIM, CALIFORNIA
27014	NATIONAL SEMI-CONDUCTOR CORP. SANTA CLARA, CALIFORNIA
56289	SPRAGUE ELECTRIC CO. (Pacific Division) LOS ANGELES, CALIFORNIA
71471	AEROVOX CORPORATION (Cinema Plant) MONCKS CORNER, SOUTH CAROLINA
71785	TRW ELECTRONIC COMPONENTS (Cinch Division) ELK GROVE VILLAGE, ILLINOIS
72136	ELECTRO MOTIVE MFG. CO., INC. WILLIMANTIC, CONNECTICUT
72982	ERIE TECHNOLOGICAL PRODUCTS, INC. ERIE, PENNSYLVANIA
73138	BECKMAN INSTRUMENTS, INC. (Helipot Division) FULLERTON, CALIFORNIA
75915	LITTELFUSE, INC. DES PLAINES, ILLINOIS
79727	C-W INDUSTRIES WARMINSTER, PENNSYLVANIA
80131	ELECTRONICS INDUSTRIES ASSOC. WASHINGTON, D.C.
81349	MILITARY SPECIFICATION
82389	SWITCHCRAFT, INC. CHICAGO, ILLINOIS
86884	RADIO CORP. OF AMERICA (Electronics Components Division) HARRISON, NEW JERSEY
98291	SEALECTRO CORPORATION MAMARONECK, NEW YORK
99800	AMERICAN PRECISION INDUSTRIES, INC. (Delevan Division) EAST AURORA, NEW YORK

406737 – Assy., FULL SYSTEMS INTERFACE

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
A1	406732	REAR PANEL ASSY	21793	406732
A2	406736	REMOTE PROGRAMMING CABLE ASSY	21793	406736
A3	406738	SIGNAL CONDITIONING MODULE ASSY	21793	406738
A4	406756	INTERFACE HARNESS ASSY	21793	406756

406732 – Assy., REAR PANEL , OPTION 009

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
B1	600759	FAN MOTOR TYPE AYAA 115 V	05624	Type AYAA
C1	100063	CAP CERAM .01 MFD 500V 20%	56289	5GAS-S10
C2	100063	CAP CERAM .01 MFD 500 V 20%	56289	5GAS-S10
F101	920205	FUSE GLASS .75 AMP 250 V (115V Operation)	75915	3AG3/4ASB
	920204	FUSE SLOW .50 AMP 250 V (220V Operation)	75915	3AG1/2ASB
H1	920733	FAN BLADE	21793	920733
H2	730645	FAN BRACKET	21793	730645
H3	600759	FAN MOTOR 115 V	05624	Type AYAA
J101	600619	CONN RECEPTACLE EAC-301	82389	EAC-301
J102	600567	CONN RECEPTACLE 31-236	02660	31-236
J103	600567	CONN RECEPTACLE 31-236	02660	31-236
J104	600567	CONN RECEPTACLE 31-236	02660	31-236
J105	600567	CONN RECEPTACLE 31-236	02660	31-236
P1	600566	CONN 6 PIN 251-0630160	71785	251-0630160
Q101	200223	TRANS NPN MJE521	04713	MJE521
Q102	200130	TRANS SILICO NPN MJE3055	04713	MJE3055
Q103	200183	TRANS SILICO PNP MJE371	04713	MJE371
S101	600680	SWITCH SLIDE SPDT GF-124	79727	GF-124
S102	600617	SWITCH SLIDE DPDT G126	79727	G126
S103	600521	SWITCH SLIDE DPDT 46256LFR	82389	46256LFR
T101	300065	TRANS POWER 115 V 11824	23095	11824

406128 – Assy., PCB, INTERCONNECT

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
C1	101174	CAP CERAM .001 MFD 500 V 10%	71471	SCD3X5F
P2	600575	CONN 25 PIN	71785	252-2530160
P4	600575	CONN 25 PIN	71785	252-2530160

406738 – Assy., SIGNAL CONDITIONING MODULE (009 OPTION)

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
J201	600567	CONN BNC 31-236	02660	31-236
J202	600567	CONN BNC 31-236	02660	31-236
P9	600566	CONN 6 PIN 251-0630160	71785	251-0630160
S202	600763	SWITCH ASSY X5P6081	11237	X5P6081
S203	600763	SWITCH ASSY X5P6081	11237	X5P6081
S206	600613	SWITCH SLIDE SPDT GF-124	79727	GF-124
S207	600613	SWITCH SLIDE SPDT GF-124	79727	GF-124
S208	600613	SWITCH SLIDE SPDT GF-124	79727	GF-124
S209	600613	SWITCH SLIDE SPDT GF-124	79727	GF-124
S210	600613	SWITCH SLIDE SPDT GF-124	79727	GF-124

406741 – Assy., PCB, PROGRAMMABLE SIGNAL CONDITIONER (009 OPTION)

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C2	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C3	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C4	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C5	100083	CAP	CERAM	300 PFD	500 V	10%	71471	SCD-DI-1
C6	100083	CAP	CERAM	300 PFD	500 V	10%	71471	SCD-DI-1
C7	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C8	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C9	100083	CAP	CERAM	300 PFD	500 V	10%	71471	SCD-DI-1
C10	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C11	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C12	100083	CAP	CERAM	300 PFD	500 V	10%	71471	SCD-DI-1
C13	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C14	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C15	110158	CAP	TANTA	10 MFD	50 V	10%	05397	T362C106K050A
C16	110158	CAP	TANTA	10 MFD	50 V	10%	05397	T362C106K050A
C17	110158	CAP	TANTA	10 MFD	50 V	10%	05397	T362C106K050A
C18	110158	CAP	TANTA	10 MFD	50 V	10%	05397	T362C106K050A
C19	130151	CAP	MICA	0.5 PFD	500 V		72136	DM15CD100D04CR
C20	130151	CAP	MICA	0.5 PFD	500 V		72136	DM15CD100D04CR
C21	130156	CAP	MICA	68 PFD	500 V	1%	72136	DM15ED068F04CR
C22	130156	CAP	MICA	68 PFD	500 V	1%	72136	DM15ED068F04CR
C23	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	5GAS-S10
C24	130155	CAP	MICA	510 PFD	500 V	1%	72136	DM15ED511F04CR
C25	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	5GAS-S10
C26	130155	CAP	MICA	510 PFD	500 V	1%	72136	DM15ED511F04CR
C27	130153	CAP	MICA	91 PFD	500 V	1%	72136	DM15ED910F04CR
C28	130155	CAP	MICA	510 PFD	500 V	1%	72136	DM15ED511F04CR
C29	130153	CAP	MICA	91 PFD	500 V	1%	72136	DM15ED910F04CR
C30	130155	CAP	MICA	510 PFD	500 V	1%	72136	DM15ED511F04CR
C31	130150	CAP	MICA	0.5 PFD	500 V		72136	DM15CD050D04CR
C32	130150	CAP	MICA	0.5 PFD	500 V		72136	DM15CD050D04CR
C33	100041	CAP	CERAM	25 PFD	1 KV	5%	56289	10TCCQ25
C34	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C35	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C36	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C37	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C38	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C39	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C40	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C41	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C42	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10

406741 – Assy., PCB, PROGRAMMABLE SIGNAL CONDITIONER (009 OPTION) *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C43	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C44	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C45	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C46	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C47	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C48	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C49	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C50	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	5GAS-S10
CR1	211083	DIODE	SILICO		018		21793	211083
CR2	211083	DIODE	SILICO		018		21793	211083
CR3	211083	DIODE	SILICO		018		21793	211083
CR4	211083	DIODE	SILICO		018		21793	211083
CR5	211083	DIODE	SILICO		018		21793	211083
CR6	211083	DIODE	SILICO		018		21793	211083
CR7	211083	DIODE	SILICO		018		21793	211083
CR8	211083	DIODE	SILICO		018		21793	211083
CR9	211083	DIODE	SILICO		018		21793	211083
CR10	211083	DIODE	SILICO		018		21793	211083
CR11	211083	DIODE	SILICO		018		21793	211083
CR12	211083	DIODE	SILICO		018		21793	211083
CR13	211083	DIODE	SILICO		018		21793	211083
CR14	211083	DIODE	SILICO		018		21793	211083
CR15	211083	DIODE	SILICO		018		21793	211083
CR16	211083	DIODE	SILICO		018		21793	211083
CR17	211083	DIODE	SILICO		018		21793	211083
CR18	220031	DIODE	SILICO	ZENER	1/4M3.3AZ5		04713	1/4M3.3AZ5
CR19	220031	DIODE	SILICO	ZENER	1/4M3.3AZ5		04713	1/4M3.3AZ5
CR20	220031	DIODE	SILICO	ZENER	1/4M3.3AZ5		04713	1/4M3.3AZ5
CR21	220031	DIODE	SILICO	ZENER	1/4M3.3AZ5		04713	1/4M3.3AZ5
CR22	211236	DIODE	SILICO		007		21793	211236
CR23	211236	DIODE	SILICO		007		21793	211236
CR24	211236	DIODE	SILICO		007		21793	211236
CR25	211236	DIODE	SILICO		007		21793	211236
CR26	220019	DIODE	SILICO	ZENER	1N752A		81349	1N752A
CR27	220019	DIODE	SILICO	ZENER	1N752A		81349	1N752A
CR28	220011	DIODE	SILICO	ZENER	1N968B		81349	1N968B
CR29	220011	DIODE	SILICO	ZENER	1N968B		81349	1N968B
CR30	210064	DIODE	Matched Pair with CR31		018		21793	210064
CR31	210064	DIODE	Matched Pair with CR30		018		21793	210064
CR32	210064	DIODE	Matched Pair with CR33		018		21793	210064
CR33	210064	DIODE	Matched Pair with CR32		018		21793	210064

406741 -- Assy., PCB, PROGRAMMABLE SIGNAL CONDITIONER (009 OPTION) *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
J6	600610	CONN	RECEPTACLE		50-053-0000	98291	50-053-0000
J7	600610	CONN	RECEPTACLE		50-053-0000	98291	50-053-0000
J21	920735	SOCKET	16 PIN		133-51-02-006	71785	133-51-02-006
J22	920734	SOCKET	14 PIN		133-51-02-003	71785	133-51-02-003
J23	920735	SOCKET	16 PIN		133-51-02-006	71785	133-51-02-006
J25	920734	SOCKET	14 PIN		133-51-02-003	71785	133-51-02-003
J26	920734	SOCKET	14 PIN		133-51-02-003	71785	133-51-02-003
K1	310123	RELAY	REED		RA3038-1051-02	15636	RA3038-1051-02
K2	310123	RELAY	REED		RA3038-1051-02	15636	RA3038-1051-02
K3	310123	RELAY	REED		RA3038-1051-02	15636	RA3038-1051-02
K4	310123	RELAY	REED		RA3038-1051-02	15636	RA3038-1051-02
K5	310123	RELAY	REED		RA3038-1051-02	15636	RA3038-1051-02
K6	310123	RELAY	REED		RA3038-1051-02	15636	RA3038-1051-02
K7	310123	RELAY	REED		RA3038-1051-02	15636	RA3038-1051-02
K8	310123	RELAY	REED		RA3038-1051-02	15636	RA3038-1051-02
K9	310123	RELAY	REED		RA3038-1051-02	15636	RA3038-1051-02
L1	310068	CHOKE	RF	1 μH	10%	99800	1537-12
L2	310068	CHOKE	RF	1 μH	10%	99800	1537-12
L3	310068	CHOKE	RF	1 μH	10%	99800	1537-12
L4	310068	CHOKE	RF	1 μH	10%	99800	1537-12
L5	310068	CHOKE	RF	1 μH	10%	99800	1537-12
L6	310108	CHOKE		.18 μH	10%	99800	1025-02
L7	310108	CHOKE		.18 μH	10%	99800	1025-02
Q1	200200	TRANS		NPN	200200	21793	200200
Q2	200200	TRANS		NPN	200200	21793	200200
Q3	200200	TRANS		NPN	200200	21793	200200
Q4	200200	TRANS		NPN	200200	21793	200200
Q5	200200	TRANS		NPN	200200	21793	200200
Q6	200200	TRANS		NPN	200200	21793	200200
Q7	200200	TRANS		NPN	200200	21793	200200
Q8	200200	TRANS		NPN	200200	21793	200200
Q9	200200	TRANS		NPN	200200	21793	200200
Q10	200200	TRANS		NPN	200200	21793	200200
Q11	200068	TRANS			2N4250	80131	2N4250
Q12	200068	TRANS			2N4250	80131	2N4250
Q13	200189	TRANS	Matched Pair with Q31		TIS58	21793	200189
Q14	200189	TRANS	Matched Pair with Q32		TIS58	21793	200189
Q15	200186	TRANS	Matched Pair with Q29		2N5179	21793	200186
Q16	200219	TRANS	Matched Pair with Q30		2N3563	21793	200219

406741 – Assy., PCB, PROGRAMMABLE SIGNAL CONDITIONER (009 OPTION) *continued*

REF DES	DANA P/N	DESCRIPTION			FSC	MANU P/N
Q17	200186	TRANS	Matched Pair with Q25	2N5179	21793	200186
Q18	200186	TRANS	Matched Pair with Q26	2N5179	21793	200186
Q19	200219	TRANS	Matched Pair with Q27	2N3563	21793	200219
Q20	200219	TRANS	Matched Pair with Q28	2N3563	21793	200219
Q21	200186	TRANS	Matched Pair with Q23	2N5179	21793	200186
Q22	200219	TRANS	Matched Pair with Q24	2N3563	21793	200219
Q23	200186	TRANS	Matched Pair with Q21	2N5179	21793	200186
Q24	200219	TRANS	Matched Pair with Q22	2N3563	21793	200219
Q25	200186	TRANS	Matched Pair with Q17	2N5179	21793	200186
Q26	200186	TRANS	Matched Pair with Q18	2N5179	21793	200186
Q27	200219	TRANS	Matched Pair with Q19	2N3563	21793	200219
Q28	200219	TRANS	Matched Pair with Q20	2N3563	21793	200219
Q29	200186	TRANS	Matched Pair with Q15	2N5179	21793	200186
Q30	200219	TRANS	Matched Pair with Q16	2N3563	21793	200219
Q31	200189	TRANS	Matched Pair with Q13	TIS58	21793	200189
Q32	200189	TRANS	Matched Pair with Q14	TIS58	21793	200189
Q33	200068	TRANS		2N4250	80131	2N4250
Q34	200200	TRANS	NPN	200200	21793	200200
Q35	200068	TRANS		2N4250	80131	2N4250
Q36	200200	TRANS	NPN	200200	21793	200200
Q37	200200	TRANS	NPN	200200	21793	200200
Q38	200200	TRANS	NPN	200200	21793	200200
Q39	200068	TRANS		2N4250	80131	2N4250
Q40	200068	TRANS		2N4250	80131	2N4250
Q41	200200	TRANS	NPN	200200	21793	200200
Q42	200200	TRANS	NPN	200200	21793	200200
Q43	200200	TRANS	NPN	200200	21793	200200
Q44	200200	TRANS	NPN	200200	21793	200200
Q45	200200	TRANS	NPN	200200	21793	200200
Q46	200200	TRANS	NPN	200200	21793	200200
Q47	200200	TRANS	NPN	200200	21793	200200
Q48	200200	TRANS	NPN	200200	21793	200200
Q49	200037	TRANS	SILICO NPN	2N3646	80131	2N3646
Q50	200037	TRANS	SILICO NPN	2N3646	80131	2N3646
Q51	200037	TRANS	SILICO NPN	2N3646	80131	2N3646
Q52	200037	TRANS	SILICO NPN	2N3646	80131	2N3646
B1	920563	BEAD	SHIELDING	56-59065/4B	02114	56-59065/4B
B2	920563	BEAD	SHIELDING	56-59065/4B	02114	56-59065/4B
B3	920563	BEAD	SHIELDING	56-59065/4B	02114	56-59065/4B
B4	920563	BEAD	SHIELDING	56-59065/4B	02114	56-59065/4B

406741 – Assy., PCB, PROGRAMMABLE SIGNAL CONDITIONER (009 OPTION) *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
B5	920563	BEAD	SHIELDING	56-59065/4B		02114	56-59065/4B
B6	920563	BEAD	SHIELDING	56-59065/4B		02114	56-59065/4B
R1	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R2	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R3	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R4	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R5	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R6	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R7	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R8	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R9	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R10	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R11	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R12	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R13	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R14	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R15	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R16	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R17	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R18	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R19	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R20	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R21	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R22	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R23	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R24	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R25	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R26	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R27	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R28	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R29	010719	RES	METAL	16.2 K	1% 1/10W	81349	RN55D1622F
R30	010719	RES	METAL	16.2 K	1% 1/10W	81349	RN55D1622F
R31	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R32	000271	RES	CARBON	270 OHM	5% 1/4W	81349	RC07GF271J
R33	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R34	000271	RES	CARBON	270 OHM	5% 1/4W	81349	RC07GF271J
R35	040115	POT	CERMET	500 OHM	10%	73138	62PR500
R36	010874	RES	METAL	3.92 K	1%	81349	RN55C3921F
R37	040115	POT	CERMET	500 OHM	10%	73138	62PR500
R38	010874	RES	METAL	3.92 K	1%	81349	RN55C3921F
R39	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J

406741 – Assy., PCB, PROGRAMMABLE SIGNAL CONDITIONER (009 OPTION) *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R40	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R41	000432	RES	CARBON	4.3 K		5% 1/4W	81349	RC07GF432J
R42	000432	RES	CARBON	4.3 K		5% 1/4W	81349	RC07GF432J
R43	010555	RES	METAL	1.82 K	T-2	1% 1/10W	81349	RN55C1821F
R44	010555	RES	METAL	1.82 K	T-2	1% 1/10W	81349	RN55C1821F
R45	010555	RES	METAL	1.82 K	T-2	1% 1/10W	81349	RN55C1821F
R46	010555	RES	METAL	1.82 K	T-2	1% 1/10W	81349	RN55C1821F
R47	040115	POT	CERMET	500 OHM		10%	73138	62PR500
R48	010555	RES	METAL	1.82 K	T-2	1% 1/10W	81349	RN55C1821F
R49	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R50	040115	POT	CERMET	500 OHM		10%	73138	62PR500
R51	010555	RES	METAL	1.82 K	T-2	1% 1/10W	81349	RN55C1821F
R52	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R53	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R54	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R55	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R56	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R57	010880	RES	METAL	3.09 K		1%	81349	RN55C3091F
R58	010880	RES	METAL	3.09 K		1%	81349	RN55C3091F
R59	000200	RES	CARBON	20 OHM		5% 1/4W	81349	RC07GF200J
R60	000200	RES	CARBON	20 OHM		5% 1/4W	81349	RC07GF200J
R61	010879	RES	METAL	1 M		1%	81349	RN55D1004F
R62	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R63	010879	RES	METAL	1 M		1%	81349	RN55D1004F
R64	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R65	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R66	010875	RES	METAL	124 K		1%	81349	RN55C1243F
R67	000620	RES	CARBON	62 OHM		5% 1/4W	81349	RC07GF620J
R68	010875	RES	METAL	124 K		1%	81349	RN55C1243F
R69	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R70	010631	RES	METAL	10.2 K		1% 1/10W	81349	RN55D1022F
R71	000114	RES	CARBON	110 K		5% 1/4W	81349	RC07GF114J
R72	000114	RES	CARBON	110 K		5% 1/4W	81349	RC07GF114J
R73	010879	RES	METAL	1 M		1%	81349	RN55D1004F
R74	010879	RES	METAL	1 M		1%	81349	RN55D1004F
R75	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R76	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R77	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R78	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R79	000751	RES	CARBON	750 OHM		5% 1/4W	81349	RC07GF751J
R80	010630	RES	METAL	9.09 K		1% 1/10W	81349	RN55D9091F
R81	000751	RES	CARBON	750 OHM		5% 1/4W	81349	RC07GF751J

406741 – Assy., PCB, PROGRAMMABLE SIGNAL CONDITIONER (009 OPTION) *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R82	010630	RES	METAL	9.09 K		1% 1/10W	81349	RN55D9091F
R83	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R84	010705	RES	METAL	4.53 K	T-0	1% 1/10W	81349	RN55D4531F
R85	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R86	010705	RES	METAL	4.53 K	T-0	1% 1/10W	81349	RN55D4531F
R87	000751	RES	CARBON	750 OHM		5% 1/4W	81349	RC07GF751J
R88	000751	RES	CARBON	750 OHM		5% 1/4W	81349	RC07GF751J
R89	000910	RES	CARBON	91 OHM		5% 1/4W	81349	RC07GF910J
R90	000470	RES	CARBON	47 OHM		5% 1/4W	81349	RC07GF470J
R91	000910	RES	CARBON	91 OHM		5% 1/4W	81349	RC07GF910J
R92	000470	RES	CARBON	47 OHM		5% 1/4W	81349	RC07GF470J
R93	000152	RES	CARBON	1.5 K		5% 1/4W	81349	RC07GF152J
R94	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R95	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R96	000430	RES	CARBON	43 OHM		5% 1/4W	81349	RC07GF430J
R97	001100	RES	CARBON	2.2 K		5% 1/2W	81349	RC20GF222J
R98	000430	RES	CARBON	43 OHM		5% 1/4W	81349	RC07GF430J
R99	001100	RES	CARBON	2.2 K		5% 1/2W	81349	RC20GF222J
R100	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R101	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R102	040123	POT	CERMET	1 K	62-1-1-102		73138	62-1-1-102
R103	040123	POT	CERMET	1 K	62-1-1-102		73138	62-1-1-102
R104	000152	RES	CARBON	1.5 K		5% 1/4W	81349	RC07GF152J
R105	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R106	000910	RES	CARBON	91 OHM		5% 1/4W	81349	RC07GF910J
R107	000470	RES	CARBON	47 OHM		5% 1/4W	81349	RC07GF470J
R108	001100	RES	CARBON	2.2 K		5% 1/2W	81349	RC20GF222J
R109	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R110	000910	RES	CARBON	91 OHM		5% 1/4W	81349	RC07GF910J
R111	000470	RES	CARBON	47 OHM		5% 1/4W	81349	RC07GF470J
R112	001100	RES	CARBON	2.2 K		5% 1/2W	81349	RC20GF222J
R113	040110	POT		100 OHM	62PR100		73138	62PR100
R114	040110	POT		100 OHM	62PR100		73138	62PR100
R115	001874	RES	CARBON	680 OHM		5% 1/2W		
R116	000751	RES	CARBON	750 OHM		5% 1/4W	81349	RC07GF751J
R117	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R118	010705	RES	METAL	4.53 K	T-0	1% 1/10W	81349	RN55D4531F
R119	001874	RES	CARBON	680 OHM		5% 1/2W		
R120	000751	RES	CARBON	750 OHM		5% 1/4W	81349	RC07GF751J
R121	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R122	010705	RES	METAL	4.53 K	T-0	1% 1/10W	81349	RN55D4531F
R123	010630	RES	METAL	9.09 K		1% 1/10W	81349	RN55D9091F

406741 -- Assy., PCB, PROGRAMMABLE SIGNAL CONDITIONER (009 OPTION) *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R124	010630	RES	METAL	9.09 K		1% 1/10W	81349	RN55D9091F
R125	010873	RES	METAL	2.21 K		1%	81349	RN55C2211F
R126	010631	RES	METAL	10.2 K		1% 1/10W	81349	RN55D1022F
R127	010873	RES	METAL	2.21 K		1%	81349	RN55C2211F
R128	010631	RES	METAL	10.2 K		1% 1/10W	81349	RN55D1022F
R129	010555	RES	METAL	1.82 K	T-2	1% 1/10W	81349	RN55C1821F
R130	010705	RES	METAL	4.53 K	T-0	1% 1/10W	81349	RN55D4531F
R131	010555	RES	METAL	1.82 K	T-2	1% 1/10W	81349	RN55C1821F
R132	010705	RES	METAL	4.53 K	T-0	1% 1/10W	81349	RN55D4531F
R133	010878	RES	METAL	348 K		1%	81349	RN55C3483F
R134	010878	RES	METAL	348 K		1%	81349	RN55C3483F
R135	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R136	000391	RES	CARBON	390 OHM		5% 1/4W	81349	RC07GF391J
R137	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R138	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R139	000391	RES	CARBON	390 OHM		5% 1/4W	81349	RC07GF391J
R140	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R141	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R142	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R143	010892	RES	METAL	383 K		1%	81349	RN55C3833F
R144	010892	RES	METAL	383 K		1%	81349	RN55C3833F
R145	010892	RES	METAL	383 K		1%	81349	RN55C3833F
R146	010892	RES	METAL	383 K		1%	81349	RN55C3833F
R147	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R148	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R149	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R150	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R151	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R152	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R153	000682	RES	CARBON	6.8 K		5% 1/4W	81349	RC07GF682J
R154	000682	RES	CARBON	6.8 K		5% 1/4W	81349	RC07GF682J
R155	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R156	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R157	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R158	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R159	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R160	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R161	000682	RES	CARBON	6.8 K		5% 1/4W	81349	RC07GF682J
R162	000682	RES	CARBON	6.8 K		5% 1/4W	81349	RC07GF682J
R163	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R164	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R165	000391	RES	CARBON	390 OHM		5% 1/4W	81349	RC07GF391J

406741 – Assy., PCB, PROGRAMMABLE SIGNAL CONDITIONER (009 OPTION) *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
R166	000391	RES CARBON 390 OHM 5% 1/4W	81349	RC07GF391J
R167	000241	RES CARBON 240 OHM 5% 1/4W	81349	RC07GF241J
R168	000241	RES CARBON 240 OHM 5% 1/4W	81349	RC07GF241J
R169	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R170	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R171	000100	RES CARBON 10 OHM 5% 1/4W	81349	RC07GF100J
R172	010631	RES METAL 10.2 K 1% 1/10W	81349	RN55D1022F
R173	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R174	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R175	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
AR1	230110	INTEGRATED CIRCUIT OP AMP	27014	LM301A
AR2	230110	INTEGRATED CIRCUIT OP AMP	27014	LM301A
U1C	230187	INTEGRATED CIRCUIT MC1406L	04713	MC1406L
U1C	920460	SOCKET INTEGRATED CIRCUIT 14 PIN		CA-14S-TSD-E
U1D	230118	INTEGRATED CIRCUIT NPN CA3086	86884	CA3086
U1D	920460	SOCKET INTEGRATED CIRCUIT 14 PIN		CA-14S-TSD-E
U2B*	230116	INTEGRATED CIRCUIT PLASTIC 7432	07263	7432
U2B	920734	SOCKET INTEGRATED CIRCUIT 14 PIN	71785	133-51-02-003
U3B	230028	INTEGRATED CIRCUIT CERAM SN7400	07263	SN7400
U3B	920734	SOCKET INTEGRATED CIRCUIT 14 PIN	71785	133-51-02-003
U3C	230115	INTEGRATED CIRCUIT PLASTIC 7409	07263	7409
U3C	920460	SOCKET INTEGRATED CIRCUIT 14 PIN		CA-14S-TSD-E
U3D	230115	INTEGRATED CIRCUIT PLASTIC 7409	07263	7409
U3D	920460	SOCKET INTEGRATED CIRCUIT 14 PIN		CA-14S-TSD-E
U4A	230074	INTEGRATED CIRCUIT PLASTIC 7442	07263	7442
U4A	920735	SOCKET INTEGRATED CIRCUIT 16 PIN	71785	133-51-02-006
U4B	230074	INTEGRATED CIRCUIT PLASTIC 7442	07263	7442
U4B	920735	SOCKET INTEGRATED CIRCUIT 16 PIN	71785	133-51-02-006
U5B	230116	INTEGRATED CIRCUIT PLASTIC 7432	07263	7432
U5B	920460	SOCKET INTEGRATED CIRCUIT 14 PIN		CA-14S-TSD-E
U5C	230187	INTEGRATED CIRCUIT MC1406L	04713	MC1406L
U5C	920460	SOCKET INTEGRATED CIRCUIT 14 PIN		CA-14S-TSD-E
U5D	230118	INTEGRATED CIRCUIT NPN CA3086	86884	CA3086
U5D	920460	SOCKET INTEGRATED CIRCUIT 14 PIN		CA-14S-TSD-E
W1	600245	JUMPER L-2007-1LP		L-2007-1LP

*Used on 8015B and 8035B Units only

406756 – Assy., HARNESS INTERFACE

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
A1	406733	CABLE HARNESS ASSY	21793	406733
CR31	211083	DIODE SILICO 018	21793	211083
CR32	211083	DIODE SILICO 018	21793	211083
CR33	211083	DIODE SILICO 018	21793	211083
CR34	211083	DIODE SILICO 018	21793	211083
CR35	211083	DIODE SILICO 018	21793	211083
CR36	211083	DIODE SILICO 018	21793	211083
CR37	211083	DIODE SILICO 018	21793	211083
CR38	211083	DIODE SILICO 018	21793	211083
CR39	211083	DIODE SILICO 018	21793	211083
CR40	211083	DIODE SILICO 018	21793	211083
CR41	211083	DIODE SILICO 018	21793	211083
CR42	211083	DIODE SILICO 018	21793	211083
CR43	211083	DIODE SILICO 018	21793	211083
CR44	211083	DIODE SILICO 018	21793	211083
CR45	211083	DIODE SILICO 018	21793	211083
CR46	211083	DIODE SILICO 018	21793	211083
CR47	211083	DIODE SILICO 018	21793	211083
CR48	211083	DIODE SILICO 018	21793	211083
CR49	211083	DIODE SILICO 018	21793	211083
CR50	211083	DIODE SILICO 018	21793	211083
CR51	211083	DIODE SILICO 018	21793	211083
CR52	211083	DIODE SILICO 018	21793	211083

406733 – Assy., REMOTE & RECORDER, OPTION 009

REF DES	DANA P/N	DESCRIPTION			FSC	MANU P/N
J111	715092	RECORDER	PCB	715092	21793	715092
J112	715093	RECORDER	PCB	715093	21793	715093
P25	600760	PLUG	14 PIN	CA-14P-05		CA-14P-05
P26	600760	PLUG	14 PIN	CA-14P-05		CA-14P-05

406664 – Assy., PCB, SYSTEMS INTERFACE, OPTION 008

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
A1	406563	ASSY CABLE HARNESS 406563	21793	406563
C1	100017	CAP CERAM .01 MFD 100 V 20%	56289	TG-S10
CR31	211083	DIODE SILICO 018	21793	211083
CR32	211083	DIODE SILICO 018	21793	211083
CR33	211083	DIODE SILICO 018	21793	211083
CR34	211083	DIODE SILICO 018	21793	211083
CR35	211083	DIODE SILICO 018	21793	211083
CR36	211083	DIODE SILICO 018	21793	211083
CR37	211083	DIODE SILICO 018	21793	211083
CR38	211083	DIODE SILICO 018	21793	211083
CR39	211083	DIODE SILICO 018	21793	211083
CR41	211083	DIODE SILICO 018	21793	211083
CR42	211083	DIODE SILICO 018	21793	211083
CR43	211083	DIODE SILICO 018	21793	211083
CR44	211083	DIODE SILICO 018	21793	211083
CR45	211083	DIODE SILICO 018	21793	211083
CR46	211083	DIODE SILICO 018	21793	211083
CR47	211083	DIODE SILICO 018	21793	211083
CR48	211083	DIODE SILICO 018	21793	211083
CR49	211083	DIODE SILICO 018	21793	211083
CR50	211083	DIODE SILICO 018	21793	211083
P8	600566	CONN 6 PIN 251-0630160	71785	251-0630160
P110	600698	CONN 15 PIN 251-15-30-260	71785	251-15-30-260
P111	600698	CONN 15 PIN 251-15-30-260	71785	251-15-30-260
P112	600698	CONN 15 PIN 251-15-30-260	71785	251-15-30-260

406563 – Assy., REMOTE & RECORDER HARNESS

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
J110	715091	PCB 15 PIN	21793	715091
J111	715092	PCB 15 PIN	21793	715092
J112	715093	PCB 15 PIN	21793	715093

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